



# HD74AC273

## Octal D-Type Flip-Flop

REJ03D0265-0200Z  
(Previous ADE-205-386 (Z))  
Rev.2.00  
Jul.16.2004

### Description

The HD74AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flops's Q output

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### Features

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See HD74AC373 for Transparent Latch Version
- See HD74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- Ordering Information

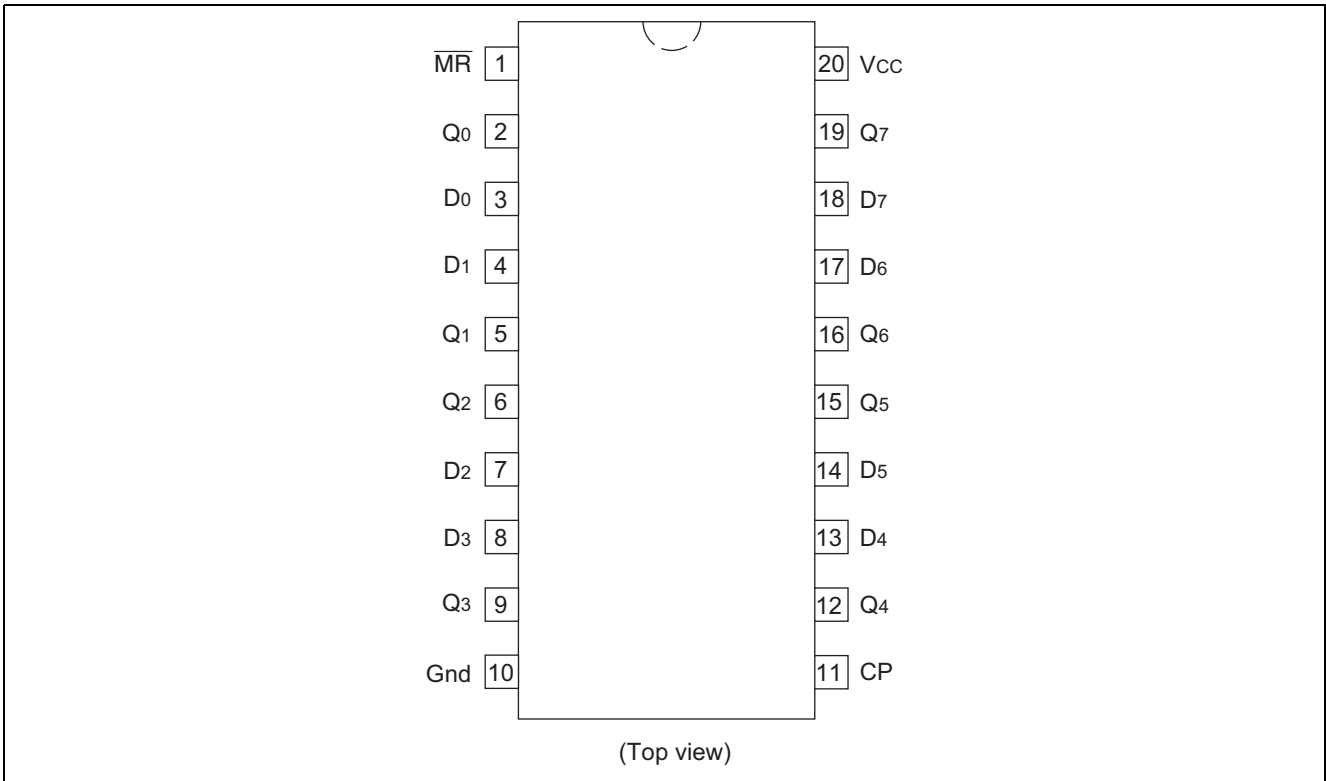
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC273P	DIP-20 pin	DP-20N	P	—
HD74AC273FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74AC273RPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)

Notes: 1. Please consult the sales office for the above package availability.

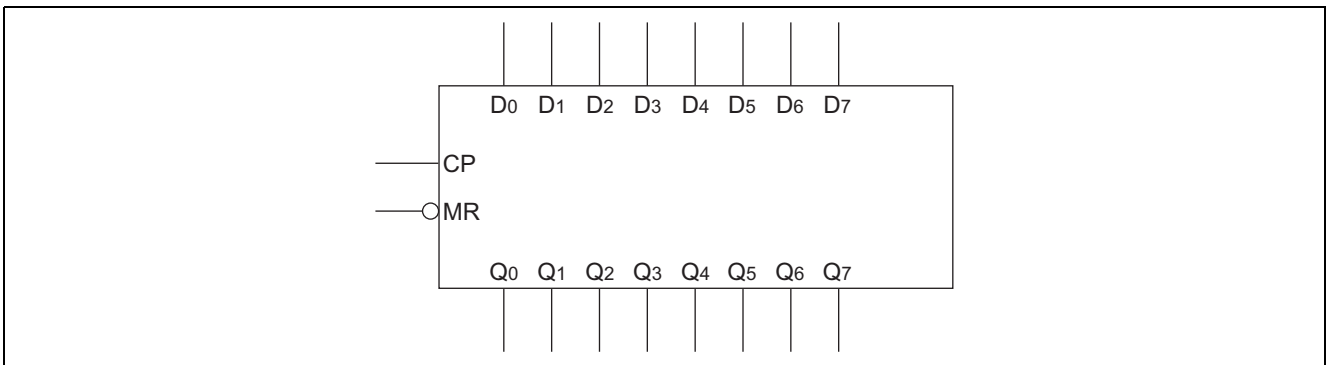
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.



### Pin Arrangement



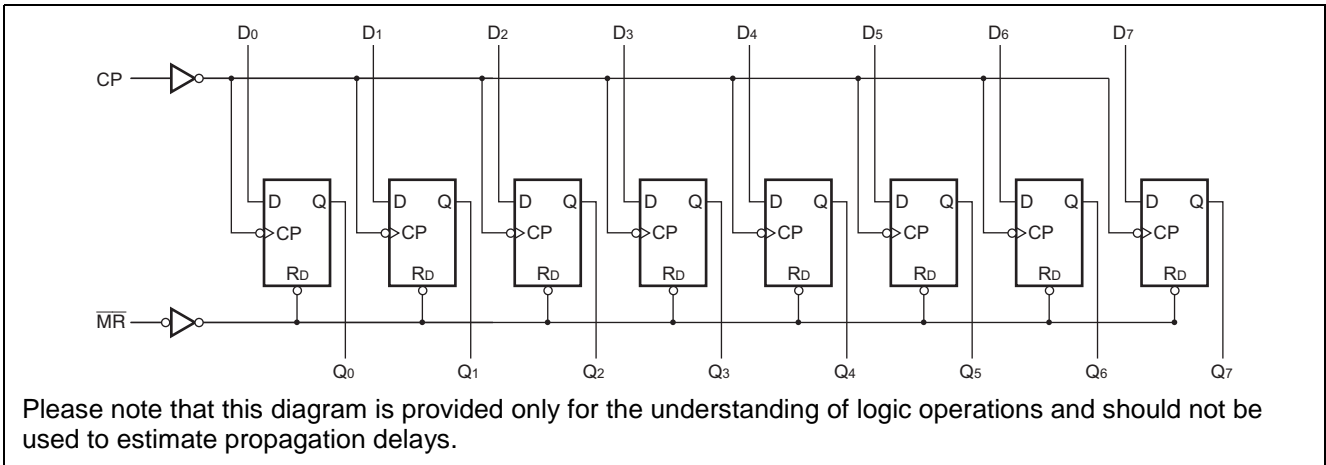
### Logic Symbol



### Pin Names

- D<sub>0</sub> – D<sub>7</sub> Data Inputs
- $\overline{MR}$  Master Reset
- CP Clock Pulse Input
- Q<sub>0</sub> – Q<sub>7</sub> Data Outputs

### Logic Diagram



### Mode Select-Truth Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	$D_n$	$Q_n$
Reset (Clear)	L	X	X	L
Load "1"	H		H	H
Load "0"	H		L	L

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial
- : Low-to-High Clock Transition

### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	$V_{CC}$	-0.5 to 7	V	
DC input diode current	$I_{IK}$	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	$V_I$	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	$I_{OK}$	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	$V_O$	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	$I_O$	$\pm 50$	mA	
DC $V_{CC}$ or ground current per output pin	$I_{CC}, I_{GND}$	$\pm 50$	mA	
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$	

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	$V_{CC}$	2 to 6	V	
Input and output voltage	$V_I, V_O$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to +85	$^{\circ}C$	
Input rise and fall time (except Schmitt inputs) $V_{IN}$ 30% to 70% $V_{CC}$	$t_r, t_f$	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5V$
				$V_{CC} = 5.5V$

**DC Characteristics**

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition				
			min.	typ.	max.	min.	max.						
Input Voltage	V <sub>IH</sub>	3.0	2.1	1.5	—	2.1	—	V	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V				
		4.5	3.15	2.25	—	3.15	—						
		5.5	3.85	2.75	—	3.85	—						
	V <sub>IL</sub>	3.0	—	1.50	0.9	—	0.9		V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V				
		4.5	—	2.25	1.35	—	1.35						
		5.5	—	2.75	1.65	—	1.65						
Output voltage	V <sub>OH</sub>	3.0	2.9	2.99	—	2.9	—	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OUT</sub> = -50 μA				
		4.5	4.4	4.49	—	4.4	—						
		5.5	5.4	5.49	—	5.4	—						
		3.0	2.58	—	—	2.48	—			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA			
		4.5	3.94	—	—	3.80	—				I <sub>OH</sub> = -24 mA		
		5.5	4.94	—	—	4.80	—				I <sub>OH</sub> = -24 mA		
	V <sub>OL</sub>	3.0	—	0.002	0.1	—	0.1		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OUT</sub> = 50 μA				
		4.5	—	0.001	0.1	—	0.1						
		5.5	—	0.001	0.1	—	0.1						
		3.0	—	—	0.32	—	0.37			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA			
		4.5	—	—	0.32	—	0.37				I <sub>OL</sub> = 24 mA		
		5.5	—	—	0.32	—	0.37				I <sub>OL</sub> = 24 mA		
		Input leakage current	I <sub>IN</sub>	5.5	—	—	±0.1			—	±1.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
		Dynamic output current*	I <sub>OLD</sub>	5.5	—	—	—			86	—	mA	V <sub>OLD</sub> = 1.1 V
I <sub>OHD</sub>	5.5		—	—	—	-75	—	mA	V <sub>OHD</sub> = 3.85 V				
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	8.0	—	80	μA	V <sub>IN</sub> = V <sub>CC</sub> or ground				

\*Maximum test duration 2.0 ms, one output loaded at a time.

**AC Characteristics**

Item	Symbol	V <sub>CC</sub> (V)*1	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f <sub>max</sub>	3.3	90	125	—	75	—	MHz
		5.0	140	175	—	125	—	
Propagation delay Clock to output	t <sub>PLH</sub>	3.3	1.0	7.0	12.5	1.0	14.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay Clock to output	t <sub>PHL</sub>	3.3	1.0	7.0	13.0	1.0	14.5	ns
		5.0	1.0	5.0	10.0	1.0	11.0	
Propagation delay MR to output	t <sub>PHL</sub>	3.3	1.0	7.0	13.0	1.0	14.0	ns
		5.0	1.0	5.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements

Item	Symbol	V <sub>CC</sub> (V)*1	Ta = +25°C C <sub>L</sub> = 50 pF		Ta = -40°C to +85°C C <sub>L</sub> = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW Data to CP	t <sub>su</sub>	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
Hold time, HIGH or LOW Data to CP	t <sub>h</sub>	3.3	-2.0	0.0	0.0	ns
		5.0	-1.0	1.0	1.0	
Clock pulse width HIGH or LOW	t <sub>w</sub>	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
MR Pulse width HIGH or LOW	t <sub>w</sub>	3.3	2.0	5.5	6.0	ns
		5.0	1.5	4.0	4.5	
Recovery time MR to CP	t <sub>rec</sub>	3.3	1.5	3.5	4.5	ns
		5.0	1.0	2.0	3.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

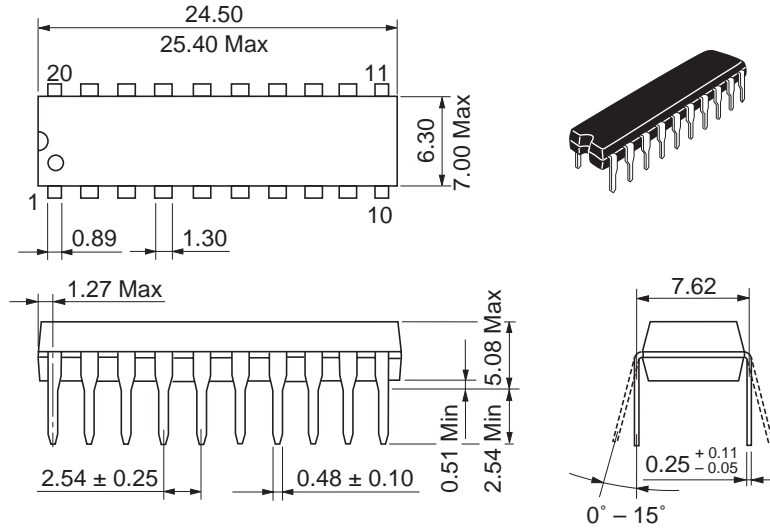
## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C <sub>IN</sub>	4.5	pF	V <sub>CC</sub> = 5.5 V
Power dissipation capacitance	C <sub>PD</sub>	50.0	pF	V <sub>CC</sub> = 5.0 V

Package Dimensions

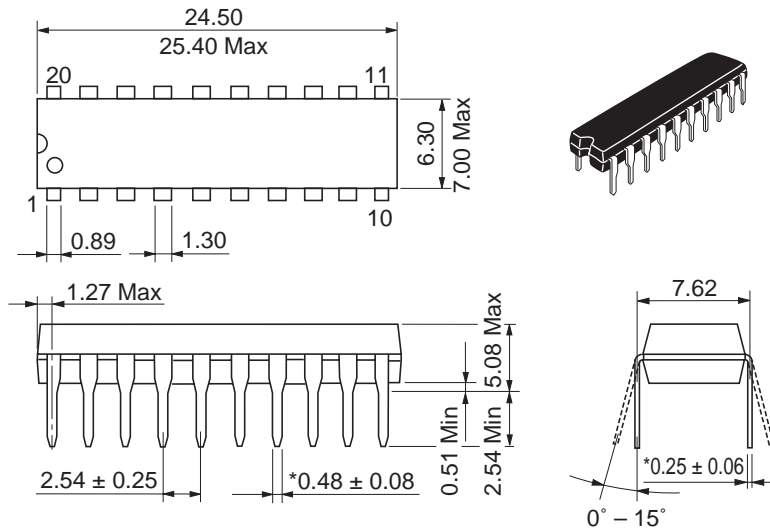
As of January, 2003

Unit: mm



Package Code	DP-20N
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

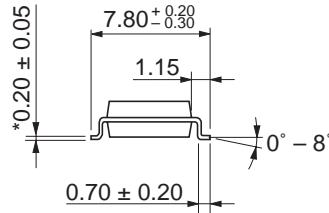
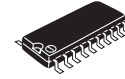
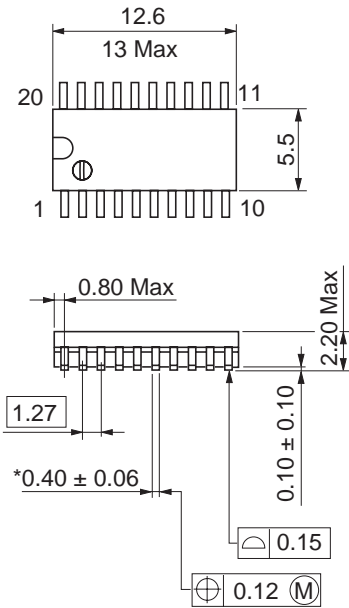
Unit: mm



\*Ni/Pd/AU Plating

Package Code	DP-20NEV
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

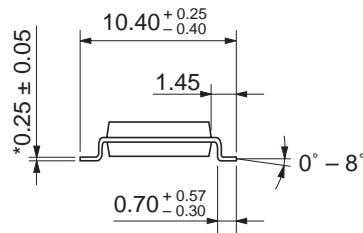
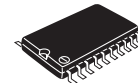
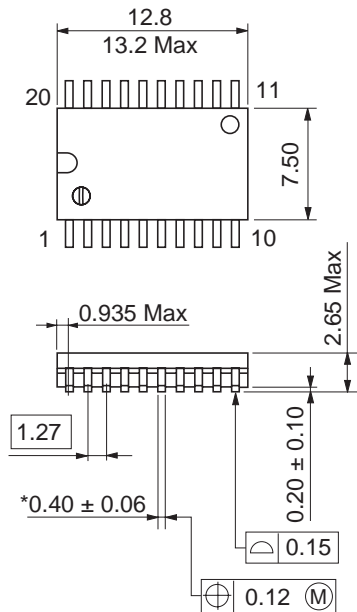
As of January, 2003  
Unit: mm



Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

\*Ni/Pd/Au plating

As of January, 2003  
Unit: mm



Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

\*Ni/Pd/Au plating

## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

---

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
  2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
  3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
  4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
  5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
  6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
  8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
- 



### RENESAS SALES OFFICES

<http://www.renesas.com>

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**  
Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**  
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**  
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**  
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**  
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001