HARRIS SEMICONDUCTOR

HGTP3N60C3D, HGT1S3N60C3D, HGT1S3N60C3DS

6A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

May 1996

Features

- 6A, 600V at $T_C = +25^oC$
- 600V Switching SOA Capability
- Typical Fall Time - 130ns at $T_J = +150^oC$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTP3N60C3D, HGT1S3N60C3D, and HGT1S3N60C3DS are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between $+25^oC$ and $+150^oC$. The IGBT used is the development type TA49113. The diode used in anti-parallel with the IGBT is the development type TA49055.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

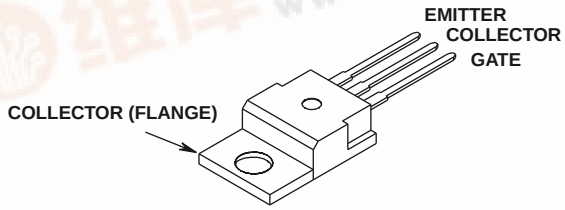
PART NUMBER	PACKAGE	BRAND
HGTP3N60C3D	TO-220AB	G3N60C3D
HGT1S3N60C3D	TO-262AA	G3N60C3D
HGT1S3N60C3DS	TO-263AB	G3N60C3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. HGT1S3N60C3DS9A.

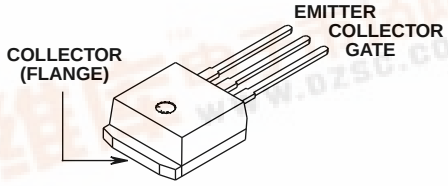
Formerly Developmental Type TA49119.

Packaging

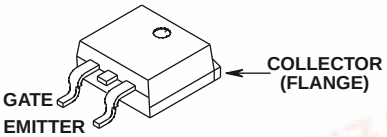
JEDEC TO-220AB



JEDEC TO-262AA

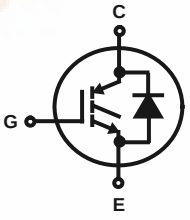


JEDEC TO-263AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP3N60C3D, HGT1S3N60C3D HGT1S3N60C3DS	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = +25^oC$	I_{C25}	6	A
At $T_C = +110^oC$	I_{C110}	3	A
Collector Current Pulsed (Note 1)	I_{CM}	24	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = +150^oC$, Fig. 14	SSOA	18A at 480V	
Power Dissipation Total at $T_C = +25^oC$	P_D	33	W
Power Dissipation Derating $T_C > +25^oC$		0.27	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +150	^oC
Maximum Lead Temperature for Soldering	T_L	260	^oC
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$, Fig 6	t_{SC}	8	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = +125^oC$, $R_{GE} = 82\Omega$.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	250	μA
		$V_{CE} = BV_{CES}$	$T_C = +150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.65	2.0	V
			$T_C = +150^oC$	-	1.85	2.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	5.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 25V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = +150^oC$, $R_G = 82\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)}$=480V	18	-	-	A
			$V_{CE(PK)}$=600V	2	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	IC = IC110, VCE = 0.5 BVCES	$V_{GE} = 15V$	-	10.8	13.5	nC
			$V_{GE} = 20V$	-	13.8	17.3	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 82\Omega$, $L = 1mH$		-	5	-	ns
Current Rise Time	t_{RI}			-	10	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	325	400	ns
Current Fall Time	t_{FI}			-	130	275	ns
Turn-On Energy	E_{ON}			-	85	-	μJ
Turn-Off Energy (Note 1)	E_{OFF}			-	245	-	μJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 3A$		-	2.0	2.5	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 3A$, $dI_{EC}/dt = 200A/\mu s$		-	22	28	ns
		$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$		-	17	22	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	3.75	$^oC/W$
		Diode		-	-	3.0	$^oC/W$

NOTE:

1. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTP3N60C3D, HGT1S3N60C3D, and HGT1S3N60C3DS were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951

Typical Performance Curves

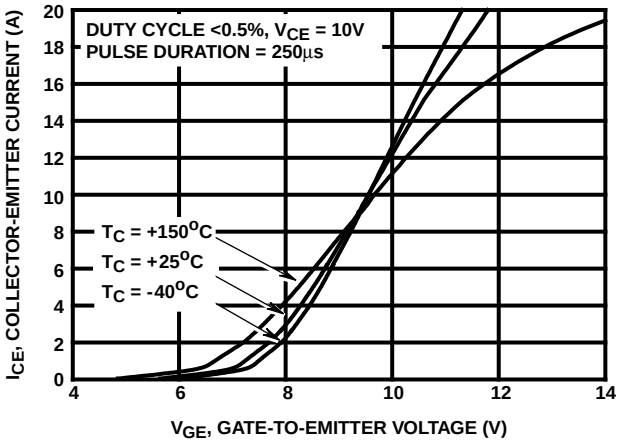


FIGURE 1. TRANSFER CHARACTERISTICS

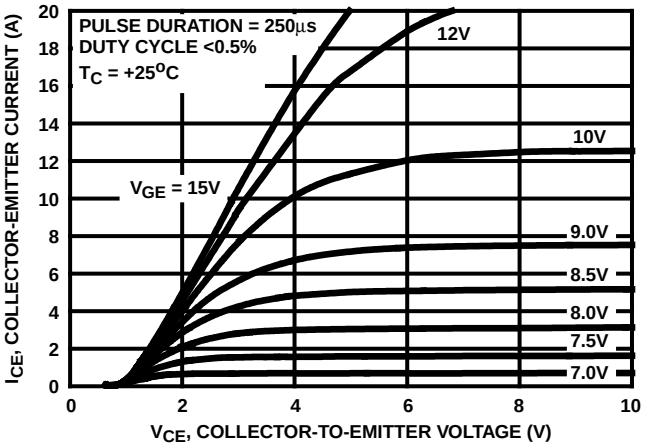


FIGURE 2. SATURATION CHARACTERISTICS

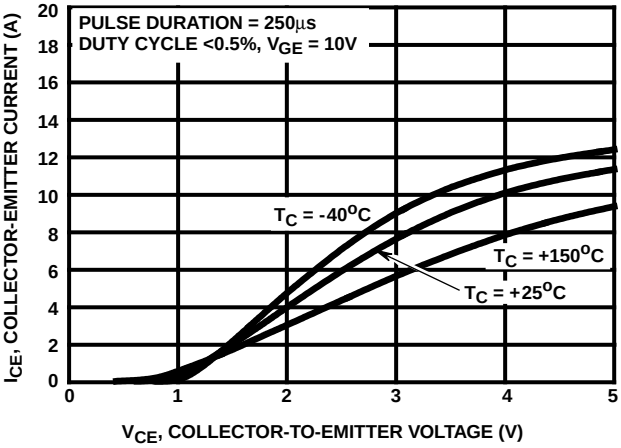


FIGURE 3. COLLECTOR-EMITTER ON - STATE VOLTAGE

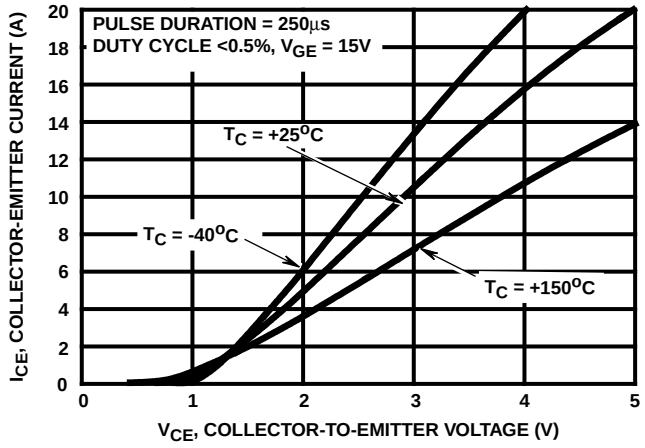


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

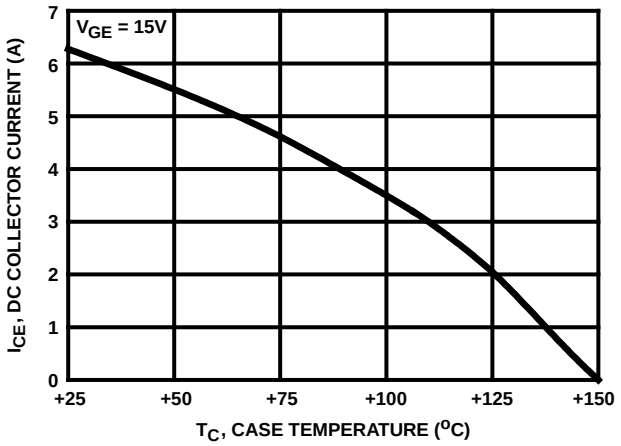


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

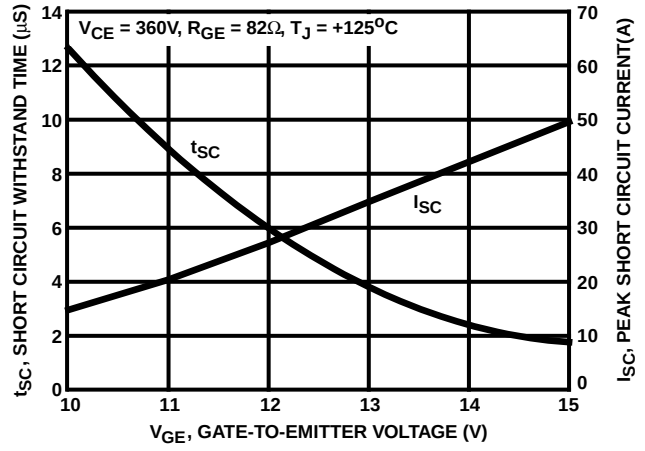


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

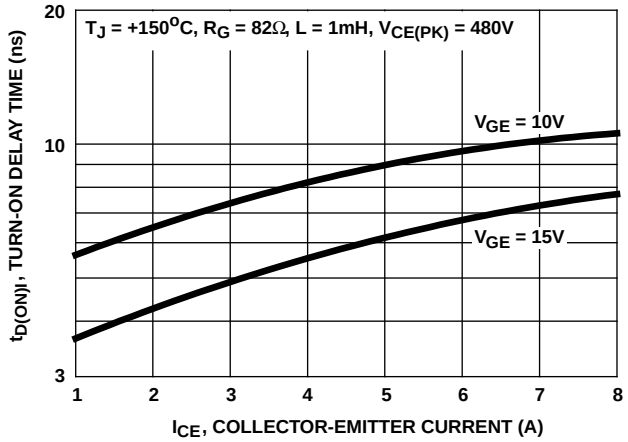


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

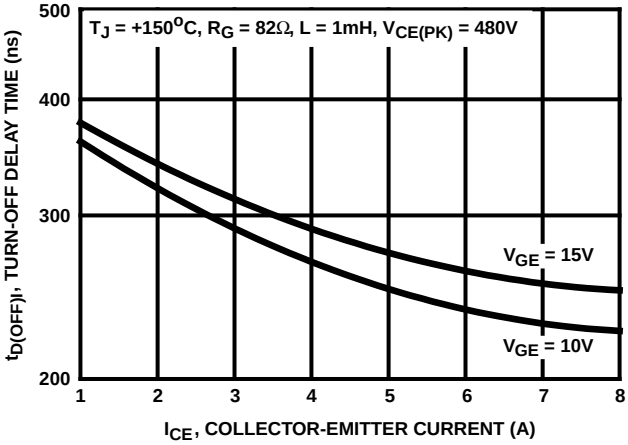


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

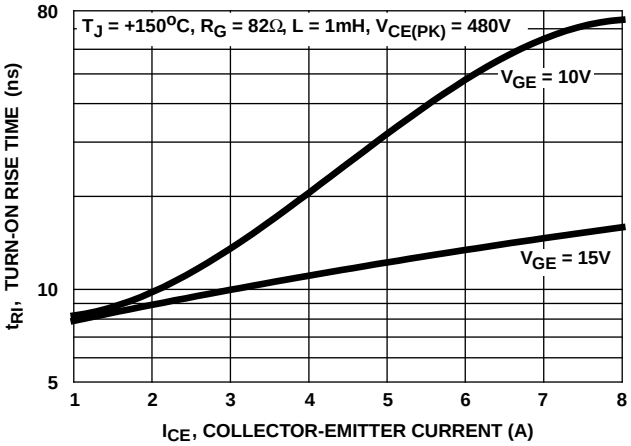


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

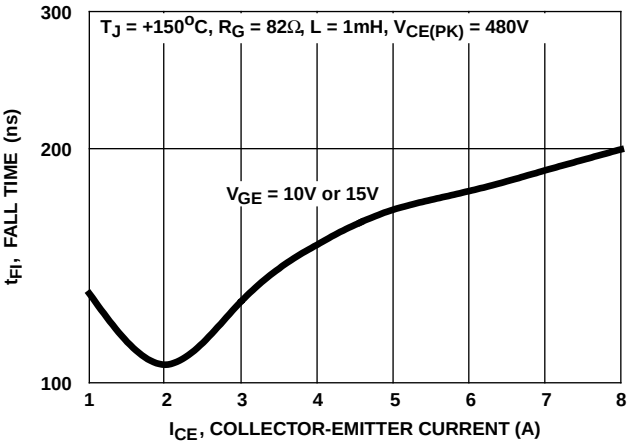


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

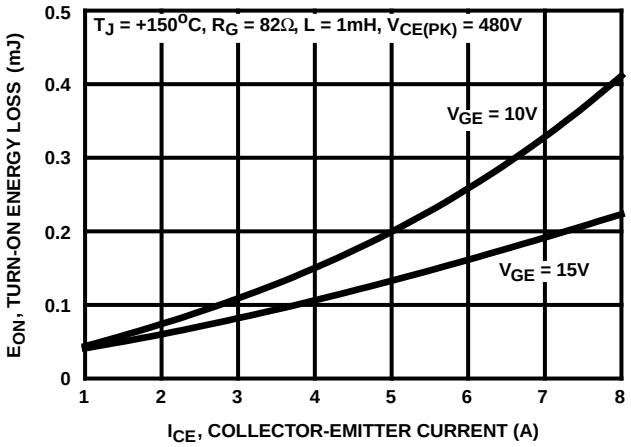


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

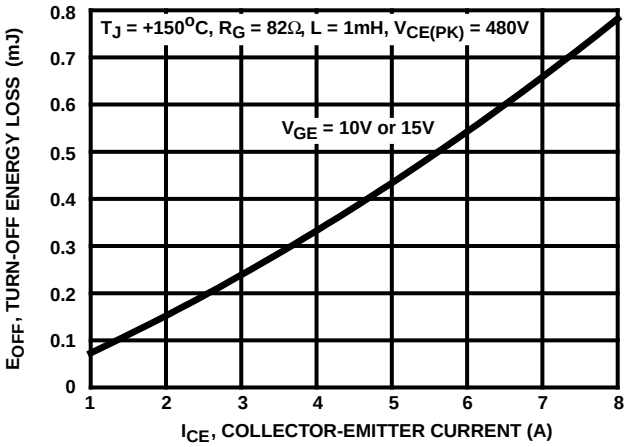


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

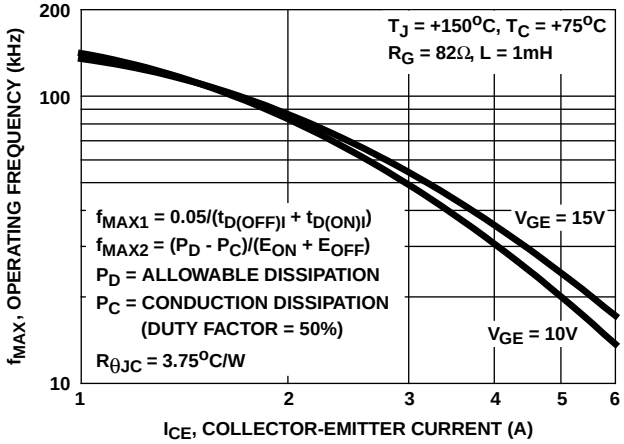


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

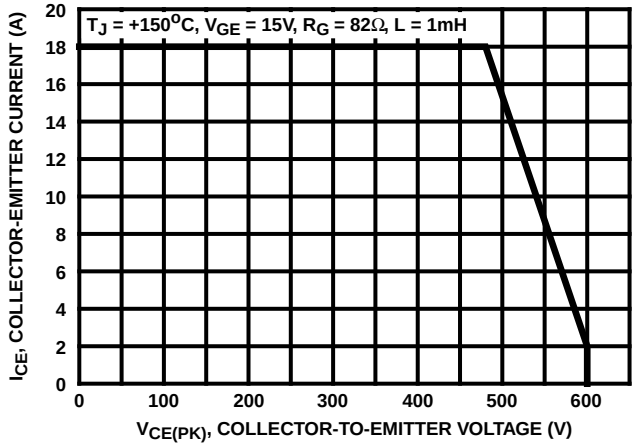


FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

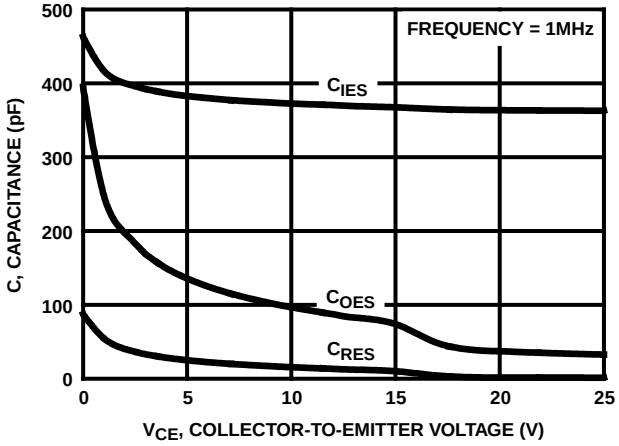


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

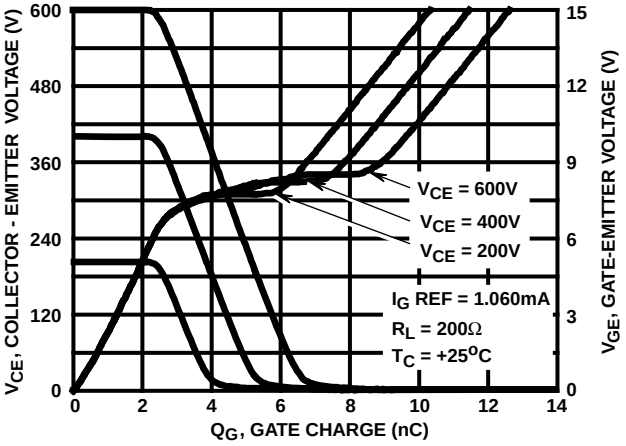


FIGURE 16. GATE CHARGE WAVEFORMS

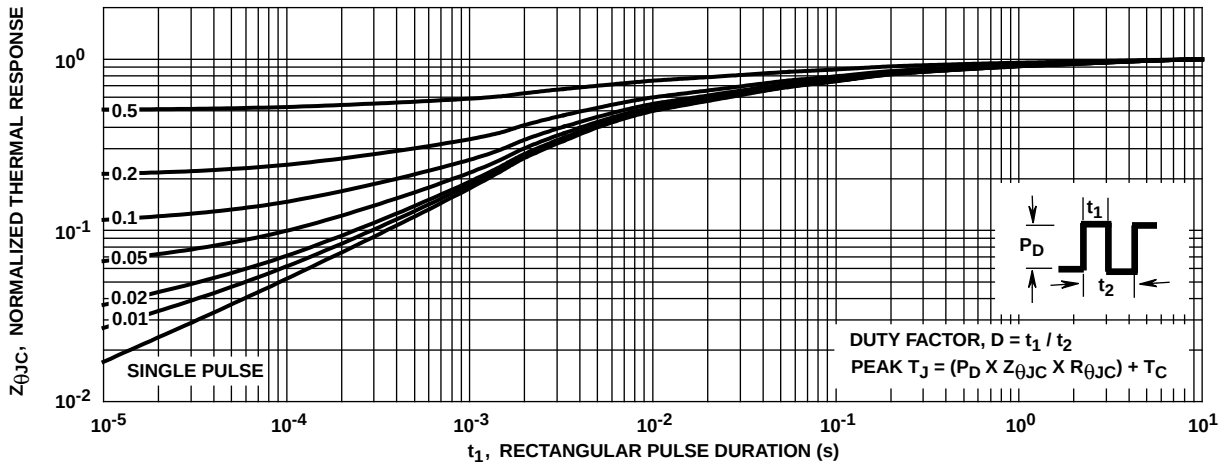


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Typical Performance Curves (Continued)

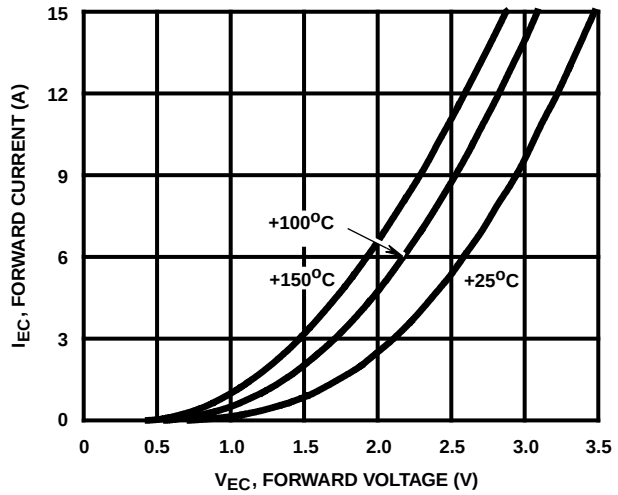


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

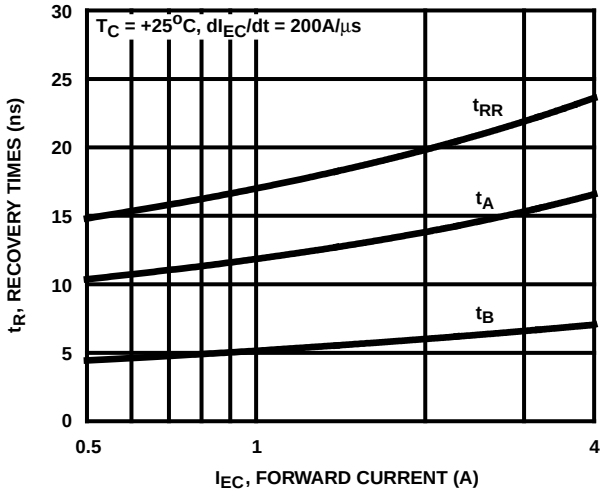


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveforms

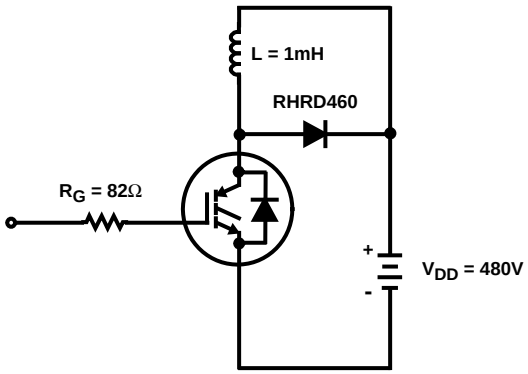


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

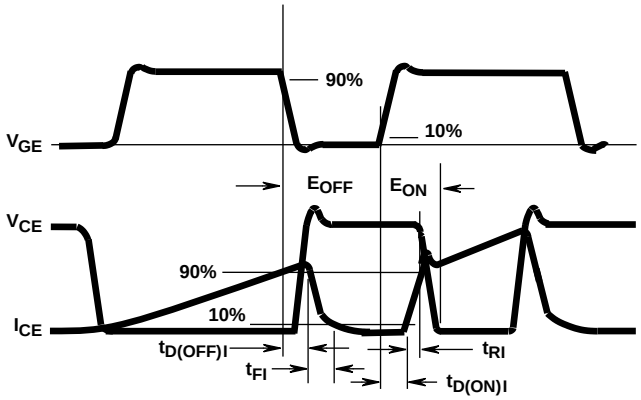


FIGURE 21. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBTs

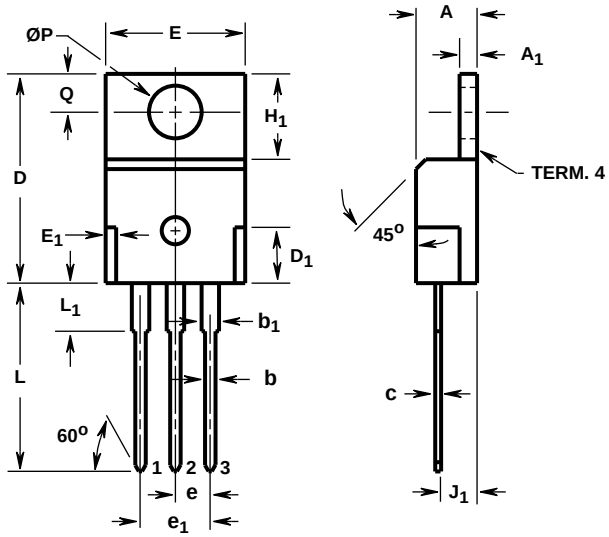
Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †ECCOSORBD LD26™ or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD 1 - GATE
LEAD 2 - COLLECTOR
LEAD 3 - EMITTER
TERM. 4 - COLLECTOR

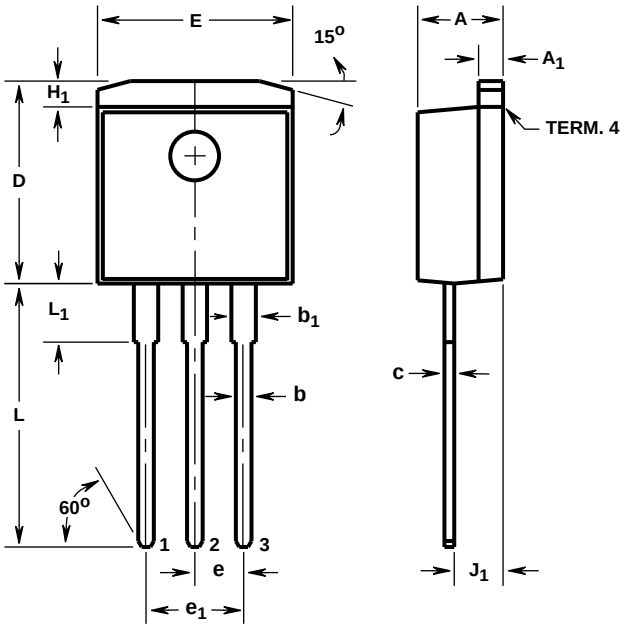
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-262AA

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



LEAD 1 - GATE

LEAD 2 - COLLECTOR

LEAD 3 - EMITTER

TERM. 4 - COLLECTOR

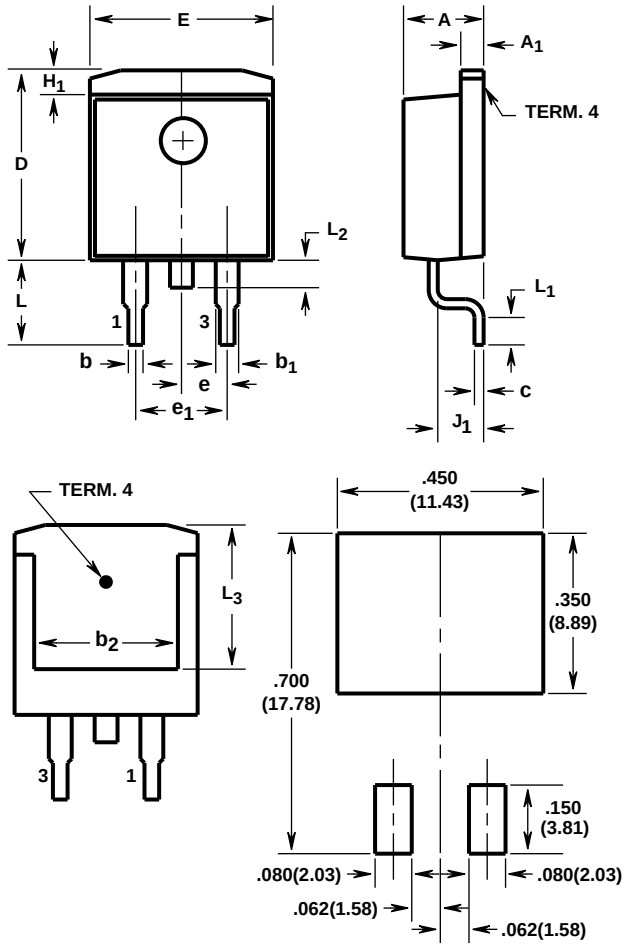
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

LEAD 1 - GATE

LEAD 3 - EMITTER

TERM. 4 - COLLECTOR

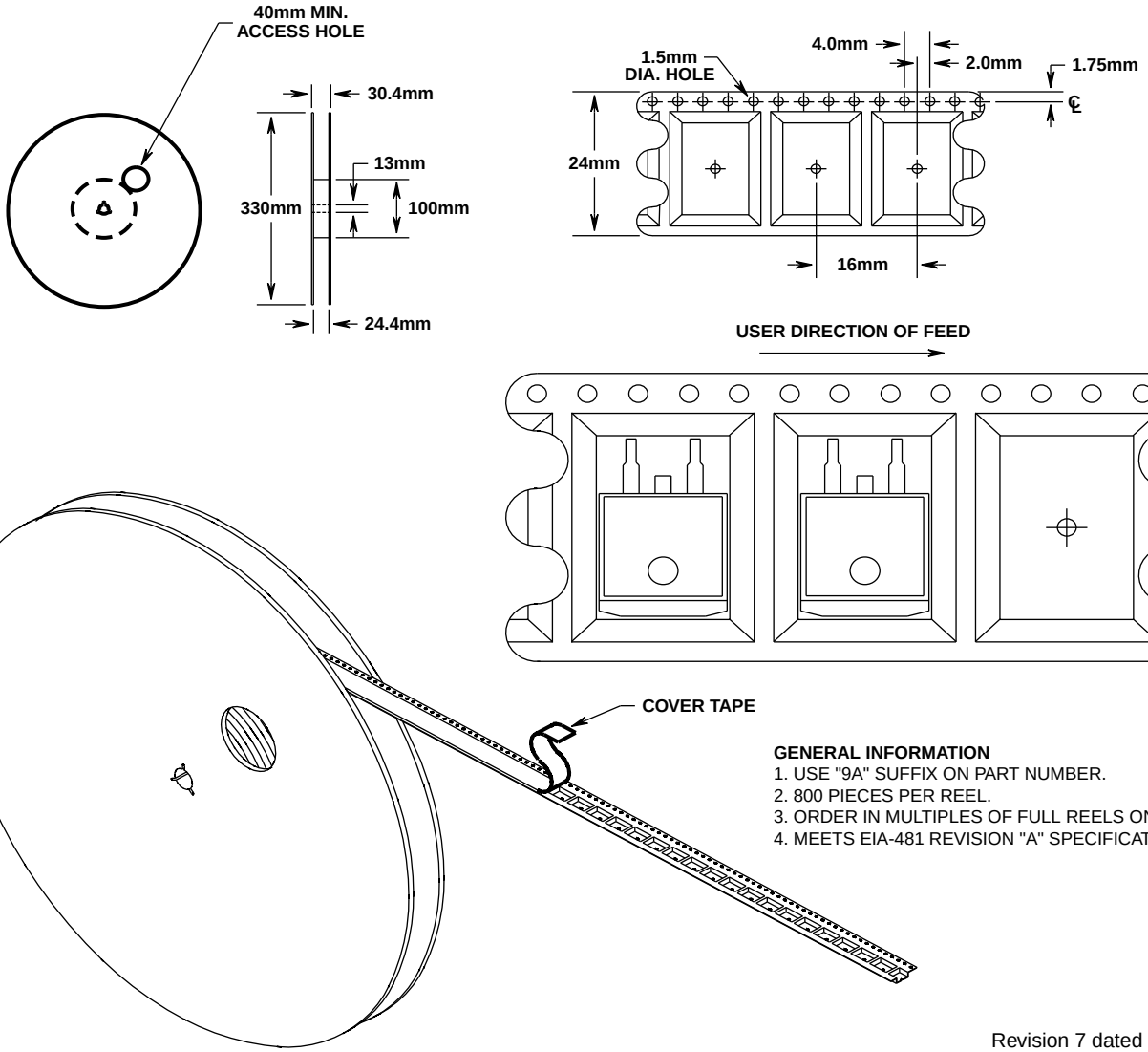
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 7 dated 10-95

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