



# HMC223MS8

## GaAS MMIC MSOP8 T/R SWITCH 4.5 - 6 GHz

FEBRUARY 2001

v01.0300

### Features

- INDUSTRY FIRST LOW COST 4.5-6 GHz SWITCH
- ULTRA SMALL PACKAGE: MSOP8
- HIGH INPUT P1dB: +33 dBm
- SINGLE POSITIVE SUPPLY: +3 TO +8V

### General Description

The HMC223MS8 is a low-cost SPDT switch in an 8-lead MSOP package for use in transmit-receive applications. The device can control signals from 4.5 to 6 GHz and is especially suited for 5.2 GHz UNII and 5.8 GHz ISM applications with only 1.2 dB loss. The design provides exceptional power handling performance; input P1dB = +33dBm at 5 Volt bias. RF1 or RF2 is a reflective short when "Off". On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families. No DC blocking capacitors are required on RF I/O ports. HMC223MS8 is especially suited for PCMCIA wireless LAN applications.



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SWITCHES

SPDT

SMT

### Guaranteed Performance, Vdd = +5 Vdc, 50 Ohm System, -40 to +85 deg C

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	4.5 - 6.0 GHz		1.2	1.7	dB
	5.1 - 5.4 GHz		1.2	1.6	dB
	5.4 - 5.9 GHz		1.3	1.7	dB
Isolation	4.5 - 6.0 GHz	15	25		dB
	5.1 - 5.4 GHz	22	26		dB
	5.4 - 5.9 GHz	16	20		dB
Return Loss	RF Common	4.5 - 6.0 GHz	10	13	dB
		5.1 - 5.9 GHz	11	15	dB
	RF1 & RF2	4.5 - 6.0 GHz	10	13	dB
		5.1 - 5.9 GHz	12	16	dB
Input Power for 1dB Compression	0/3V Control	4.5 - 6.0 GHz	27	31	dBm
	0/5V Control	4.5 - 6.0 GHz	29	33	dBm
Input Third Order Intercept	0/3V Control	4.5 - 6.0 GHz	30	34	dBm
	0/5V Control	4.5 - 6.0 GHz	32	36	dBm
Switching Characteristics	tRISE, tFALL (10/90% RF)	4.5 - 6.0 GHz		10	nS
	tON, tOFF (50% CTL to 10/90% RF)			25	nS

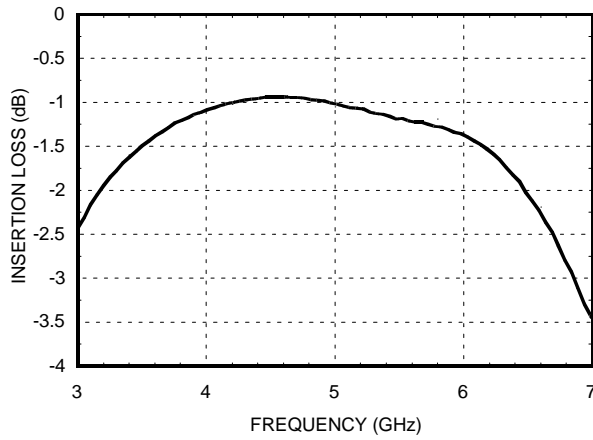


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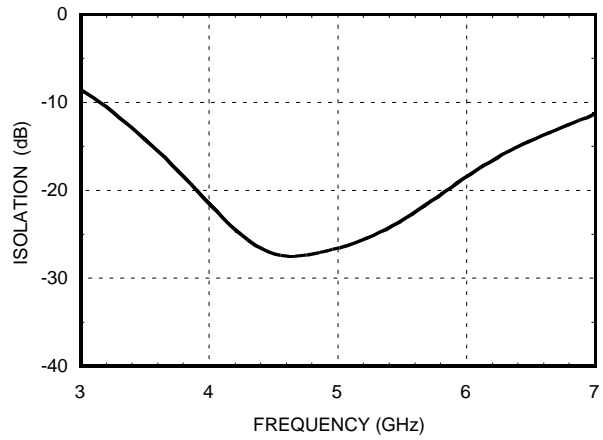
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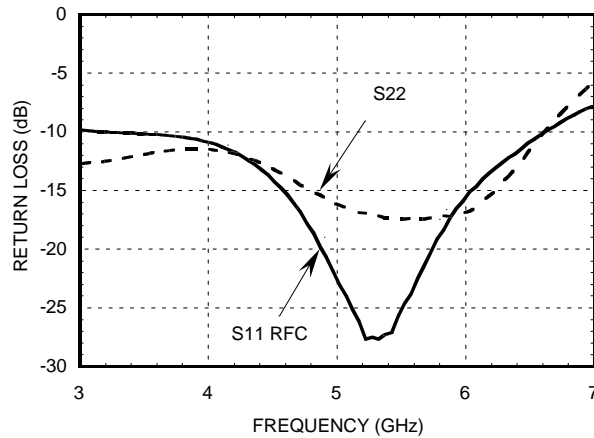
### Insertion Loss



### Isolation



### Return Loss

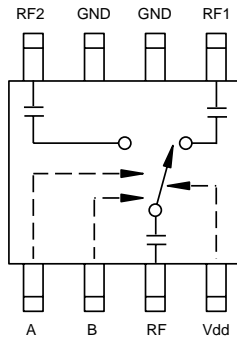


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### Functional Diagram



### Truth Table

\*Control Input Voltage Tolerances are  $\pm 0.2$  Vdc

Bias Vdd (Vdc)	Control Input *		Bias Current Ivdd ( $\mu$ A)	Control Current Ia ( $\mu$ A)	Control Current Ib ( $\mu$ A)	Signal Path State	
	A (Vdc)	B (Vdc)				RF to RF1	RF to RF2
3	0	0	10	-5	-5	OFF	OFF
3	0	Vdd	10	-10	0	ON	OFF
3	Vdd	0	10	0	-10	OFF	ON
5	0	0	45	-22	-23	OFF	OFF
5	0	Vdd	45	-5	-40	ON	OFF
5	Vdd	0	45	-40	-5	OFF	ON

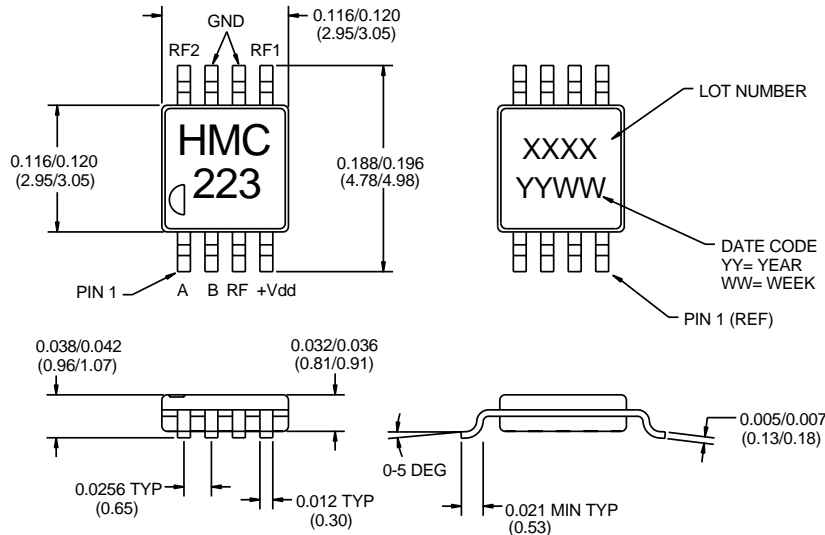
### Absolute Maximum Ratings

Bias Voltage Range (Vdd)	-0.2 to +12 Vdc
Control Voltage Range (A & B)	-0.2 to +Vdd Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C

Caution: Do not operate in 1dB compression at power levels above +33 dBm and do not 'hot switch' power levels greater than +23dBm ( $V_{dd} = +5Vdc$ ).

DC blocks are not required at ports RFC, RF1 and RF2.

### Outline



- 1) MATERIAL:
  - A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
  - B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)

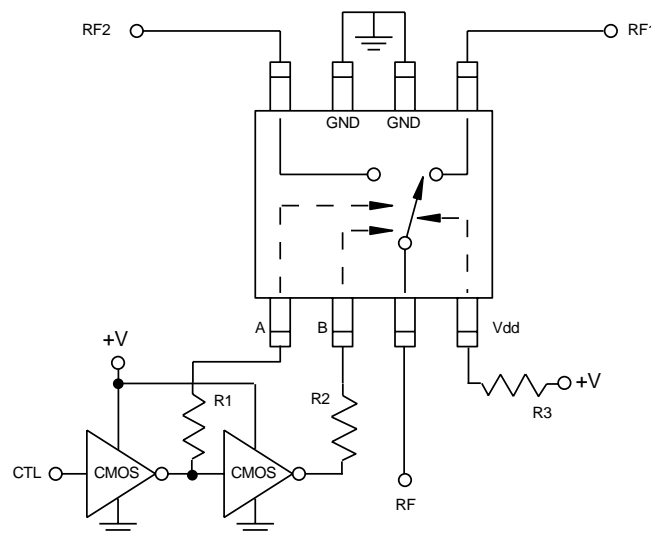


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### Typical Application Circuit



**Notes:**

1. Control inputs A and B can be driven directly with CMOS logic (HC) with V of 3 to 8 Volts applied to the CMOS logic gates and to pin 4 of the RF switch.
2. Set V to 5 Volts and use HCT series logic to provide a TTL driver interface.
3. Highest RF signal power capability is achieved with V set to +10V. However, the switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.
4. RF ByPass: Do not use RF bypass capacitors on Vdd, A or B ports. Resistors R1, R2, R3 = 100 Ohms should be placed close to the Vdd, A and B ports. Use resistor size 0402 to minimize parasitic inductances and capacitances.
5. DC Blocking capacitors are not required for each RF port.
6. Evaluation PCB available.

**See Page 8 - 4 for Layout Guidelines Application Note.**

