Hittite MICROWAVE CORPORATION

RoHS EARTH FRIENDLY

Designer's Kit Available

v02.0705

HMC305LP4 / 305LP4E

0.5 dB LSB GaAs MMIC 5-BIT SERIAL CONTROL DIGITAL ATTENUATOR, 0.7 - 3.8 GHz

Typical Applications

The HMC305LP4 / HMC305LP4E is ideal for:

- Cellular/3G Infrastructure
- Fixed Wireless, WiMax & WiBro
- Test Instrumentation

Features

0.5 dB LSB Steps to 15.5 dB

CMOS Compatible Serial Data Interface

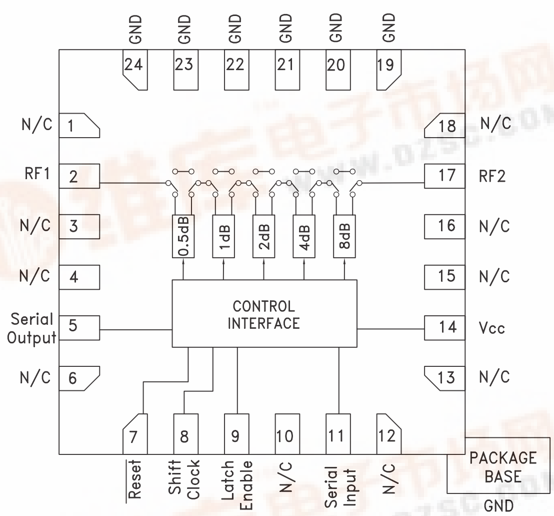
SPI Compatible Serial Output

+/- 0.3 dB Typical Bit Error

QFN Leadless SMT Package, 16mm²

Included in the HMC-DK004 Designer's Kit

Functional Diagram



General Description

The HMC305LP4 & HMC305LP4E are broadband 5-bit positive control GaAs IC digital attenuators with CMOS compatible serial-to-parallel drivers packaged in leadless QFN 4 x 4 mm SMT packages. Covering 0.7 to 3.8 GHz, the insertion loss is typically less than 1.5 to 2 dB. The attenuator bit values are 0.5 (LSB), 1, 2, 4, and 8 dB for a total attenuation of 15.5 dB. Attenuation accuracy is excellent at ± 0.25 dB typical with an IIP3 of up to +52 dBm. Five bit serial control words are used to select each attenuation state. A single Vcc bias of +3V to +5V applied through an external 5k Ohm resistor is required.

Electrical Specifications, T_A = +25° C, Vcc = +3V to +5V

Parameter		Frequency	Min.	Typical	Max.	Units
Insertion Loss		0.7 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 3.8 GHz		1.2 1.5 1.8 2.0	1.5 2.0 2.3 2.5	dB dB dB dB
Attenuation Range		0.7 - 3.8 GHz		15.5		dB
Return Loss (RF1 & RF2, All Atten. States)		0.7 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 3.8 GHz		17 18 19 15		dB dB dB dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States		0.7 - 0.9 GHz 0.9 - 2.2 GHz 2.2 - 3.8 GHz		± (0.5 +5% of Atten. Setting) Max ± (0.3 +4% of Atten. Setting) Max ± (0.5 +5% of Atten. Setting) Max		dB dB dB
Input Power for 0.1 dB Compression	Vcc = 5V Vcc = 3V	0.7 - 3.8 GHz		25 23		dBm dBm
Input Third Order Intercept Point (Two-tone Input Power = 0 dBm Each Tone)	Vcc = 5V Vcc = 3V	0.7 - 3.8 GHz		52 48		dBm dBm
Switching Characteristics t_{RISE}, t_{FALL} (10/90% RF) t_{ON}, t_{OFF} (Latch Enable to 10/90% RF)		0.7 - 3.8 GHz		750 830		ns ns

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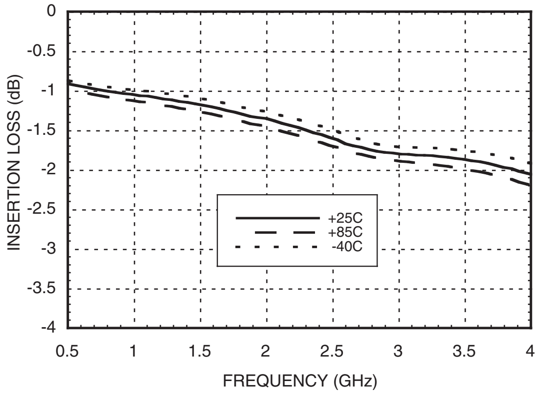
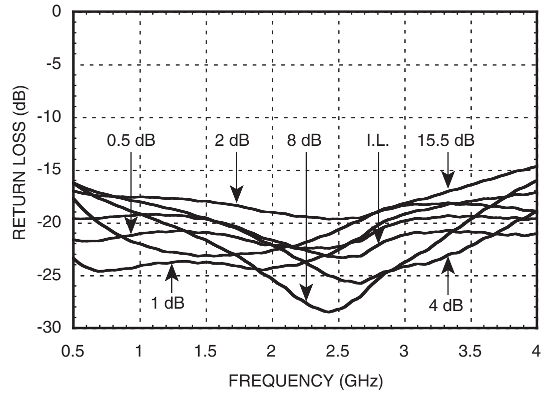
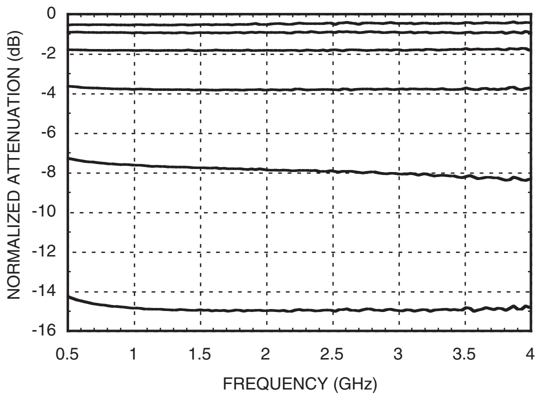
Insertion Loss



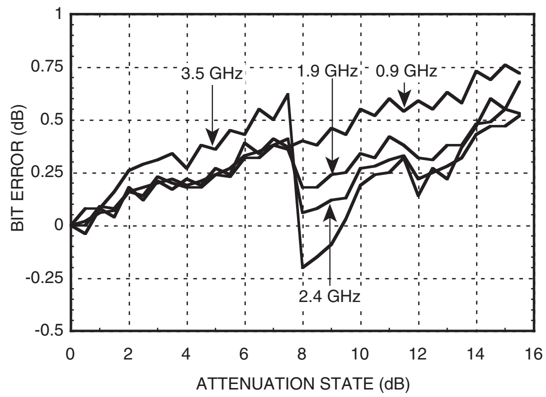
Return Loss RF1, RF2
(Only Major States are Shown)



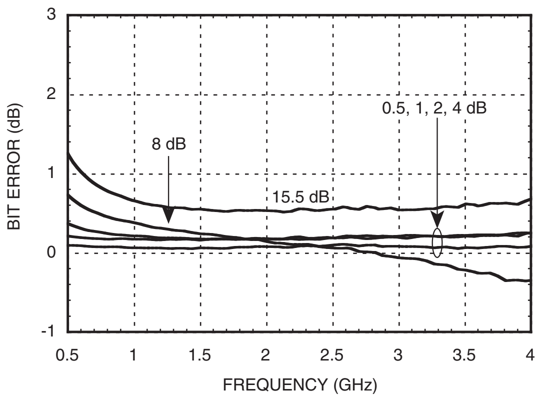
Normalized Attenuation
(Only Major States are Shown)



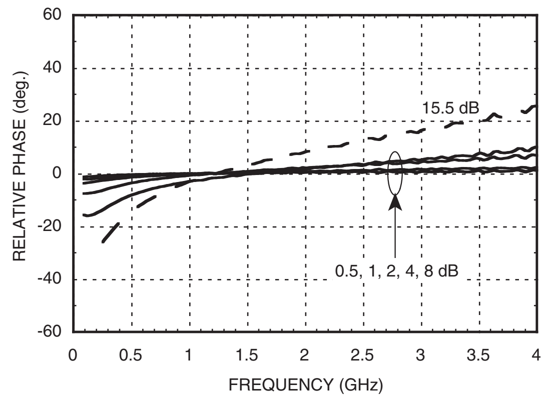
Bit Error vs. Attenuation State



Bit Error vs. Frequency
(Only Major States are Shown)



Relative Phase vs. Frequency
(Only Major States are Shown)



Note: All Data Typical Over Voltage (+3V to +5V) & Temperature (-40 to +85 deg. C.).

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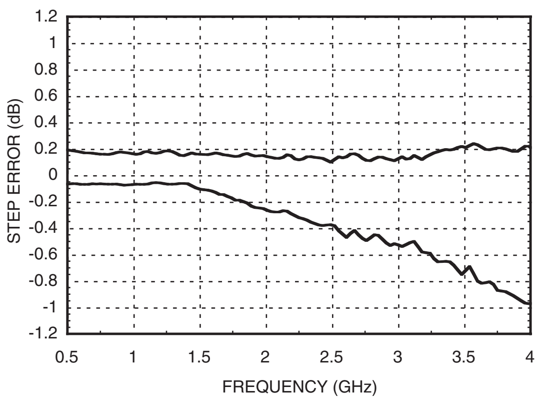
Worst Case Step Error Between Successive Attenuation States



CMOS Control Voltages

State	Vcc = +5V	Vcc = +3V
Low	0 to 1.3V	0 to 0.7V
High	3.5 to 5.0V	2.3 to 3.0V

Serial Input Truth Table

Latch Enable	Shift Clock	$\overline{\text{Reset}}$	Function
X	X	L	Shift register cleared
X	↑	H	Shift register clocked
↑	X	H	Contents of shift register transferrred to Digital Attenuator

Timing

Parameter	Symbol	Vcc = +5V		Vcc = +3V		Units
		Min.	Max.	Min.	Max.	
Serial Input Setup Time	ts	20	-	100	-	ns
Hold time from Serial Input to Shift Clock	th	0	-	5	-	ns
Setup time from Shift Clock to Latch Enable	tlsup	40	-	100	-	ns
Propagation delay, Latch Enable to C0.5 through C8	tpd	-	30	-	70	ns
Setup time from $\overline{\text{Reset}}$ to Shift Clock	-	20	-	50	-	ns
Clock Frequency (1/tclk)	fclk	-	30	-	10	MHz

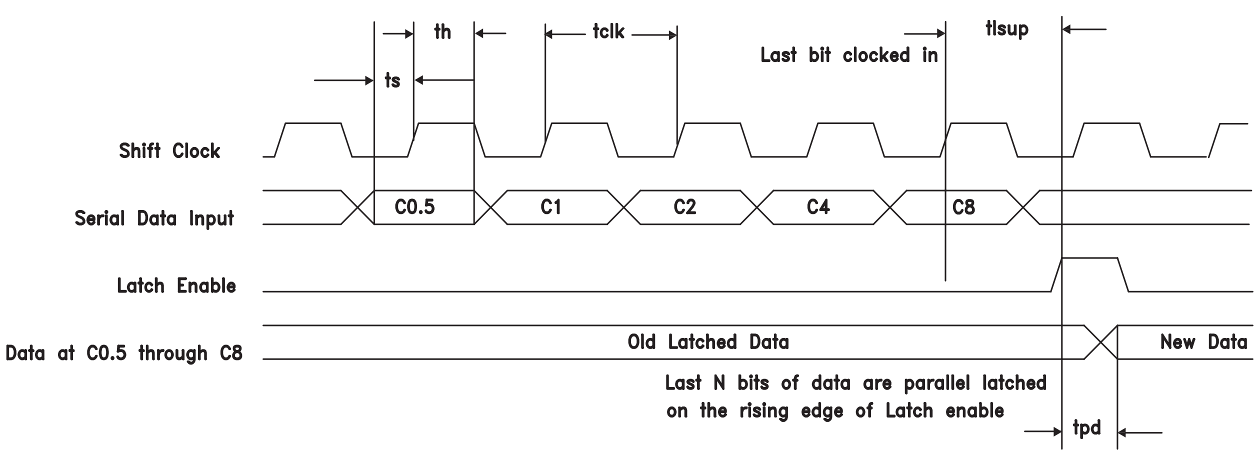
Truth Table

Serial Control Input					Attenuation Setting RF1 - RF2
C 0.5	C 1	C 2	C 4	C 8	
High	High	High	High	High	Reference I.L.
Low	High	High	High	High	0.5 dB
High	Low	High	High	High	1 dB
High	High	Low	High	High	2 dB
High	High	High	Low	High	4 dB
High	High	High	High	Low	8 dB
Low	Low	Low	Low	Low	15.5 dB Max. Atten.

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

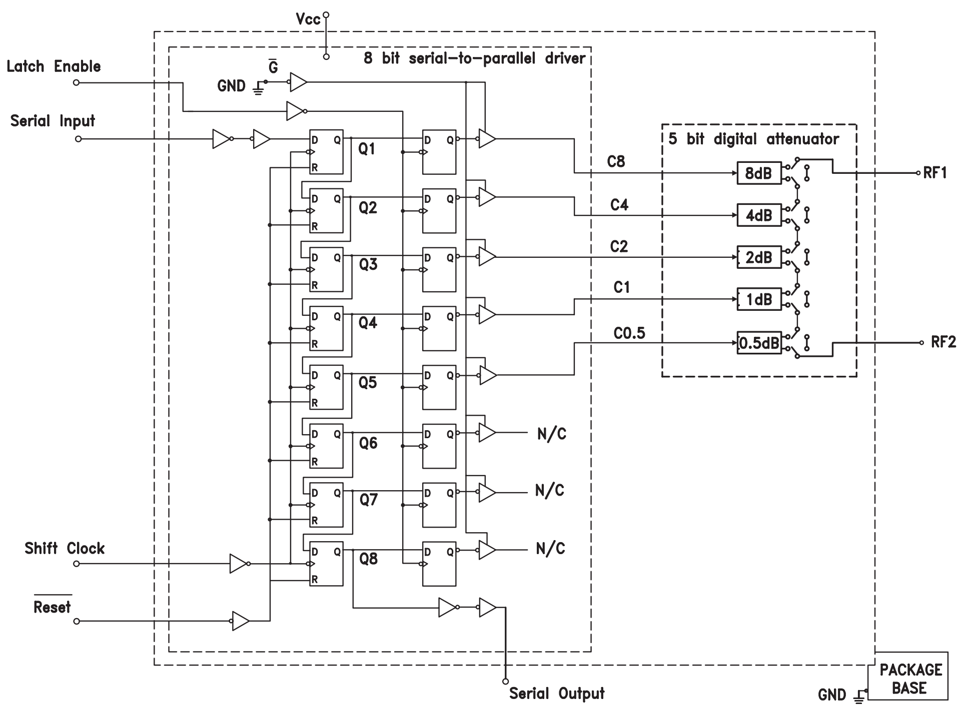
Timing Diagram

Serial data is shifted in on the rising edge of the Shift Clock, LSB first, and is latched on the rising edge of Latch Enable.

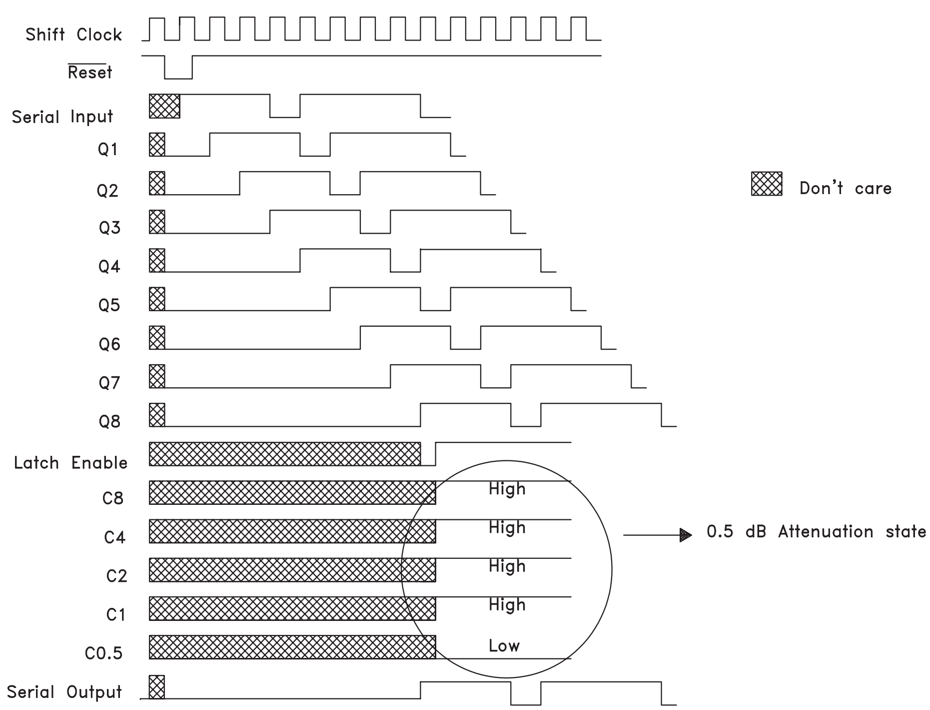


0.5 dB LSB GaAs MMIC 5-BIT SERIAL CONTROL DIGITAL ATTENUATOR, 0.7 - 3.8 GHz

Logic / Functional Diagram



Programming Example to Select 0.5 dB Attenuation State



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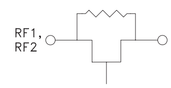
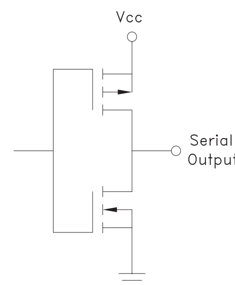
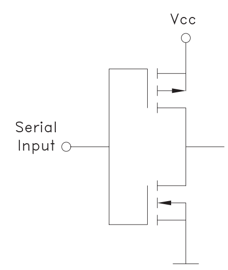
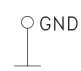
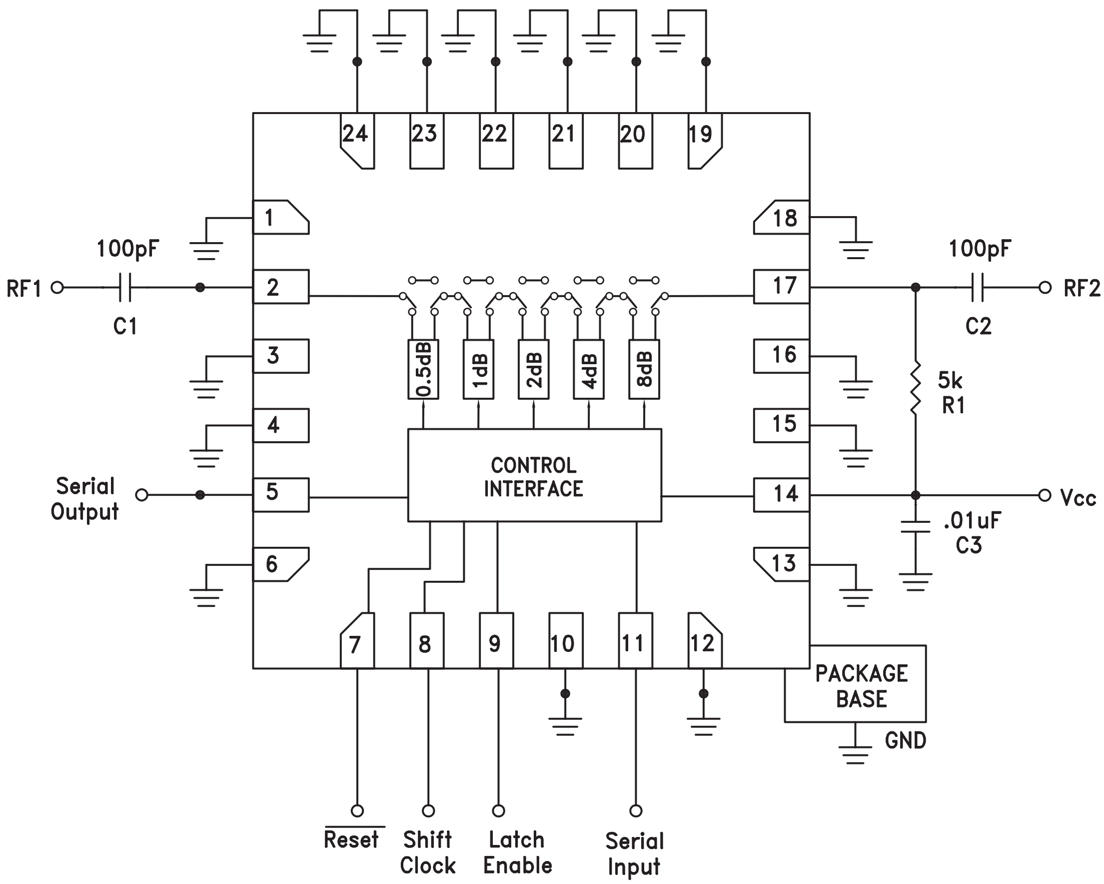
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6, 10, 12, 13, 15, 16, 18	N/C	These pins should be connected to PCB RF ground to maximize performance.	
2, 17	RF1, RF2	This pin is DC coupled and matched to 50 Ohms Blocking capacitors are required. Select value based on lowest frequency of operation.	
5	Serial Output	Serial data output. Serial input data delayed by 8 clock cycles	
7	$\overline{\text{Reset}}$	See truth table, control voltage table and timing diagram.	
8	Shift Clock		
9	Latch Enable		
11	Serial Input		
14	Vcc	Supply Voltage.	
19 - 24	GND	Package bottom has an exposed metal paddle that must also be connected to RF/DC Ground.	

Application Circuit



DC blocking capacitors C1 & C2 are required on RF1 & RF2. Choose C1 = C2 = 100 ~ 300 pF to allow lowest customer specific frequency to pass with minimal loss. R1 = 5k Ohm is required to supply voltage to the circuit through either PIN 2 or PIN 17.

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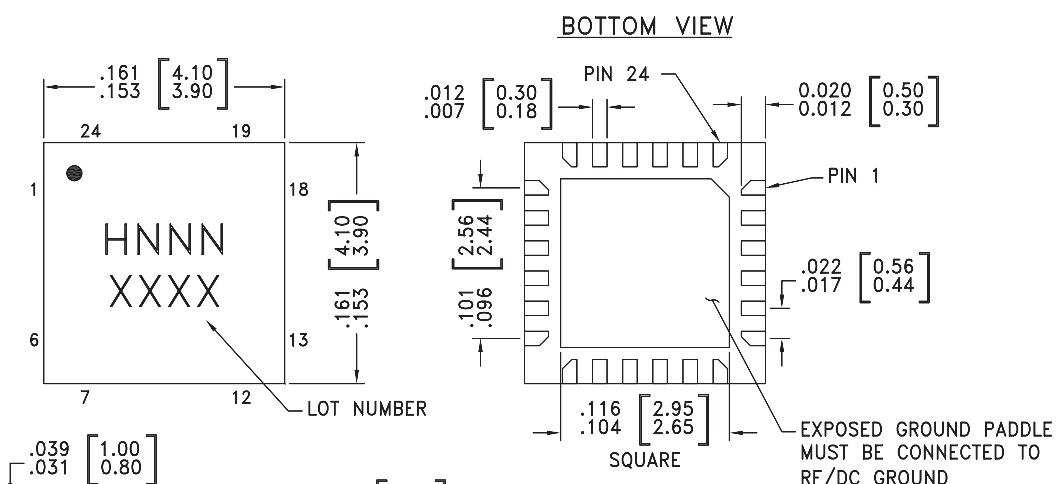
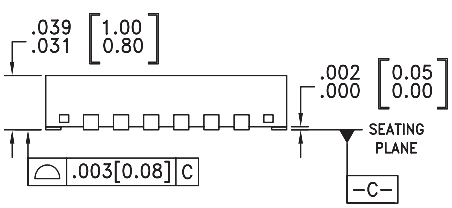
Absolute Maximum Ratings

Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input)	-1.5 to (Vcc + 1.5) Vdc
Digital Outputs (Serial Output)	-0.5 to (Vcc + 0.5)Vcc
DC Current on Serial Output	±35mA
Bias Voltage (Vcc)	+7.0 Vdc
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
RF Input Power (0.7 - 3.8 GHz)	+26 dBm
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC305LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H305 XXXX
HMC305LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H305 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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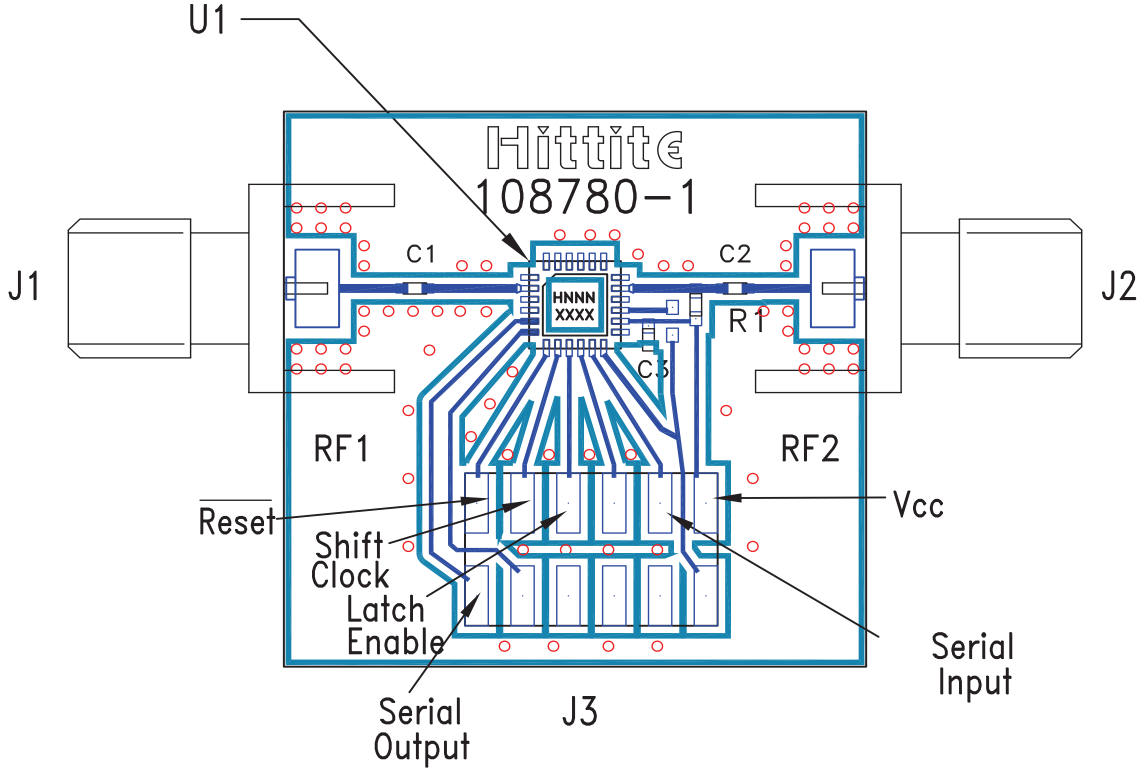
Evaluation Circuit Board



List of Materials for Evaluation PCB 108782 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	2 mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3	0.01 µF Capacitor, 0402 Pkg.
R1	5k Ohm Resistor, 0402 Pkg.
U1	HMC305LP4 / HMC305LP4E Digital Attenuator
PCB [2]	108780 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed ground paddle should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite Microwave Corporation upon request.