HMC493LP3

SMT GaAs HBT MMIC DIVIDE-BY-4, DC - 18 GHz

Typical Applications

Prescaler for DC to 18 GHz PLL Applications:

- Point-to-Point / Multi-Point Radios
- VSAT Radios
- Fiber Optic
- Test Equipment
- Military

Features

Ultra Low SSB Phase Noise: -150 dBc/Hz

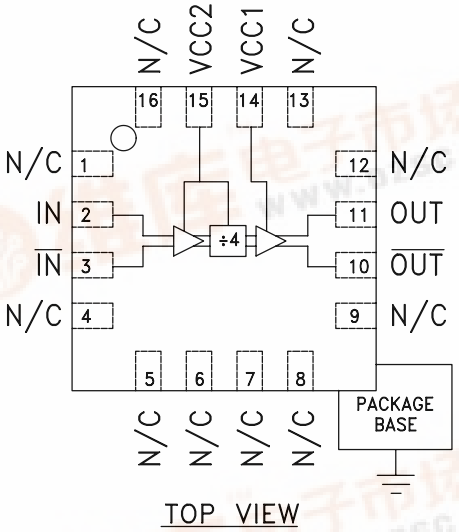
Very Wide Bandwidth

Output Power: -4 dBm

Single DC Supply: +5V

3 x 3 x 1 mm QFN SMT Package

Functional Diagram



TOP VIEW

General Description

The HMC493LP3 is a low noise Divide-by-4 Static Divider utilizing InGaP GaAs HBT technology packaged in a leadless 3x3 mm QFN surface mount plastic package. This device operates from DC (with a square wave input) to 18 GHz input frequency from a single +5.0V DC supply. The low additive SSB phase noise of -150 dBc/Hz at 100 kHz offset helps the user maintain excellent system noise performance.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vcc= +5V

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency		18	18.5		GHz
Minimum Input Frequency	Sine Wave Input. [1]		0.2	0.5	GHz
Input Power Range	Fin = 2 to 12 GHz	-15	-20	+10	dBm
	Fin = 12 to 14 GHz	-15	-20	+3	dBm
	Fin = 14 to 16 GHz	-15	-20	0	dBm
	Fin = 16 to 18 GHz	-10	-15	0	dBm
Output Power	Fin = 0.5 to 18 GHz	-7	-4		dBm
Reverse Leakage	Both RF Outputs Terminated		55		dB
SSB Phase Noise (100 kHz offset)	Pin = 0 dBm, Fin = 6 GHz		-150		dBc/Hz
Output Transition Time	Pin = 0 dBm, Fout = 882 MHz		100		pSec
Supply Current (Icc1 + Icc2)			96		mA

1. Divider will operate down to DC for square-wave input signal.

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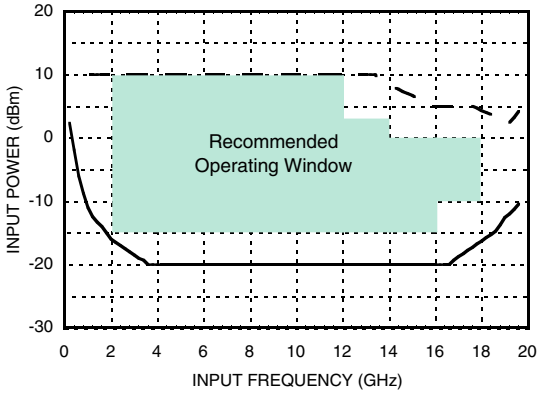
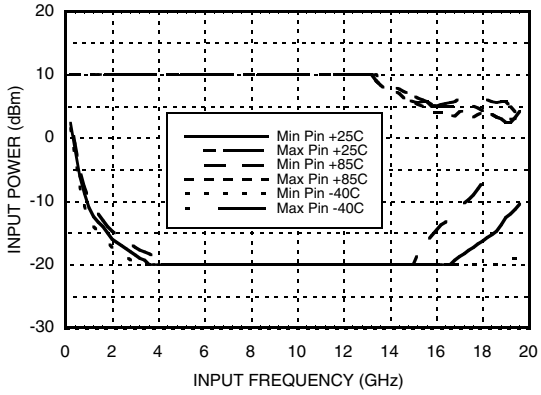
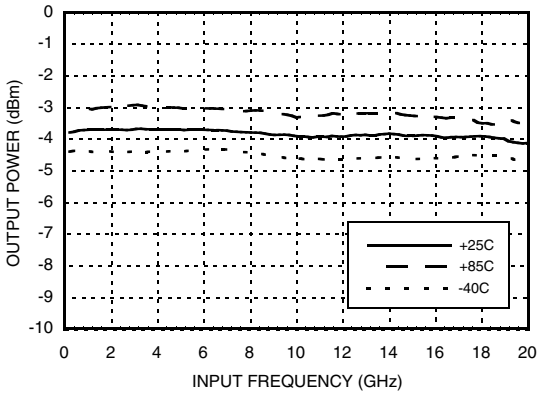
Input Sensitivity Window, T= 25 °C



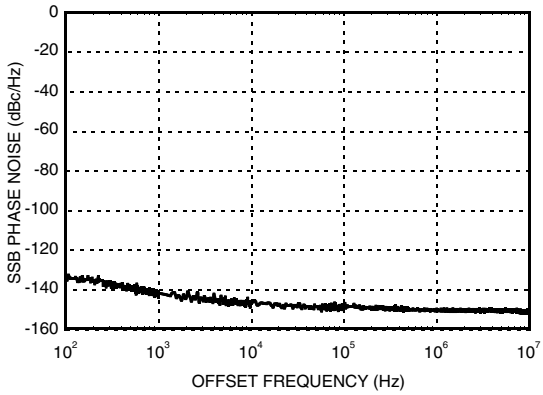
Input Sensitivity Window vs. Temperature



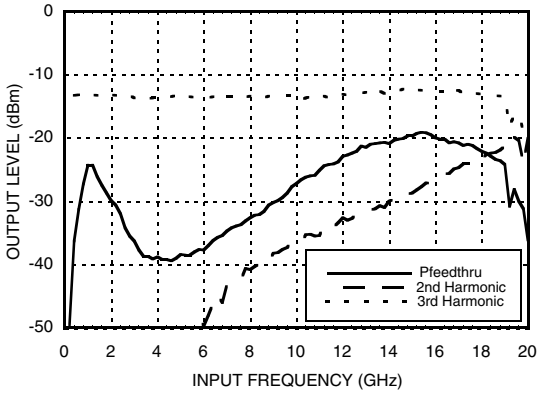
Output Power vs. Temperature



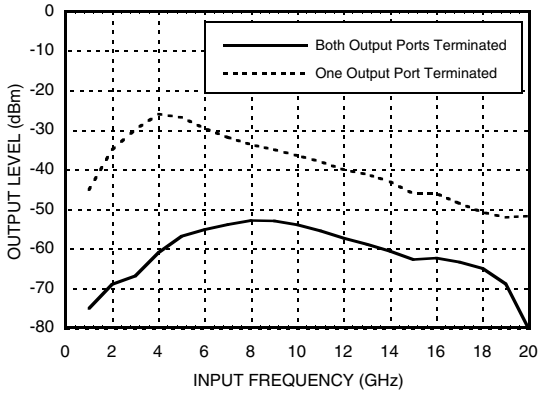
SSB Phase Noise Performance, Pin= 0 dBm, T= 25 °C



Output Harmonic Content, Pin= 0 dBm, T= 25 °C



Reverse Leakage, Pin= 0 dBm, T= 25 °C



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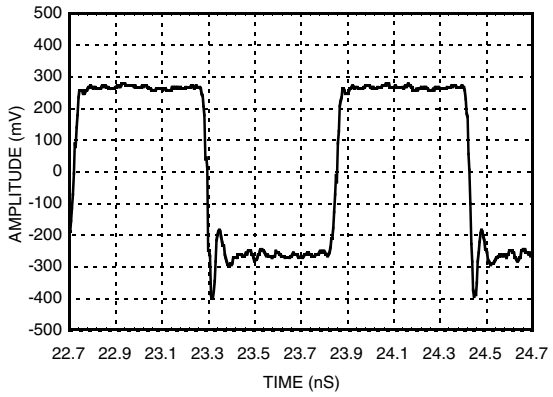
Output Voltage Waveform, Pin= 0 dBm, Fout= 882 MHz, T= 25 °C



Absolute Maximum Ratings

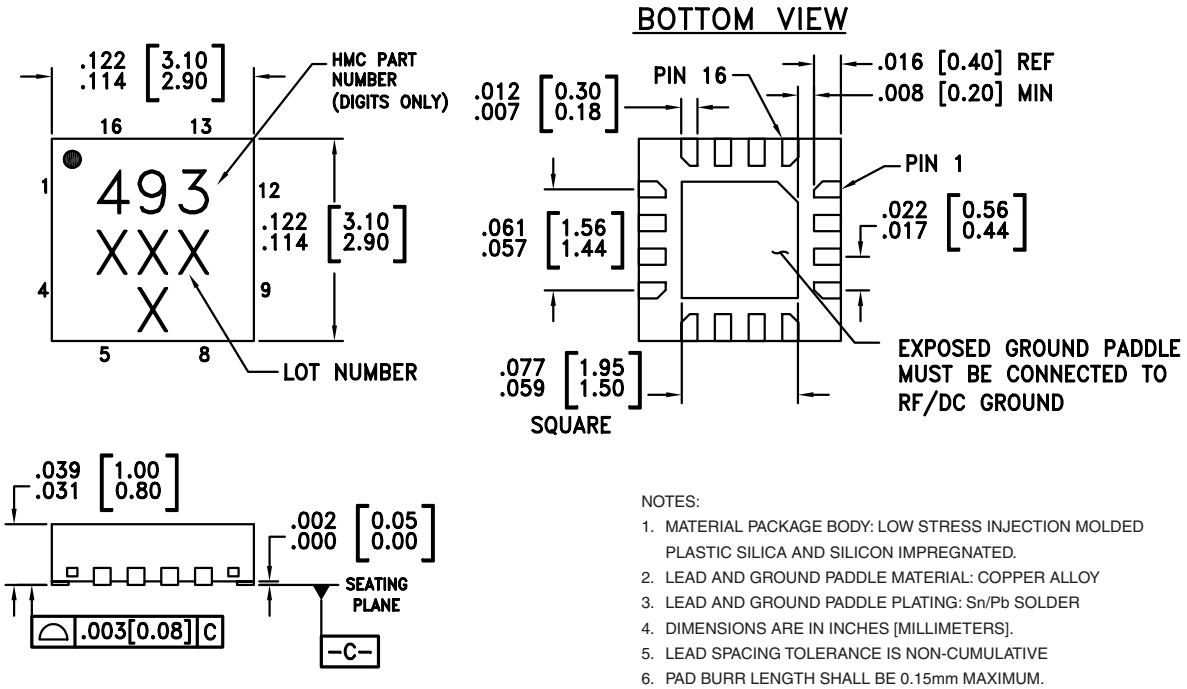
RF Input (Vcc = +5V)	+13 dBm
Supply Voltage (Vcc1, Vcc2)	+5.5V
Channel Temperature (Tc)	135 °C
Continuous Pdiss (T = 85 °C) (derate 11.9 mW/° C above 85 °C)	593 mW
Thermal Resistance (R_{TH}) (junction to ground paddle)	84 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vcc

Vcc1, Vcc2 (V)	Icc (mA)
4.75	84
5.0	96
5.25	108

Note: Divider will operate over full voltage range shown above

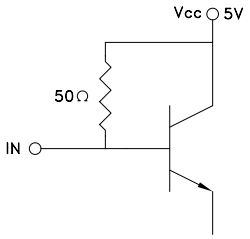
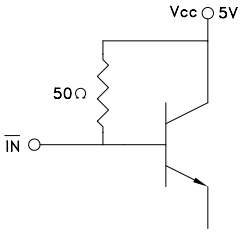
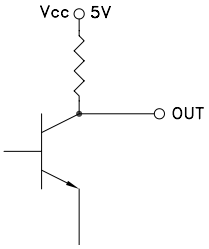
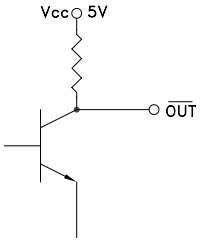
Outline Drawing



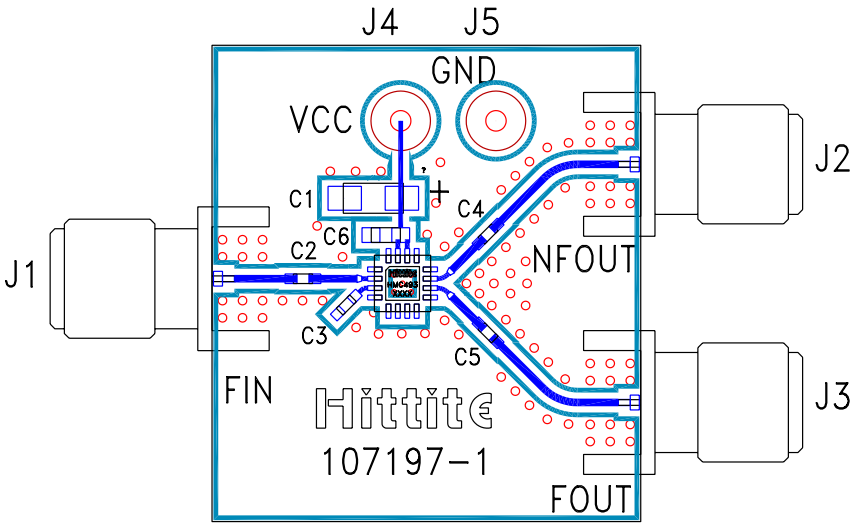
NOTES:

1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Pin Description

Pin Number	Function	Description	Interface Schematic
1, 4-9, 12, 13, 16	N/C	No connection.	
2	IN	RF Input must be DC blocked.	
3	$\overline{IN}$	RF Input 180° out of phase with pin 2 for differential operation. AC ground for single ended operation.	
10	OUT	Divided Output.	
11	$\overline{OUT}$	Divided output 180° out of phase with pin 10.	
14, 15	Vcc1, Vcc2	Supply voltage 5V ± 0.25V. Connect both pins to +5V supply.	
	GND	Ground: Backside of package has exposed metal ground slug which must be connected to RF/DC ground.	

Evaluation PCB



List of Materials

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4, J5	DC Pin
C2 - C5	100 pF Capacitor, 0402 Pkg.
C6	1000 pF Capacitor, 0603 Pkg.
C1	2.2 uF Tantalum Capacitor
U1	HMC492LP3 Divide-by-2
PCB*	107197 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. This evaluation board is designed for single ended input testing. J2 and J3 provide differential output signals.

Application Circuit