Hittite MICROWAVE CORPORATION v02.0705

RoHS✓ EARTH FRIENDLY

HMC495LP3 / 495LP3E

SiGe WIDEBAND DIRECT MODULATOR RFIC, 250 - 3800 MHz

Typical Applications

The HMC495LP3 / HMC495LP3E is suitable for various modulation systems:

- UMTS, GSM or CDMA Basestations
- Fixed Wireless or WLL
- ISM Transceivers, 900 & 2400 MHz
- GMSK, QPSK, QAM, SSB Modulators

Features

Wideband RF Frequency Range

High Carrier Suppression: 38 dBc

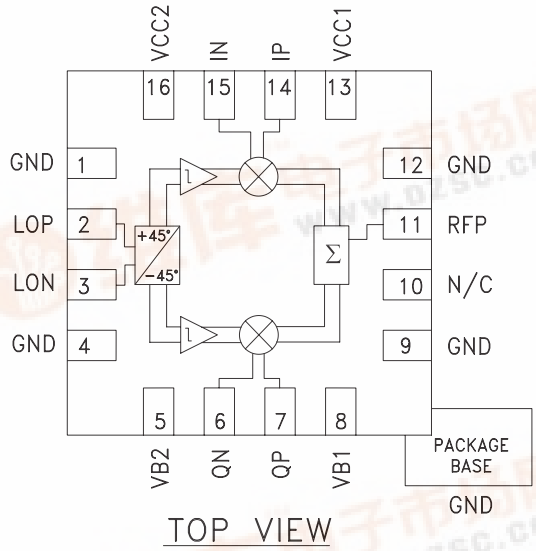
Very Low Noise Floor: -158 dBm/Hz

Low LO Power: -6 to +6 dBm

Differential or Single Ended LO Input

Single Low Current Supply: +3.3V@ 108 mA

Functional Diagram



TOP VIEW

General Description

The HMC495LP3 & HMC495LP3E are low noise Wideband Direct Quadrature Modulator RFICs which are ideal for digital modulation applications from 250 - 3800 MHz including; Cellular/3G, Broadband Wireless Access & ISM circuits. Housed in a compact 3x3 mm (LP3) SMT QFN package, the RFIC requires minimal external components & provides a low cost alternative to more complicated double upconversion architectures. The RF output port is single-ended and matched to 50 Ohms with no external components. The LO requires -6 to +6 dBm and can be driven in either differential or single-ended mode while the Baseband inputs will support modulation inputs from DC - 250 MHz typical. This device is optimized for a supply voltage of +3.3V @ 108 mA and will provide stable performance over a +3.0V to +3.6V range.

Electrical Specifications, *See Test Conditions on following page herein.*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF		450 - 960			1800 - 2200			2100 - 2700			3400 - 3800		MHz
Output Power	-7	-5		-8	-6		-9	-7		-11	-9		dBm
Output P1dB		2			1			0			-2		dBm
Output IP3		17			14			14			13		dBm
Output Noise Floor		-159			-158			-158			-157		dBm/Hz
Carrier Suppression (uncalibrated)		38			38			35			34		dBc
Sideband Suppression (uncalibrated)		34			31			30			28		dBc
IM3 Suppression		59			50			50			56		dBc
RF Port Return Loss		18			17			16			13		dB
LO Port Return Loss		13			8			7			5		dB
CDMA IS95													
ACPR@ 880 MHz & 1960 MHz		-72			-71.5			N/A			N/A		dBc
Channel Power		-15			-18.4			N/A			N/A		dBm
W-CDMA 3GPP													
ACPR@ 1960 & 2140 MHz		N/A			-60			-59			N/A		dBc
Channel Power		N/A			-17.3			-14.4			N/A		dBm

Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		0.25		3.8	GHz
RF Return Loss			16		dB
LO Input					
LO Frequency Range		0.25		3.8	GHz
LO Input Power	With 68 Ohm shunt resistor on LO port.	-6	0	+6	dBm
LO Port Return Loss	With 68 Ohm shunt resistor on LO port.		7		dB
Baseband Input Port					
Baseband Port Bandwidth	With 50Ω source & external 10 pF shunt cap to ground. Refer to HMC495LP3 Application Circuit.	DC		250	MHz
Baseband Input DC Voltage (Vbbdc)	This parameter can be varied in order to optimize the device performance over temperature and/or supply.	1.0	1.15	1.2	V
Baseband Input DC Bias Current (Ibbdc)	Single-ended.		40		µA
Single-ended Baseband Input Capacitance	De-embed to the lead of the device.		0.5		pF
DC Power Requirements	See Test Conditions Below				
Supply Voltage (Vcc1, Vcc2, Vb1, Vb2)		3	3.3	3.6	V
Supply Current (Icc1, Icc2, Ib1, Ib2)			108		mA

Test Conditions: Unless Otherwise Specified, the Following Test Conditions Were Used

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	1.15V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	800 mV
Baseband Input AC Voltage for OIP3 Measurement (Peak to Peak Differential, I and Q)	400 mV per tone @ 150 & 250 kHz
Frequency Offset for Output Noise Measurements	20 MHz
Supply & Bias Voltage (Vb1, Vb2, Vcc1, Vcc2)	3.3V
LO Input Power	0 dBm
LO Input Mode	Single-Ended
Mounting Configuration	Refer to HMC495LP3 Application Schematic Herein
Sideband & Carrier Feedthrough	Uncalibrated

Calibrated vs. Uncalibrated Test Results

During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The “Uncalibrated, +25 °C” Sideband and Carrier Suppression plots were measured at room temperature, while the “Uncalibrated, over Temperature” Sideband and Carrier Suppression plots represent the worst case uncalibrated suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated, + 25 °C” Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case calibrated Sideband Suppression levels at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated, +25 °C” Carrier Suppression data was plotted after a manual adjustment of the Ip/In & Qp/Qn DC offsets at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case Carrier Suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

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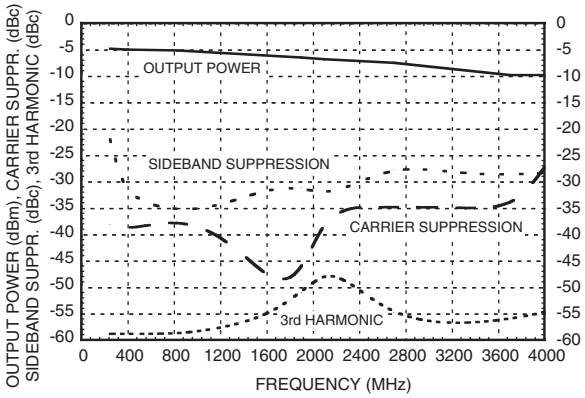
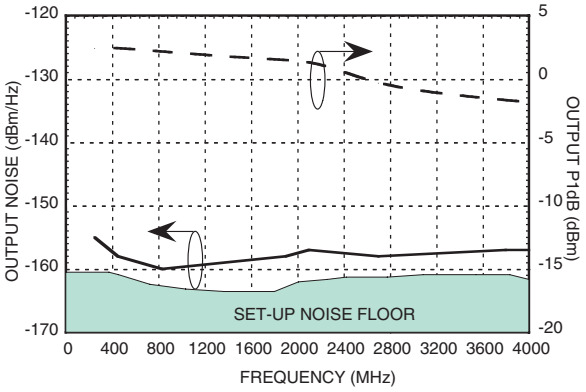
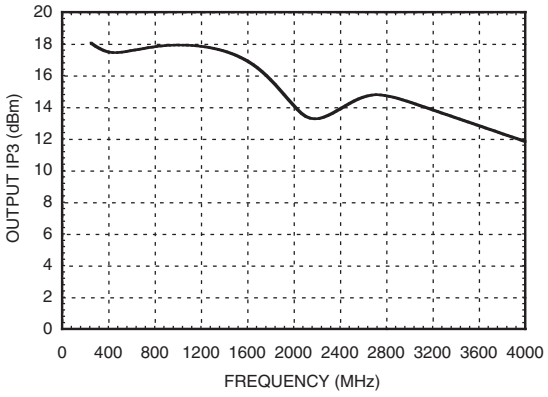
Wideband Performance vs. Frequency



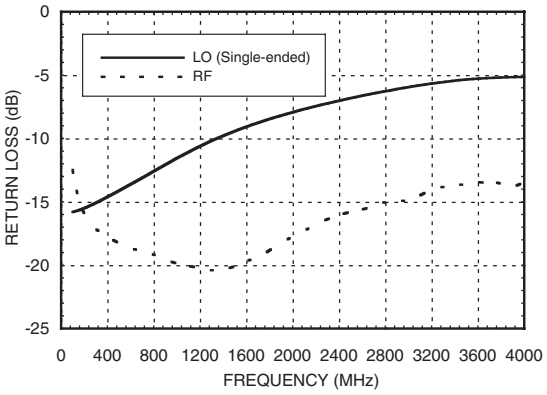
Output Noise Floor and P1dB vs. Frequency



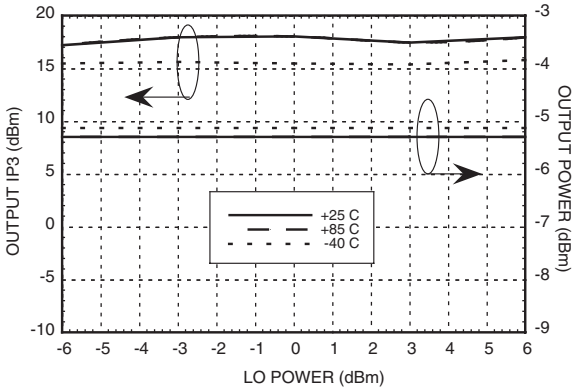
Output IP3 vs. Frequency



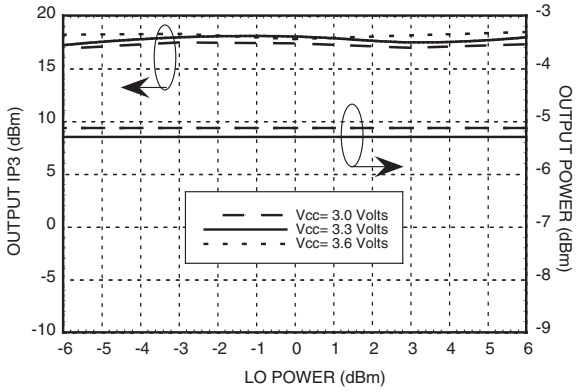
Return Loss



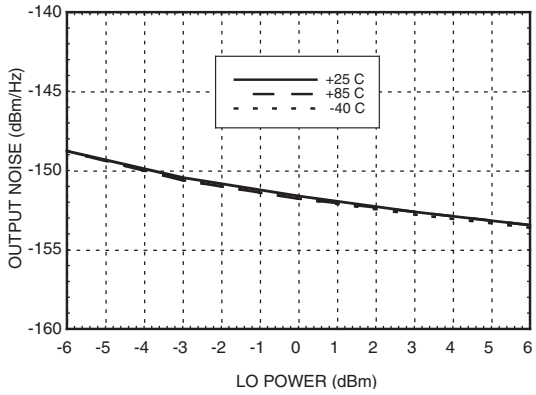
Output IP3 & Output Power vs. LO Power Over Temperature@ 830 MHz



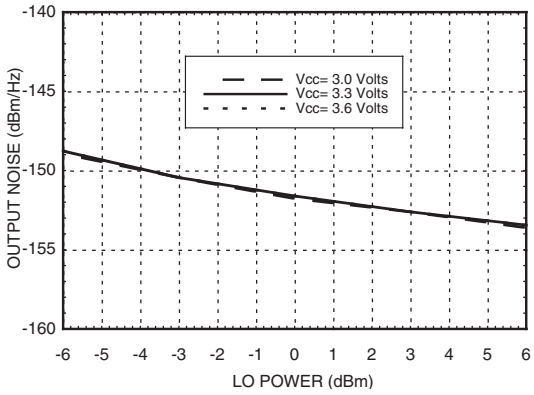
Output IP3 & Output Power vs. LO Power Over Supply@ 830 MHz



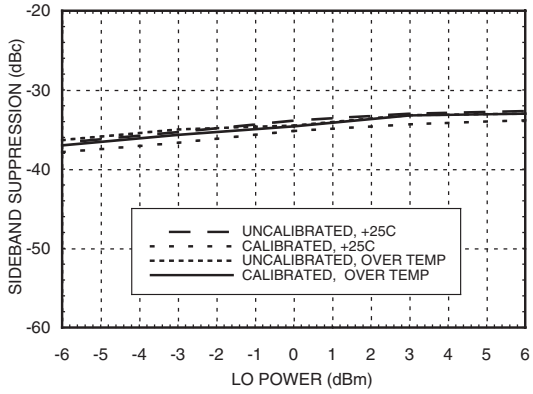
Output Noise vs. LO Power Over Temperature@ 830 MHz



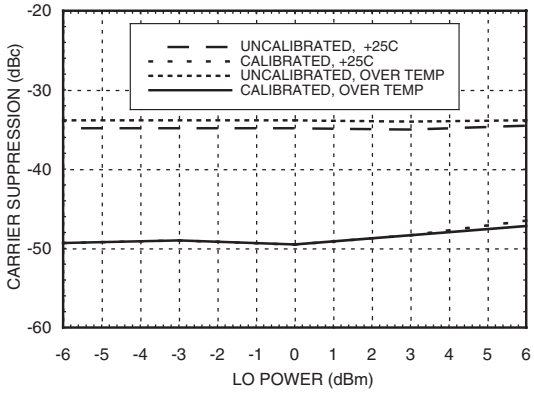
Output Noise vs. LO Power Over Supply@ 830 MHz



Sideband Suppression* vs. LO Power@ 830 MHz



Carrier Suppression* vs. LO Power@ 830 MHz



** See note titled "Calibrated vs. Uncalibrated test results" herein.*

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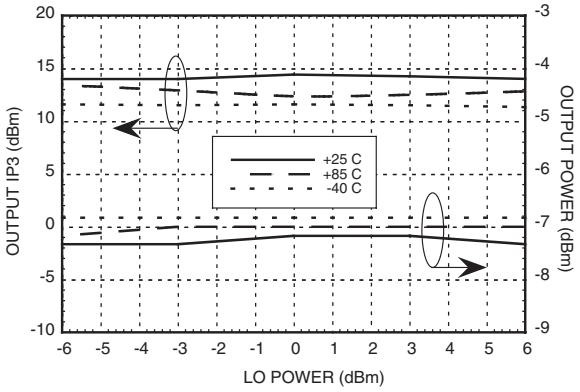
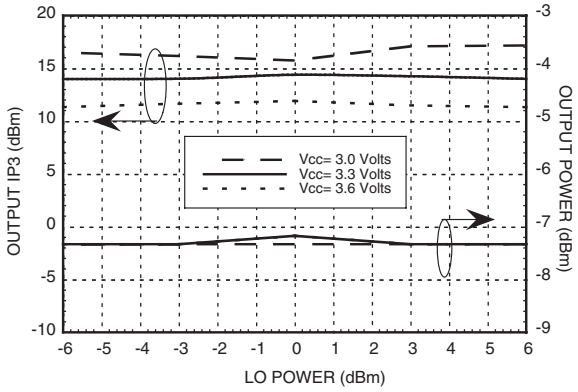
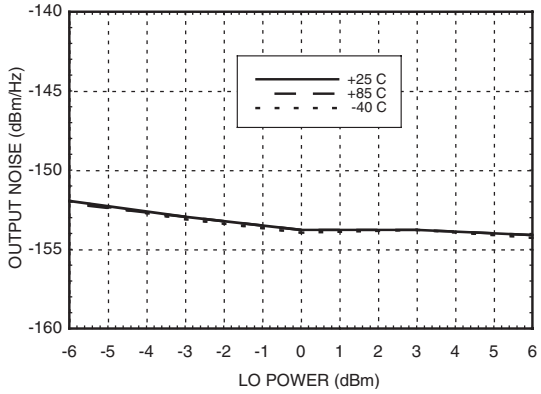
Output IP3 & Output Power vs. LO Power Over Temperature@ 1900 MHz



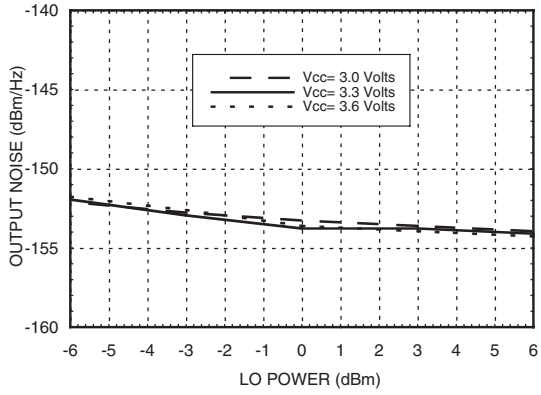
Output IP3 & Output Power vs. LO Power Over Supply@ 1900 MHz



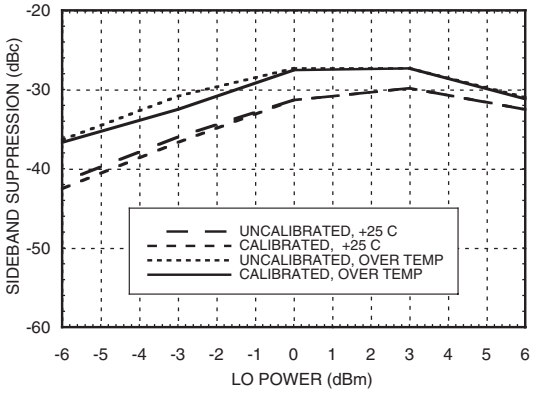
Output Noise vs. LO Power Over Temperature@ 1900 MHz



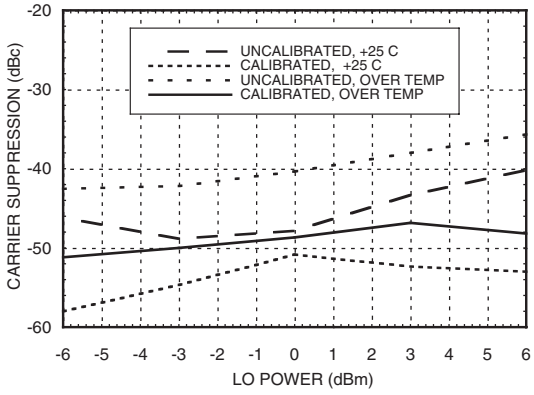
Output Noise vs. LO Power Over Supply@ 1900 MHz



Sideband Suppression* vs. LO Power@ 1900 MHz

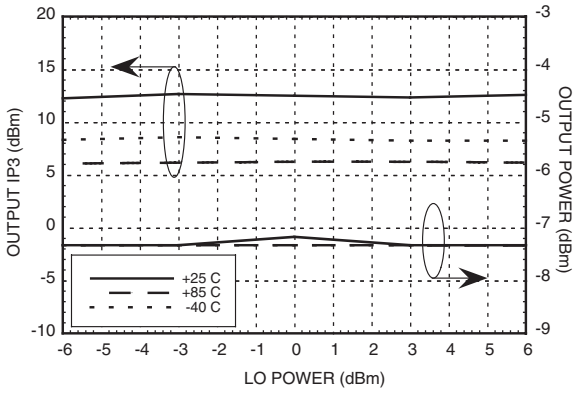


Carrier Suppression* vs. LO Power@ 1900 MHz

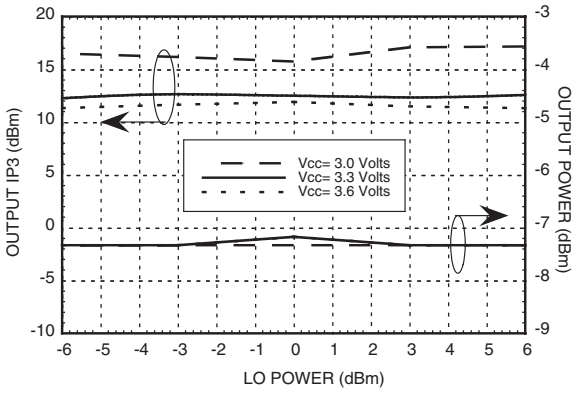


** See note titled "Calibrated vs. Uncalibrated test results" herein.*

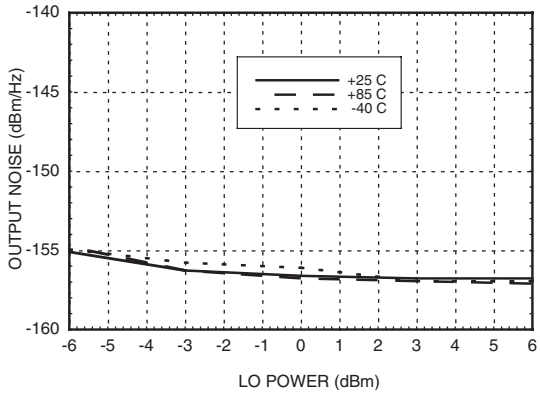
Output IP3 & Output Power vs. LO Power Over Temperature@ 2100 MHz



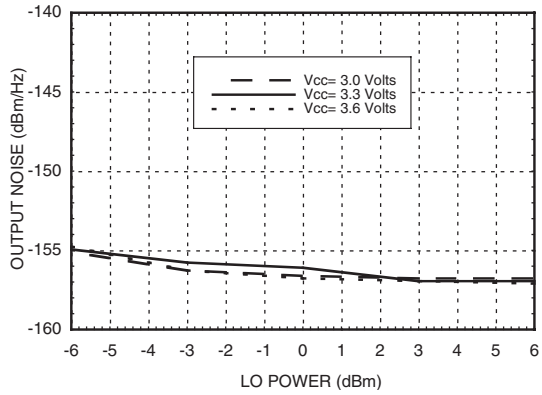
Output IP3 & Output Power vs. LO Power Over Supply@ 2100 MHz



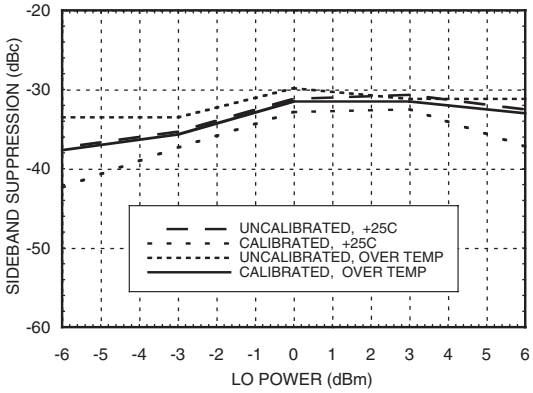
Output Noise vs. LO Power Over Temperature@ 2100 MHz



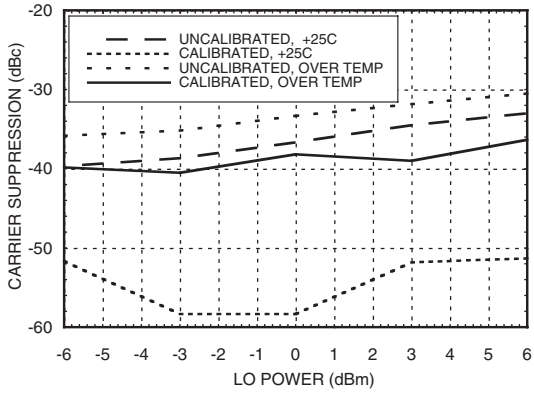
Output Noise vs. LO Power Over Supply@ 2100 MHz



Sideband Suppression* vs. LO Power@ 2100 MHz



Carrier Suppression* vs. LO Power@ 2100 MHz

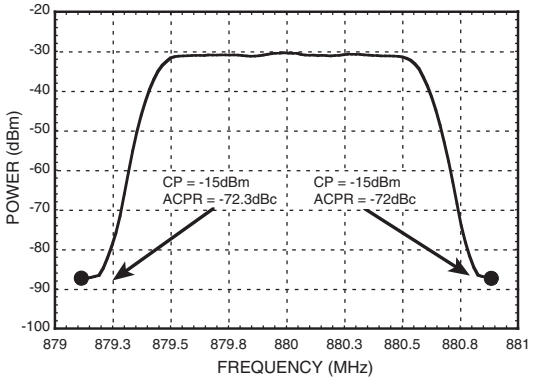


** See note titled "Calibrated vs. Uncalibrated test results" herein.*

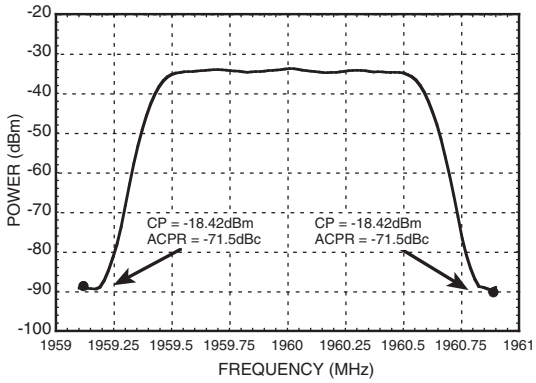
HMC495LP3 / 495LP3E

SiGe WIDEBAND DIRECT MODULATOR RFIC, 250 - 3800 MHz

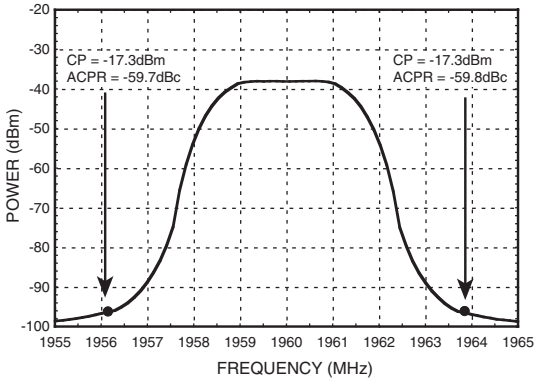
Cellular CDMA @ 880 MHz
ACPR @ 885 kHz, Vcc= 3.3V, Vdc= 1.15V



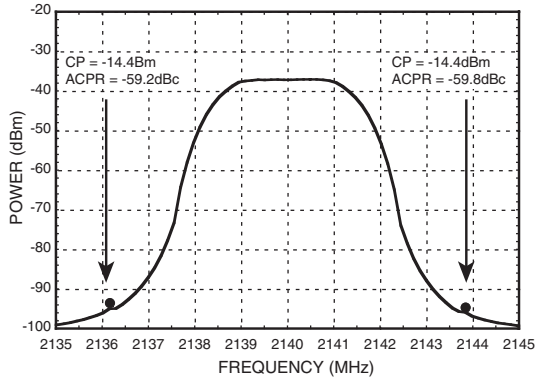
PCS CDMA @ 1960 MHz
ACPR @ 885 kHz, Vcc= 3.3V, Vdc= 1.15V



W-CDMA @ 1960 MHz
ACPR @ 3.84 MHz, Vcc= 3.3V, Vdc= 1.15V



W-CDMA @ 2140 MHz
ACPR @ 3.84 MHz, Vcc= 3.3V, Vdc= 1.15V



Note 1: W-CDMA (Modulation Set-up for ACPR Mode); The Baseband I and Q input signals were generated using “Test Model 1 with 64 channels” settings in the Agilent E3844C.

Note 2: CDMA (Modulation Set-up for ACPR Mode); The Baseband I and Q input signals were generated using the “9 channels forward” settings in the Agilent E3844C (pilot, paging, sync and 6 traffic channels).

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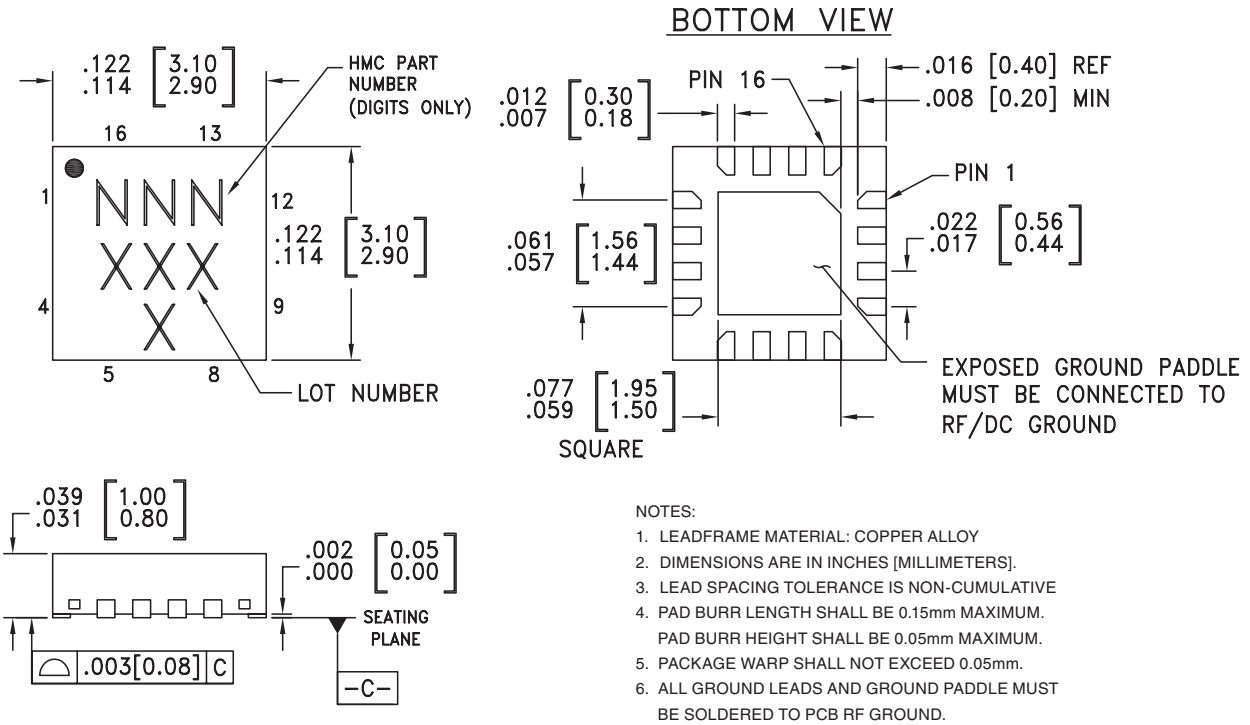
SiGe WIDEBAND DIRECT MODULATOR RFIC, 250 - 3800 MHz

Absolute Maximum Ratings

Vcc1, Vcc2, VB1, VB2	-0.5 to +6V
LO Input Power	+10 dBm Max.
Baseband Input Voltage (Reference to GND)	-0.5 to +1.8V
Channel Temperature	150 °C
Continuous Pdiss (T = 85°C) (Derate 43.5 mW/°C above 85°C)	2.83 Watts
Thermal Resistance (R_{th}) (junction to lead)	23 °C/Watt
Storage Temperature	-40 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC495LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	495 XXXX
HMC495LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	495 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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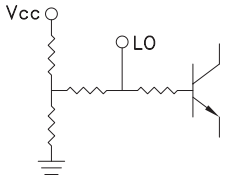
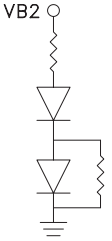
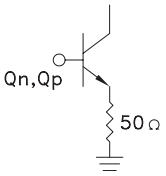
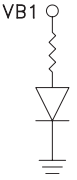
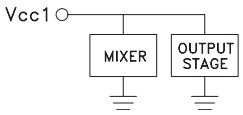
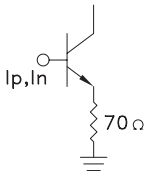
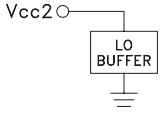
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 9, 12	GND	These pins and the ground paddle must be connected to a high quality RF/DC ground.	
2, 3	LOP, LON	Differential LO input ports. This device may be driven in either differential or single ended mode. In single ended mode, one port should be driven by the LO source while the other port may be terminated with a 50Ω resistor to ground. An external shunt 68Ω resistor is used to improve VSWR, while an external 100 pF capacitor is required to prevent DC supply voltage from appearing on the customer's PC board.	
5	VB2	Bias Voltage for the LO stage. This voltage will affect the Sideband Suppression, the Output Noise Floor and the Power Consumption. The ideal voltage range for this port is between +2.7 Vdc and +3.0 Vdc. The nominal current for this port is 5.3 mA.	
6, 7	Qn, Qp	Differential Quadrature baseband input. These are high impedance ports. The nominal recommended bias voltage is between 1.0 - 1.15V. The nominal recommended baseband input voltage is 800 mV peak to peak differential. By adjusting the DC bias voltage on ports Qn & Qp, the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltage for optimization is less than 5 mV. The amplitude and phase difference between the I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level.	
8	VB1	Bias Voltage for the output stage. This voltage should be connected to the Vcc supply. Nominal supply voltage is 3.3 Vdc. The nominal current for this port is 2.4 mA.	
10	N/C	No connect.	
11	RFP	RF Output port. This port is matched to 50Ω. A series capacitor should be connected to this port in order to prevent the DC supply voltage from appearing on the customer's PC board.	

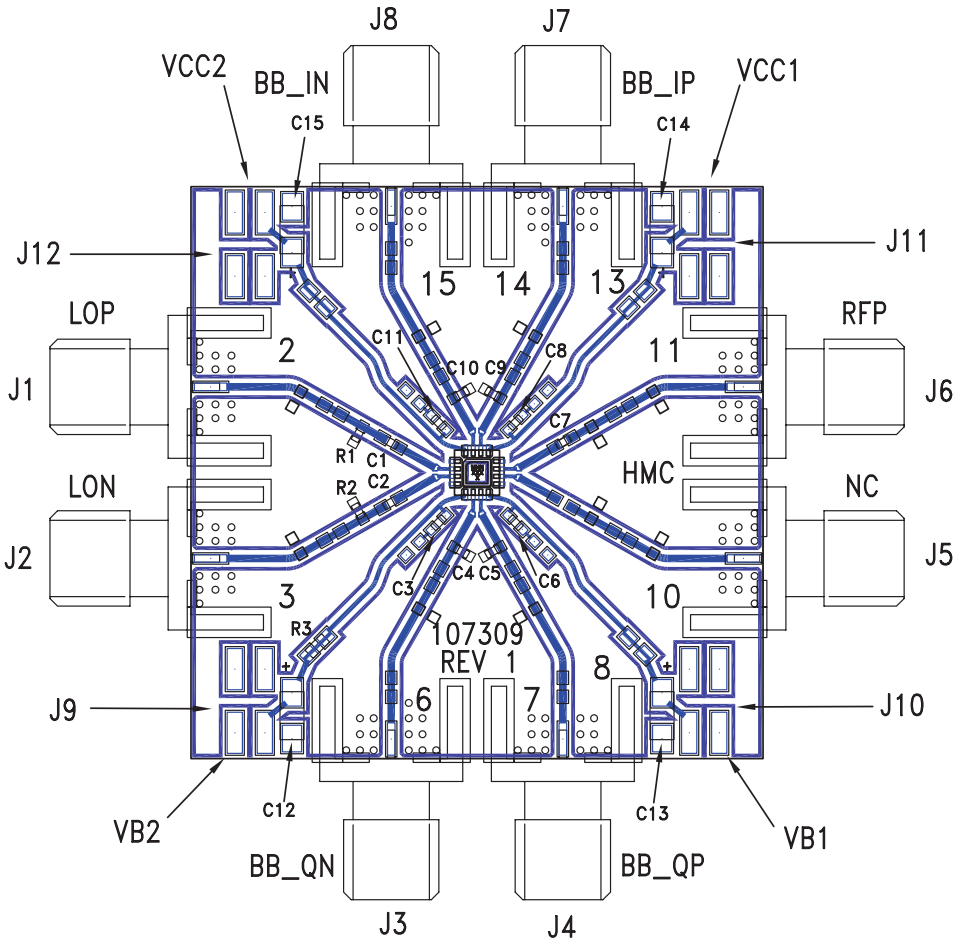
Pin Descriptions *(continued)*

Pin Number	Function	Description	Interface Schematic
13	Vcc1	Supply voltage for the mixer and output stages. Set to 3.3V for nominal operation. The nominal current for this port is 37 mA.	
14, 15	Ip, In	Differential In-Phase baseband input. These are high impedance ports. The nominal recommended bias voltage is between 1.0 - 1.15V.The nominal recommened baseband input voltage is 800 mV peak to peak differential. By adjusting the DC bias voltage on ports In & Ip, the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltage for optimization is less than 5 mV. The amplitude and phase difference between the I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level.	
16	Vcc2	Supply voltage for the LO stage. Set to 3.3V for nominal operation. The nominal current for this port is 64 mA.	

HMC495LP3 / 495LP3E

SiGe WIDEBAND DIRECT MODULATOR RFIC, 250 - 3800 MHz

Evaluation PCB



List of Materials for Evaluation PCB 107413 [1]

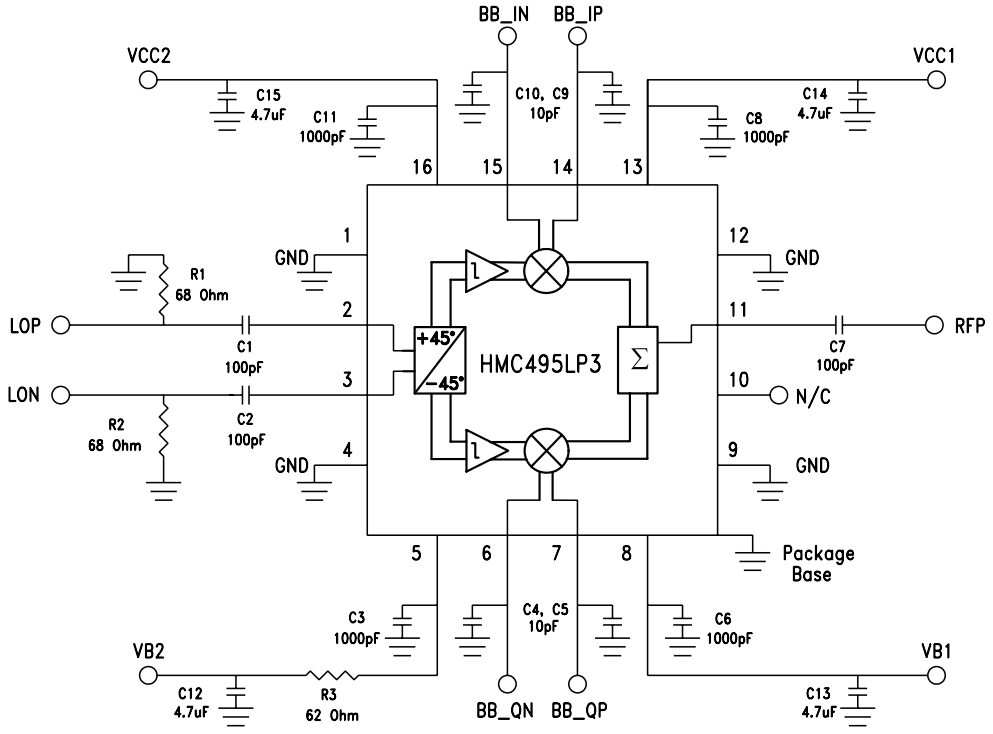
Item	Description
J1 - J8	PCB Mount SMA Connector
J9 - J12	DC Molex Connector
C1, C2, C7	100 pF Chip Capacitor, 0402 Pkg.
C3, C6, C8, C11	1000 pF Chip Capacitor, 0402 Pkg.
C4, C5, C9, C10	10 pF Chip Capacitor, 0402 Pkg.
C12 - C15	4.7 uF, Case A, Tantulum
R1, R2	68 Ohms, 0402 Pkg.
R3	62 Ohms, 0402 Pkg.
U1	HMC495LP3 / HMC495LP3E Modulator
PCB [2]	107309 Eval Board

[1] Reference this number when ordering complete evaulation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application & Evaluation PCB Schematic



Note:

Baseband input frequency range is dependent on value of C4, C5, C9 and C10. The value of 10 pF was chosen to give a typical response of DC - 250 MHz. Input frequency range can be extended up to 1 GHz with possible degradation of LO leakage and broadband noise floor response by decreasing the value of C4, C5, C9 & C10.

Characterization Set-up