



HMC581LP6 / 581LP6E

HIGH IP3 RFIC DUAL DOWNCONVERTER, 800 - 960 MHz

Typical Applications

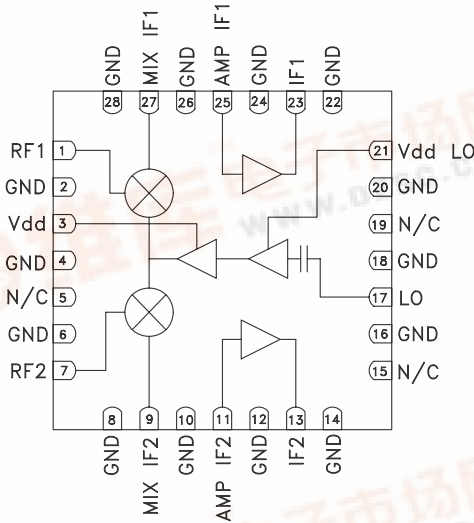
The HMC581LP6 / HMC581LP6E is ideal for Wireless Infrastructure Applications:

- GSM, GPRS & EDGE
- CDMA & W-CDMA
- Cellular / 3G Infrastructure

Features

- +26 dBm Input IP3
- Low Single Input LO Drive: 0 dBm
- 9 dB Conversion Gain
- 13 dB Noise Figure
- Single Positive Supply: +5V @ 260 mA

Functional Diagram



General Description

The HMC581LP6 & HMC581LP6E are high linearity Dual Down Converter Receiver ICs that operate from 800 - 960 MHz and deliver a +26 dBm input third order intercept point for UMTS & GSM applications. The passive mixer outputs and high dynamic range IF amplifier inputs are positioned so that an external IF filter can be placed in series between them. The converter provides a gain of 9 dB and typical single side band noise figure of 13 dB. The IC operates from a single +5V supply consuming 260 mA of current while requiring only 0 dBm LO drive. The design requires no external baluns, no external matching and supports IF frequencies between 50 and 300 MHz.

Electrical Specifications, $T_A = +25^\circ C$, LO = 0 dBm, Vdd = +5V, IF = 105 MHz*

Parameter	Min.	Typ.	Max.	Units
Frequency Range, RF		800 - 960		MHz
Frequency Range, LO		700 - 1160		MHz
Frequency Range, IF		50 - 300		MHz
Conversion Gain	7	9		dB
Noise Figure (SSB)		13		dB
LO to RF Isolation		4		dB
LO to IF Isolation		10		dB
RF to IF Isolation		15		dB
IP3 (Input)	23	26		dBm
1 dB Compression (Input)		9.5		dBm
Branch Isolation		40		dB
LO Drive Input Level (Typical)		-4 to +4		dBm
Supply Current (I _{dd} for LO & IF) (IF bias resistor= 4.7 Ohms)		256		mA

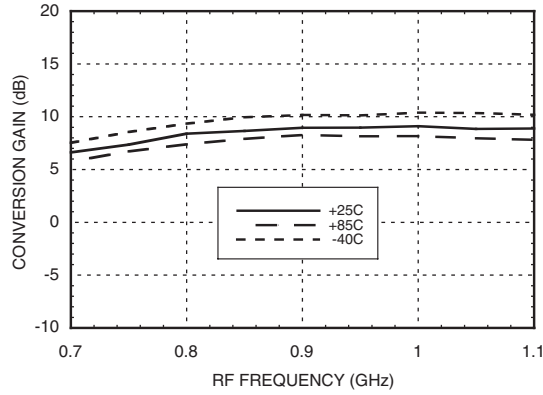
*Unless otherwise noted all measurements with low side LO & IF = 105 MHz.



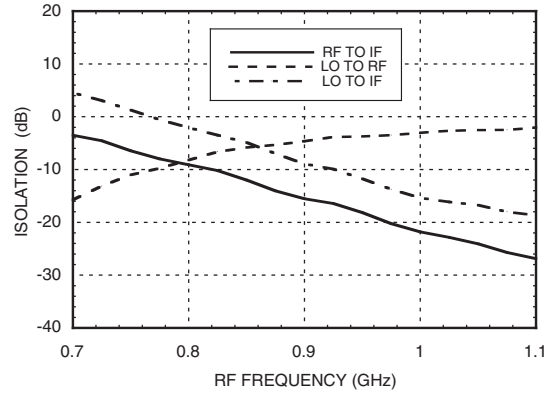
HMC581LP6 / 581LP6E

HIGH IP3 RFIC DUAL DOWNCONVERTER, 800 - 960 MHz

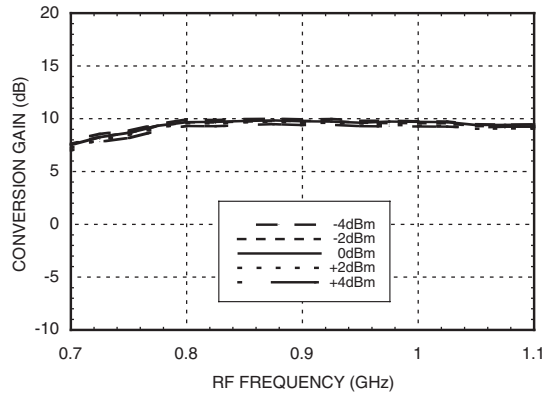
Conversion Gain vs. Temperature
@ LO = 0 dBm, IF = 200 MHz



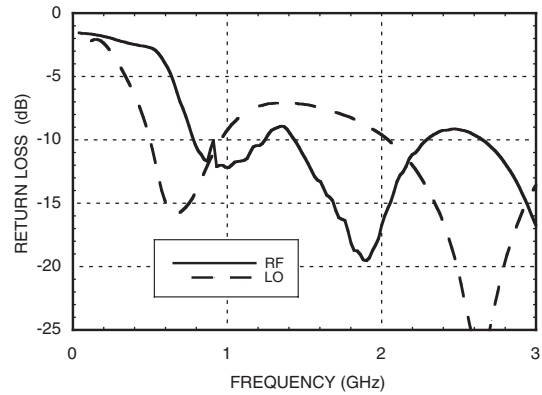
Isolation @ LO = 0 dBm



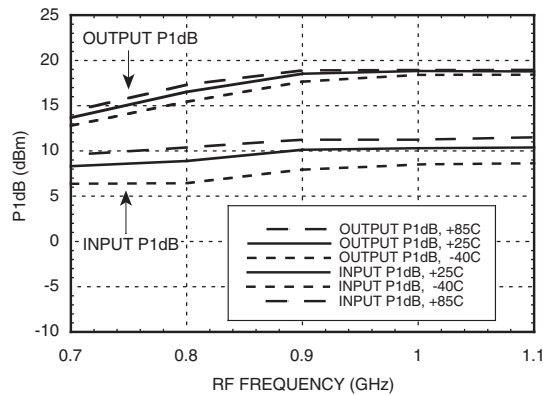
Conversion Gain vs. LO Drive, IF = 105 MHz



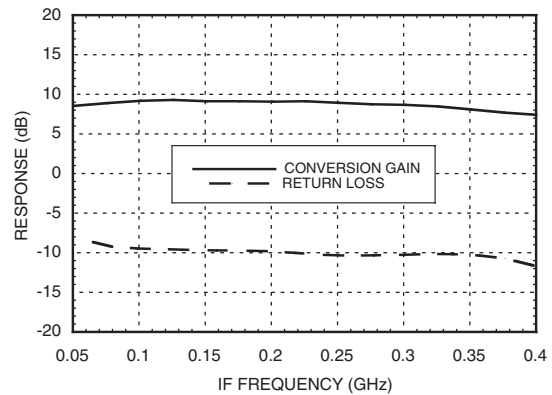
Return Loss @ LO = 0 dBm



P1dB vs. Temperature
@ LO = 0 dBm, IF = 200 MHz



IF Bandwidth, LO = 0 dBm



* Unless otherwise noted all measurements with low side LO & IF = 105 MHz.



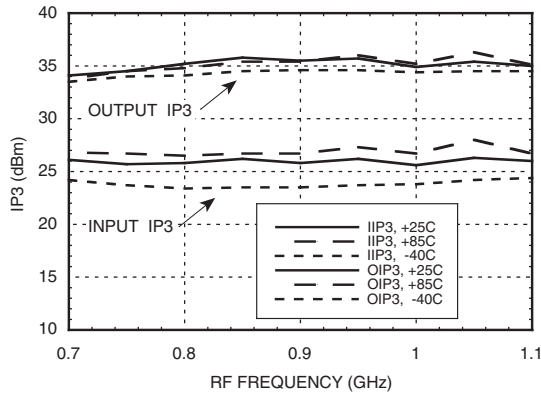
HMC581LP6 / 581LP6E

**HIGH IP3 RFIC DUAL
DOWNCONVERTER, 800 - 960 MHz**

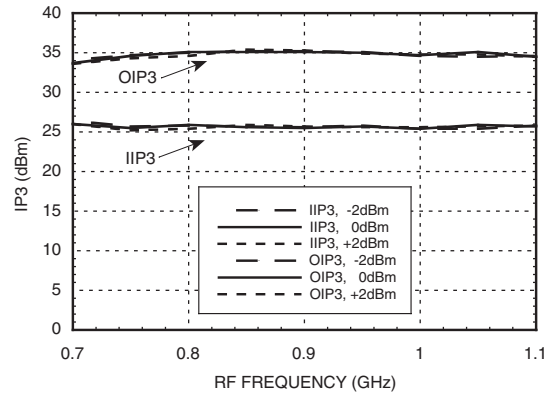
8

MIXERS - SMT

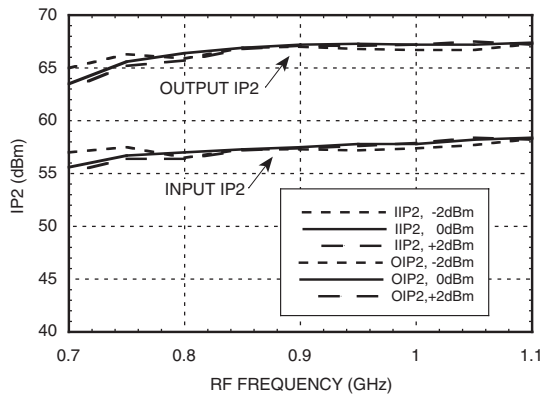
Input & Output IP3 vs. Temperature
@ LO = 0 dBm, IF = 200 MHz



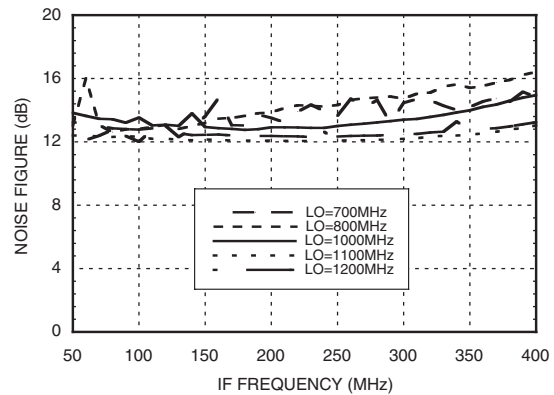
Input & Output IP3 vs LO Drive,
IF = 200 MHz



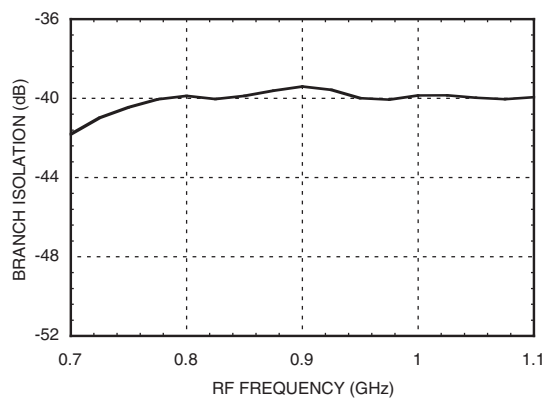
Input & Output IP2 vs. LO Drive,
IF = 200 MHz



Noise Figure vs. IF Frequency



Branch Isolation RF1, IF2 @ LO = 0 dBm



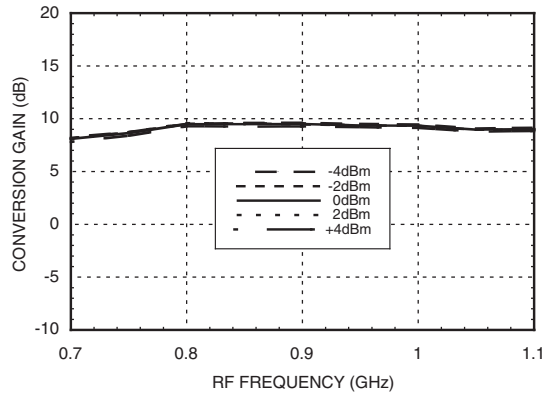
* Unless otherwise noted all measurements with low side LO & IF = 105 MHz.



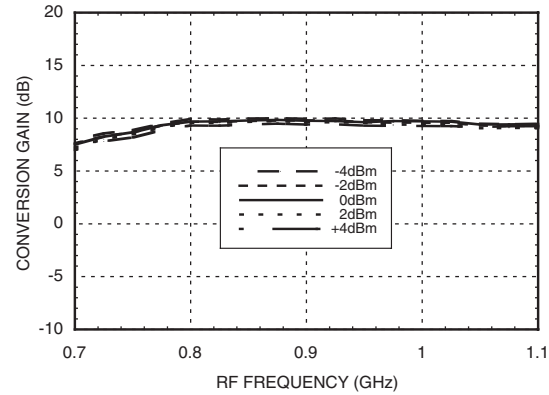
HMC581LP6 / 581LP6E

HIGH IP3 RFIC DUAL DOWNCONVERTER, 800 - 960 MHz

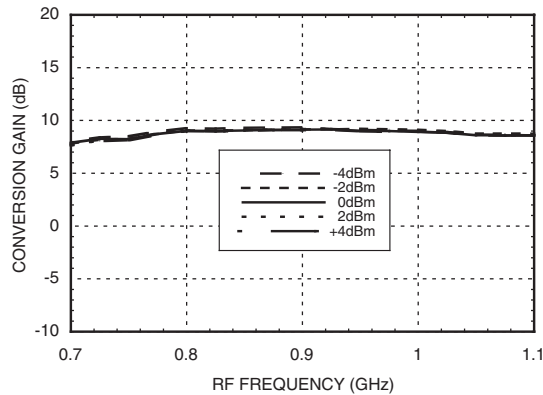
Conversion Gain vs. LO Drive IF = 70 MHz



Conversion Gain vs. LO Drive, IF = 150 MHz



Conversion Gain vs. LO Drive, IF = 200 MHz



MxN Spurious @ IF Port

mRF	nLO				
	0	1	2	3	4
0	xx	2	36	32	53
1	19	0	26	58	62
2	75	65	50	54	89
3	108	93	88	78	89
4	123	123	117	103	89

RF Freq. = 0.8 GHz @ -10 dBm
 LO Freq. = 0.7 GHz @ 0 dBm
 All values in dBc below IF power level (1RF - 1LO).

Typical Supply Current vs. Vdd

Vdd (LO + IF)	Idd (mA)
+4.5	190
+5.0	260
+5.5	340

Downconverter will operate over full voltage range shown above.

Harmonics of LO

LO Freq. (GHz)	nLO Spur @ RF Port			
	1	2	3	4
0.6	15	16	14	26
0.7	7	22	15	37
0.8	4	23	19	46
0.9	3	17	25	38
1	2	17	23	25
1.1	1	20	12	24

LO = 0 dBm
 All values in dBc below input LO level measured at RF port.



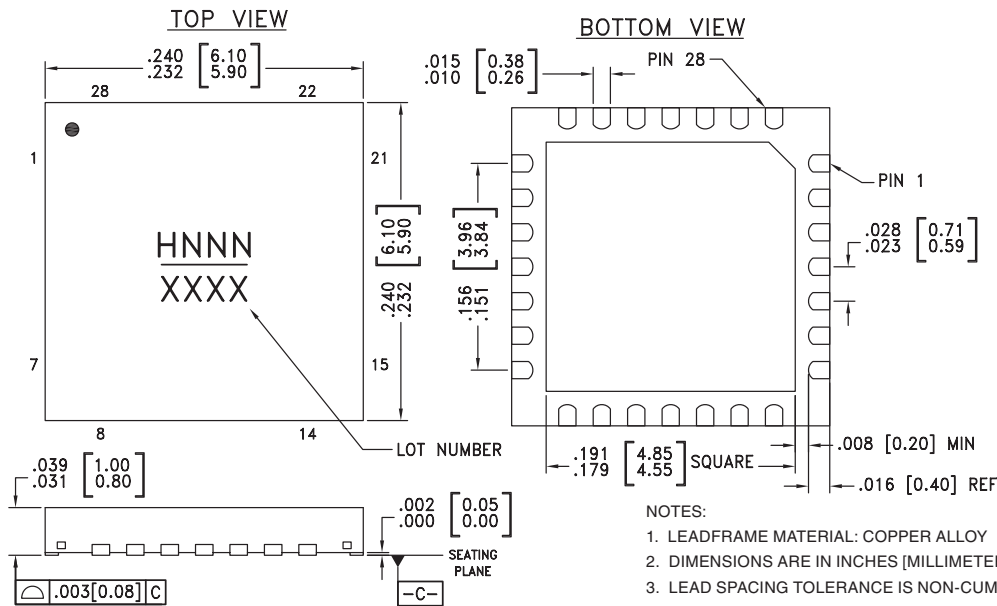
Absolute Maximum Ratings

RF / IF Input (Vdd= +5V)	+13 dBm
LO Drive (Vdd= +5V)	+15 dBm
Vdd (LO or IF)	+7 Vdc
Channel Temperature	150°C
Continuous P _{diss} (T = 85°C) (derate 25.5 mW/°C above 85°C)	1.64 W
Thermal Resistance (channel to ground paddle)	39.6 °C/W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85°C



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

- LEADFRAME MATERIAL: COPPER ALLOY
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

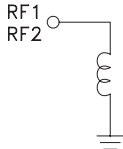

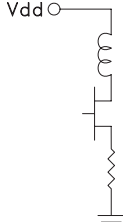
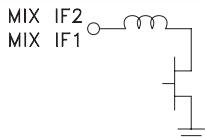
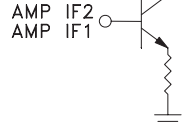
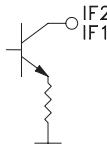
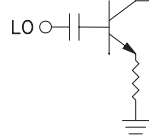
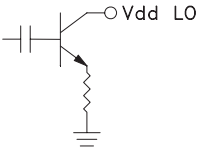
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC581LP6	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 ^[1]	H581 XXXX
HMC581LP6E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H581 XXXX

[1] Max peak reflow temperature of 235 °C

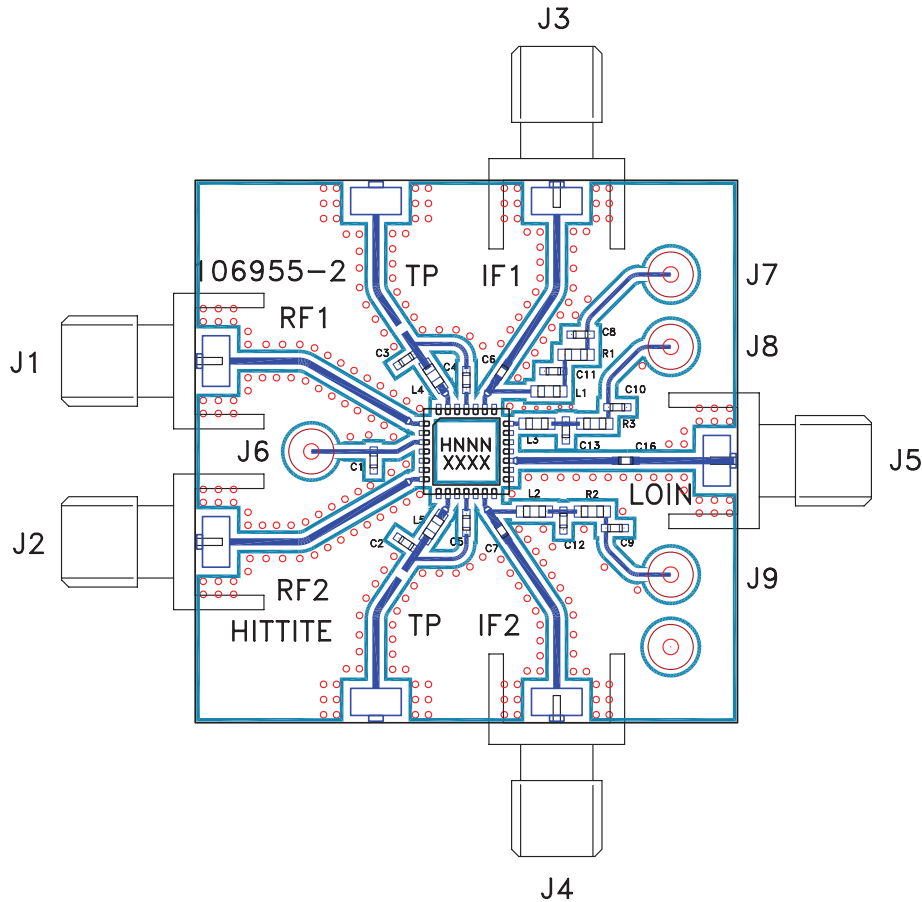
[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 7	RF1, RF2	These pins are DC coupled and matched to 50 Ohms.	
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28	GND	Backside of package has exposed metal ground slug that must also be connected to ground.	
3	Vdd	Power supply for the second stage LO amplifier. One external bypass capacitor (1,000 pF) is required. 61 mA typical, 73 mA maximum.	
5, 15, 19	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
9, 27	MIX IF2, MIX IF1	IF output from the mixers. This pin is DC coupled to the mixer. A low pass filter and blocking capacitor are required between mixer IF port and IF amplifier. (See application circuit).	
11, 25	AMP IF2, AMP IF1	Inputs to the IF amplifiers. A low pass filter and blocking capacitor are required between mixer IF port and IF amplifier. (See application circuit).	
13, 23	IF2, IF1	Outputs of the IF amplifiers and bias ports for the IF amplifiers. A pull up inductor, resistor, and bypass capacitors are required. (See application circuit). IF1 = 71 mA typical, 85 mA maximum. IF2 = 71 mA typical, 85 mA maximum.	
17	LO	This pin is AC coupled and matched to 50 Ohms.	
21	Vdd LO	Bias voltage for the first stage of the LO amplifier. A pull up inductor, resistor, and bypass capacitors are required. (See application circuit). 53 mA typical, 64 mA maximum.	

Evaluation PCB



List of Materials for Evaluation PCB 115316 [1]

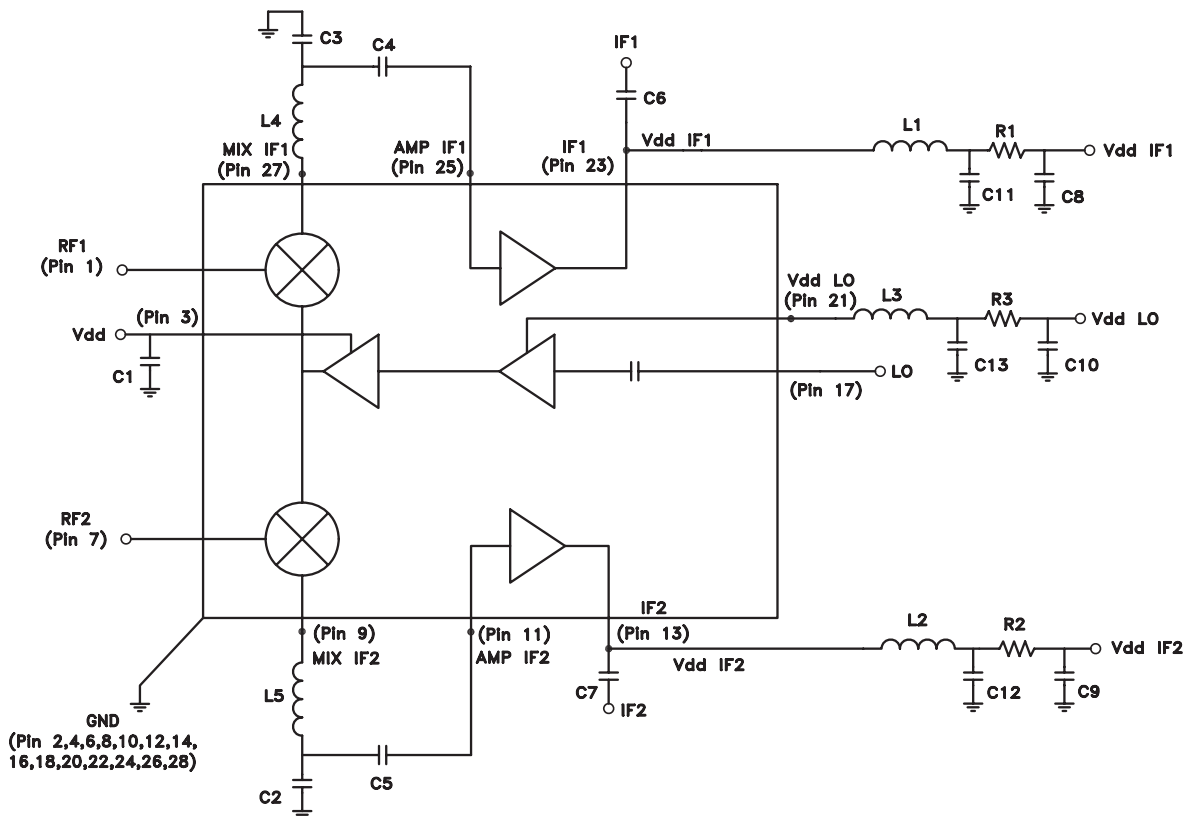
Item	Description
J1 - J5	PCB Mount SMA RF Connector
J6 - J9	DC Pins
C1, C4 - C10	1000 pF Chip Capacitor, 0402 Pkg.
C2, C3	7 pF Chip Capacitor, 0402 Pkg.
C11, C12, C13	100 pF Chip Capacitor, 0402 Pkg.
L1, L2	220 nH Chip Inductor, 0603 Pkg.
L3	22 nH Chip Inductor, 0603 Pkg.
L4, L5	27 nH Chip Inductor, 0603 Pkg.
R1, R2	4.7 Ohm Resistor, 0603 Pkg.
R3	22 Ohm Resistor, 0603 Pkg.
U1	HMC581LP6 / HMC581LP6E
PCB [2]	106955-2 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Recommended Components Values (IF = DC - 300 MHz)	
C1, C4 - C10	1000 pF
C2, C3	7 pF
C11, C12, C13	100 pF
L1, L2	220 nH
L3	22 nH
L4, L5	27 nH
R1, R2	4.7 Ohm
R3	22 Ohm

Note: L4, C3 and L5, C2 form low pass filters, these values may be changed for optimization of LO to IF isolation, depending on application frequency. C4 and C5 are DC blocks.