



HMC610LP4 / 610LP4E

**70 dB RMS POWER
DETECTOR, DC - 3.9 GHz**

Typical Applications

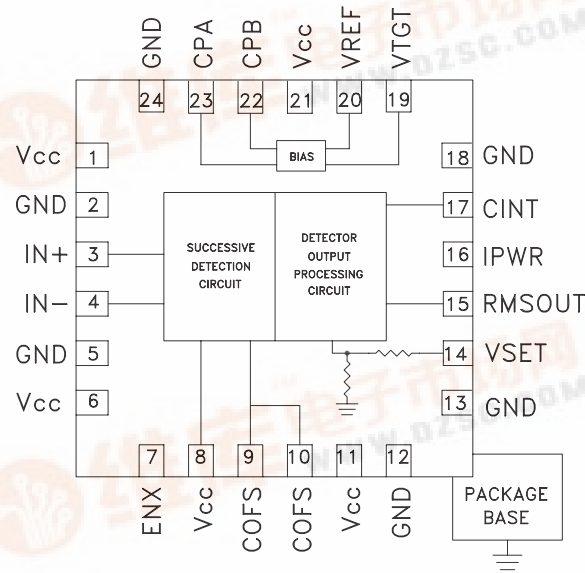
The HMC610LP4(E) is ideal for:

- Cellular / PCS / 3G
- WiMAX, WiBro, Fixed Wireless, & Military
- RF & Microwave Instrumentation
- Power Amplifier Linearization / Control Loops
- Transmitter Power Control
- Transmitter Signal Strength Indication

Features

- Accurate RMS-to-DC Conversion: DC to 3.9 GHz^[1]
- Input Dynamic Range of >70 dB:
-60 to +10 dBm in 50 Ohms
- Waveform & Modulation Independent:
GSM / CDMA / TDMA
- Linear-in-dB Output: Scaled 37 mV/dB
- Operates from 4.5 to 5.5V from -40°C to +85°C
- Power-Down Mode
- Compact 4x4mm Leadless SMT Package

Functional Diagram



General Description

The HMC610LP4(E) is a true RMS power detector capable of providing a ± 1 dB measurement dynamic range of more than 70 dB. It converts any RF input signal at its differential input, regardless of modulation or waveform complexity, to an accurately scaled linear-in-dB output response that is equivalent to the Root-Mean-Square (RMS) of the input waveform.

For normal operation, the RMSOUT pin is shorted to the VSET input, and will provide a nominal logarithmic slope of 37 mV/dB and an intercept of -70 dBm for frequencies up to 2 GHz; other slopes are achieved with external resistors connected between RMSOUT and VSET pins. Temperature stability is excellent with ± 0.5 dB error from -40°C to 85°C maintained from 100 MHz to 3.9 GHz.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $Z_o = 50\Omega$ [2]

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	900	1900	2200	2700	3000	3500	3900	MHz
Dynamic Range								
± 1 dB linearity, CW Input	73	72	71	68	65	56	42	dB
Deviation vs. Temperature								
Deviation from output @ 25°C, -45°C < T_A < 85°C; $P_{in} = -50\text{dBm}$	-0.9	-1.1	-1.2	-1.5	-0.8	-0.8	-1.0	dB
Deviation from output @ 25°C, -45°C < T_A < 85°C; $P_{in} = -20\text{dBm}$	0.5	0.3	0.2	0.3	0.6	0.4	0.3	dB
Deviation from output @ 25°C, -45°C < T_A < 85°C; $P_{in} = 5\text{dBm}$	0.8	0.5	0.4	0.8	1.2	1.3	1.3	dB

[1] Low frequency operation determined by external components

[2] Differential Input Drive Via 1:1 Balun Transformer, VTGT Connected to VREF, RMSOUT Connected to VSET, Unless Otherwise Noted.





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Electrical Specifications, (continued)

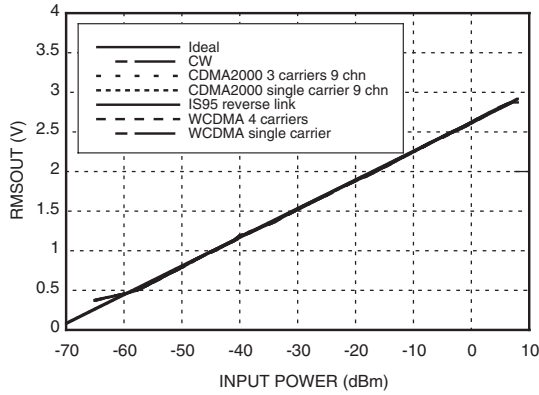
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	900	1900	2200	2700	3000	3500	3900	MHz
Modulation Deviation from CW Response								
CDMA2000 3 Carriers, 9 Channels	0.15	0.12	0.15	0.18	0.25	0.3	0.35	dB
CDMA2000 1 Carrier, 9 Channels	0.1	0.08	0.1	0.14	0.2	0.25	0.3	dB
IS95 Reverse Link	0.05	0.05	0.1	0.1	0.1	0.15	0.2	dB
WCDMA 1 Carrier	0.1	0.14	0.12	0.18	0.2	0.3	0.3	dB
WCDMA 4 Carrier	0.2	0.22	0.24	0.24	0.3	0.4	0.4	dB
Logarithmic Slope and Intercept								
Logarithmic Slope	36.5	37.3	37.8	39.3	40.5	43.5	47.5	mV/dBm
Logarithmic Intercept	-71.5	-70.3	-69	-65	-62	-57	-53	dBm
Parameter	Conditions			Min.	Typ.	Max.	Units	
RMS Conformance Error	f ≤ 2.7 GHz				±0.6		dB	
RF Input (INP, INN) Interface								
Input Resistance	Pins INN, INP, AC coupled, Differential drive				200		Ω	
Logout Interface (RMSOUT)								
Available Output Range	R _{LOAD} ≥ 200 Ω to ground			0.4		3.2	V	
Absolute Voltage Low End of Range	Detection mode, f=900 MHz, Pin= -58 dBm				0.5		V	
Absolute Voltage High End of Range	Detection mode, f=900 MHz, Pin= +15 dBm				3.12		V	
Source/Sink Current	RMSOUT held at Vs/2, to 1% change				8/0.4		mA	
Rise Time, 10% to 90%	0.2V to 1.9V, CINT=0				10		ns	
Fall Time, 90% to 10%	1.9V to 0.2V, CINT=0				500		ns	
VSET Interface (VSET)								
Nominal Input Voltage Range	To ±1 dB error			0.4		3.2	V	
Input Resistance					54		kΩ	
Voltage Reference (VREF)								
Output Voltage	T _A = 25°C				2		V	
Temperature Sensitivity	-40°C ≤ T _A ≤ +85°C						mV/°C	
Output Resistance	Small Signal at 100 kHz				8		Ω	
RMS Target Interface (VTGT)					2		V	
Nominal Input Voltage Range				0.3		4.2	V	
Power Supply Interface (Vdd)								
Supply Voltage				4.5		5.5	V	
Quiescent Current	Pin= -70 dBm				65		mA	
	Pin= +15 dBm				85		mA	



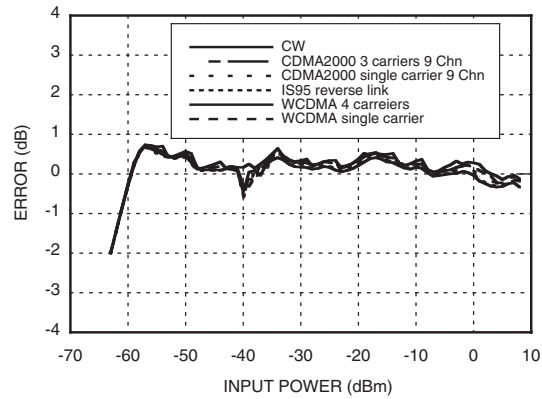
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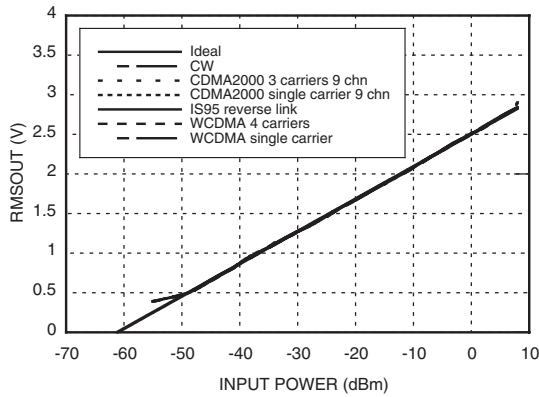
**RMSOUT vs. Pin with
Different Modulations @ 900 MHz**



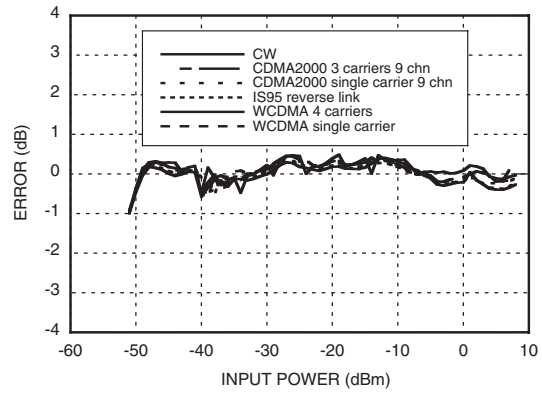
**RMSOUT Error vs. Pin with
Different Modulations @ 900 MHz**



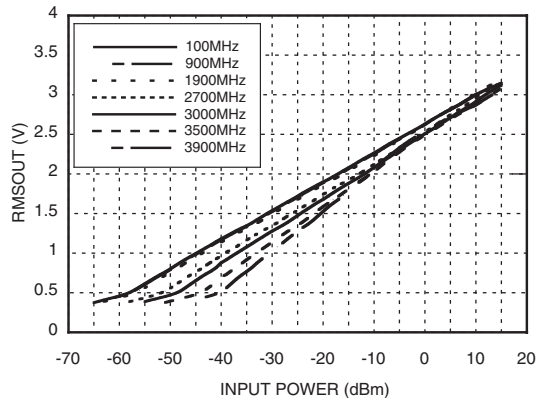
**RMSOUT vs. Pin with
Different Modulations @ 3000 MHz**



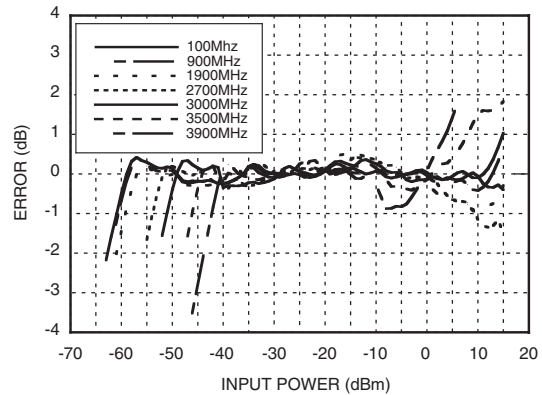
**RMSOUT Error vs. Pin with
Different Modulations @ 3000 MHz**



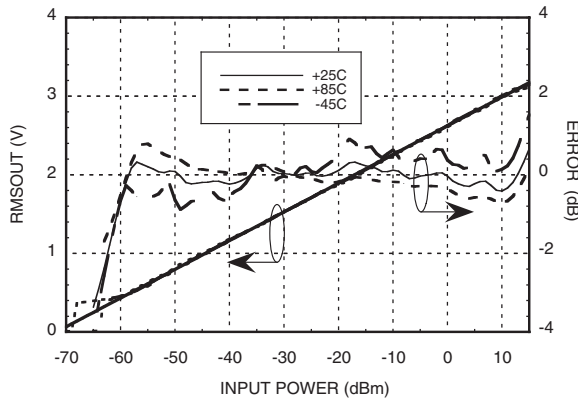
RMSOUT vs. Pin & Frequency



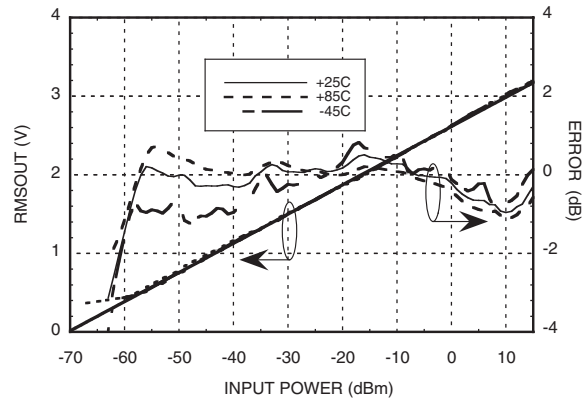
RMSOUT Error vs. Pin & Frequency



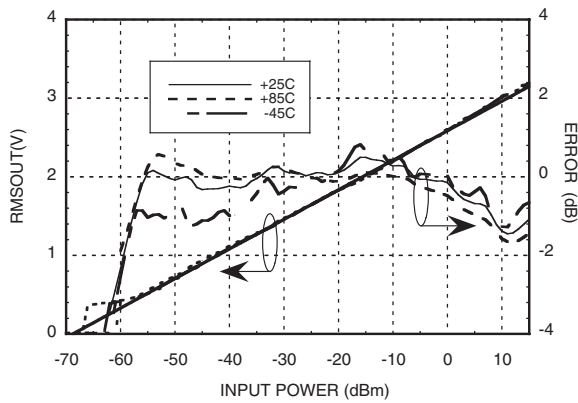
RMSOUT & Error vs. Pin @ 900 MHz^[1]



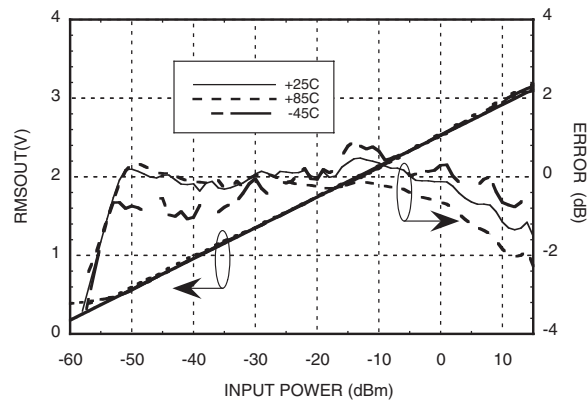
RMSOUT & Error vs. Pin @ 1900 MHz^[1]



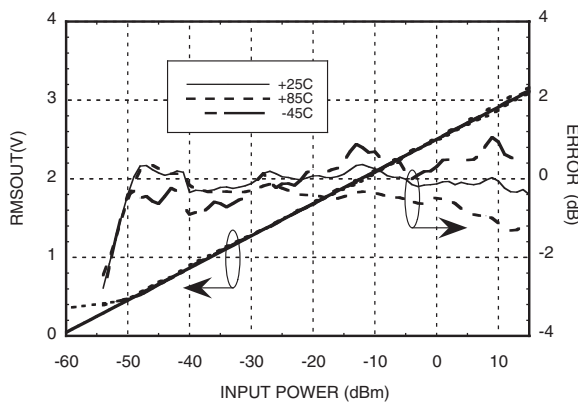
RMSOUT & Error vs. Pin @ 2200 MHz^[1]



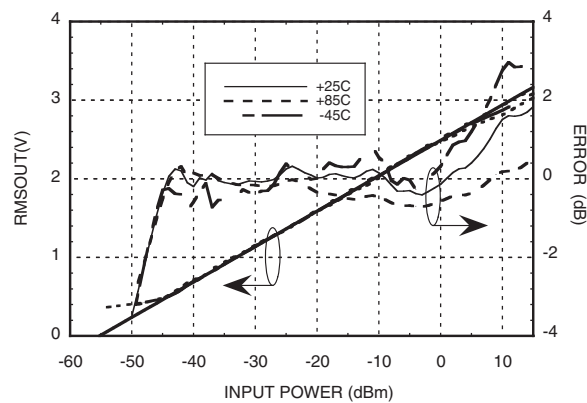
RMSOUT & Error vs. Pin @ 2700 MHz^[1]



RMSOUT & Error vs. Pin @ 3000 MHz^[1]

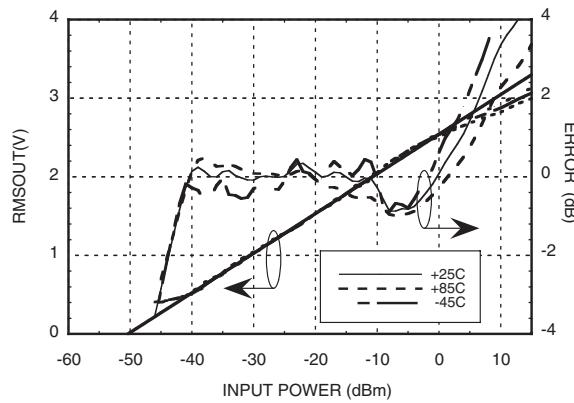


RMSOUT & Error vs. Pin @ 3500 MHz^[1]

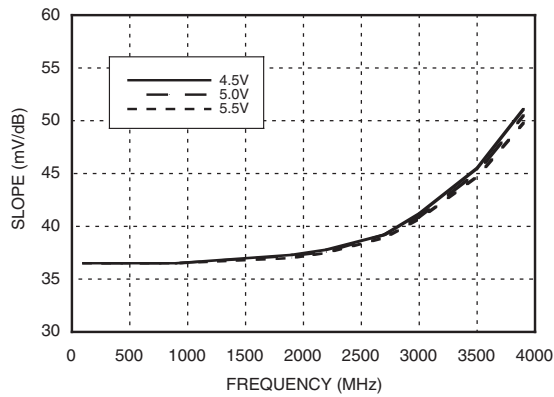


[1] CW input waveform.

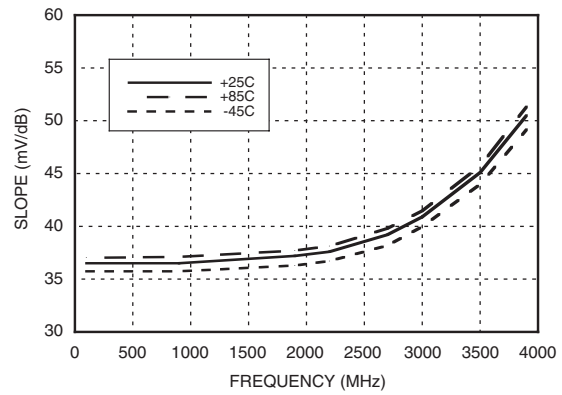
RMSOUT & Error vs. Pin @ 3900 MHz [1]



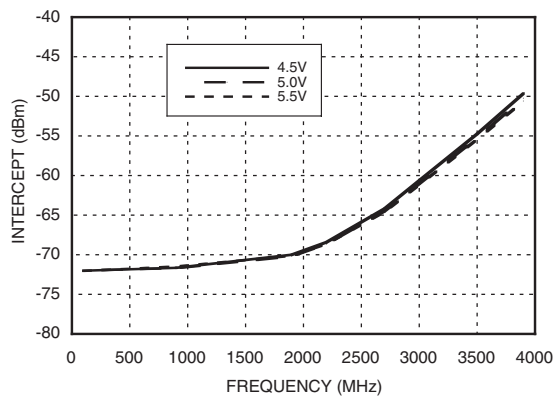
Slope vs. Frequency & Supply Voltage



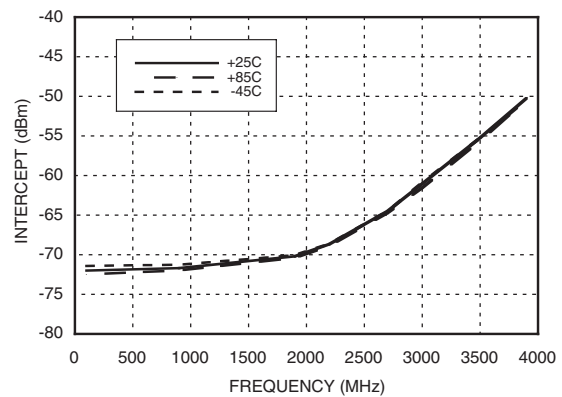
Slope vs. Frequency



Intercept vs. Frequency & Supply Voltage



Intercept vs. Frequency



[1] CW input waveform.



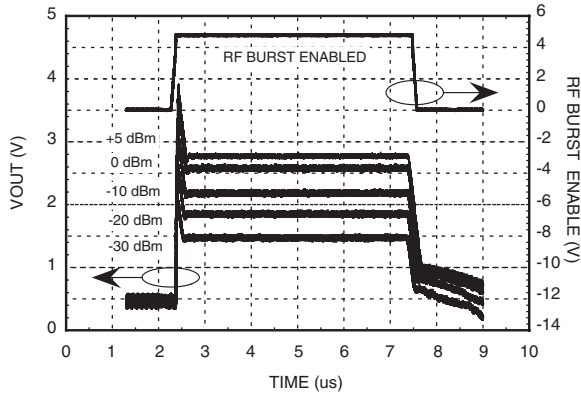
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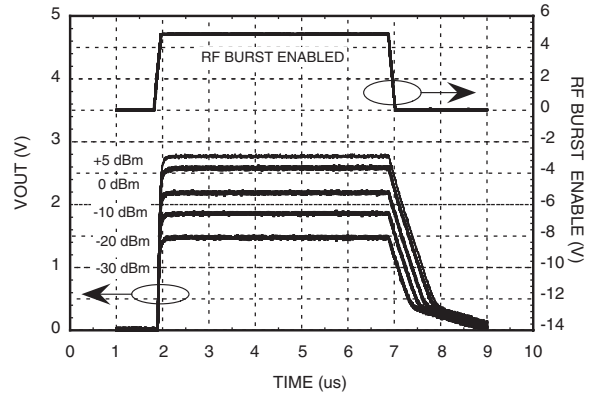
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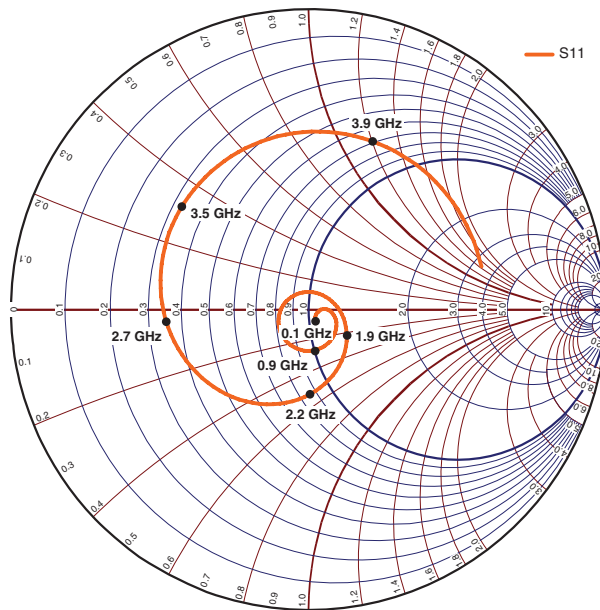
Output Response to RF Burst Input @ 1900 MHz, CINT (C17) = Open



Output Response to RF Burst Input @ 1900 MHz, CINT (C17) = 0.1 μF



Input Impedance vs Frequency, 100 MHz - 3.9 GHz [1]



[1] Reference plane at J1 connector on evaluation board.



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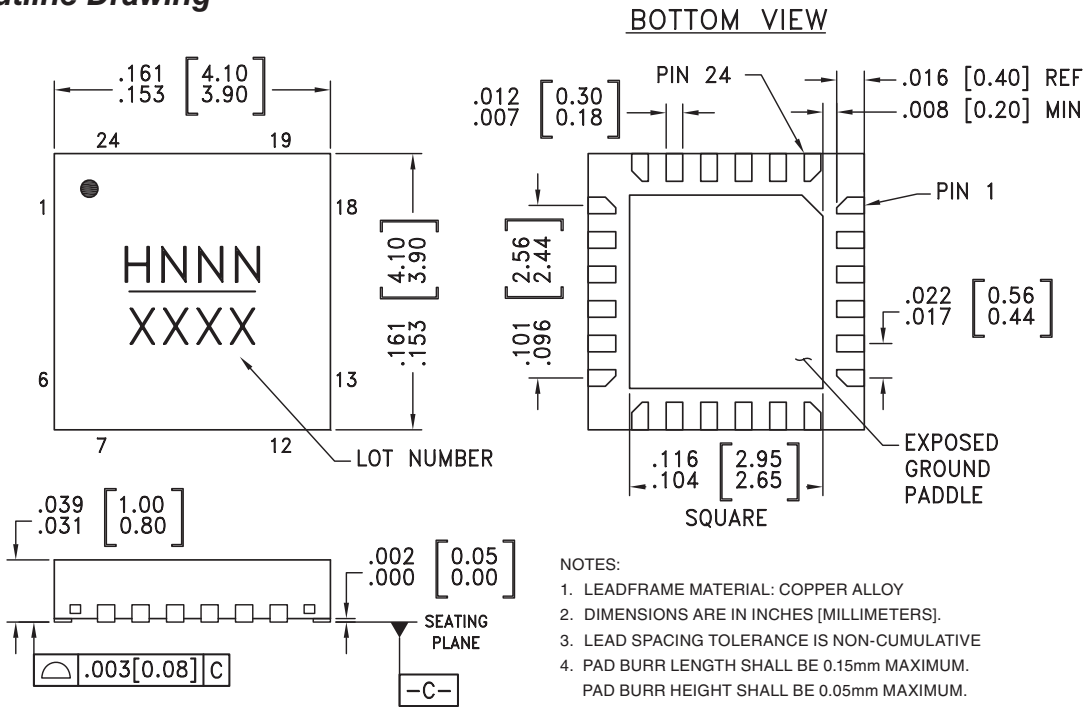
Absolute Maximum Ratings

Supply Voltage	5.6V
RF Input Power	20 dBm
Equivalent Voltage	2.25 Vrms
Channel / Junction Temperature	125 °C
Continuous P _{diss} (T = 85°C) (Derate 22.72 mW/°C above 85°C)	0.91 Watts
Thermal Resistance (R _{thj}) (junction to ground paddle)	44.02 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

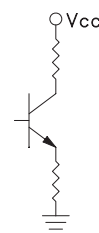

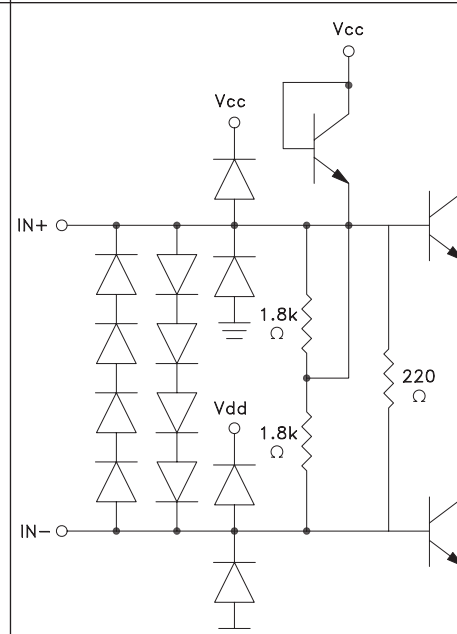
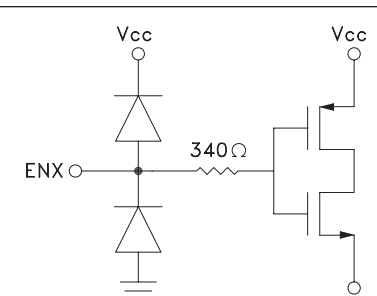
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC610LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 ^[1]	H610 XXXX
HMC610LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H610 XXXX

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

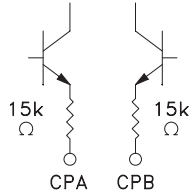
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 8, 11, 21	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	
2, 5, 12, 13, 16, 18, 24	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3, 4	IN+, IN-	RF Input pins. Connect RF to IN+ and IN- through a 1:1 balun.	
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage $V > 0.8 V_{dd}$ will initiate power saving mode.	

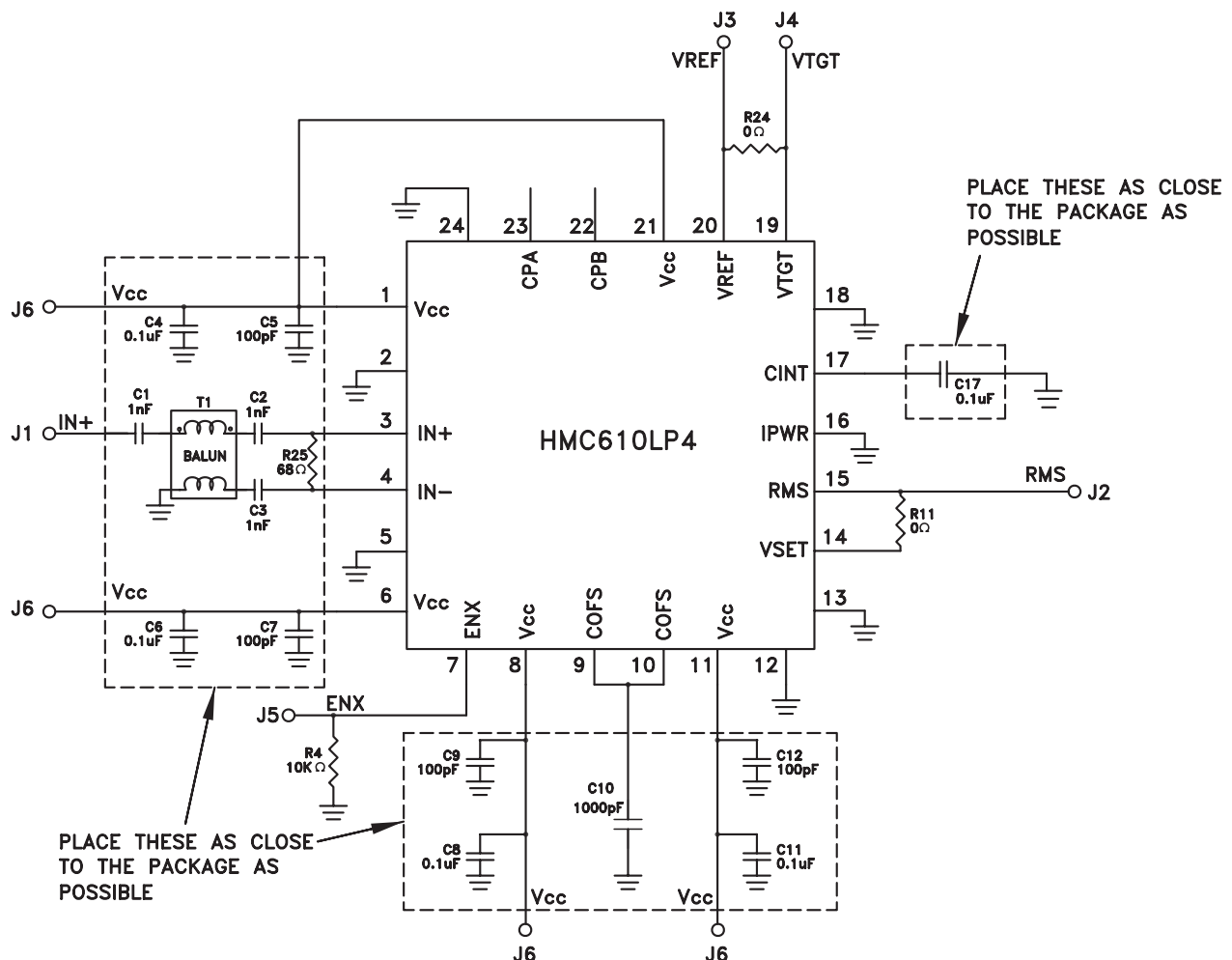
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
9, 10	COFS	Input high pass filter capacitor. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter.	
14	VSET	VSET input. Short this pin to RMSOUT for normal operation. Use a resistor between RMSOUT and VSET to increase the logarithmic slope.	
15	RMSOUT	Logarithmic output that converts the input power to a DC level. Short this pin to VSET for normal operation.	
16	IPWR	Ground for proper operation	
17	CINT	Connection for ground referenced loop filter integration capacitor.	
19	VTGT	This voltage input changes the logarithmic intercept point. Use of lower target voltage reduces error for complex signals with large crest factors. Normally connected to VREF.	
20	VREF	Reference voltage output.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
22, 23	CPB, CPA	Temperature compensation pins. Leave both pins floating for normal operation.	

Application & Evaluation PCB Schematic





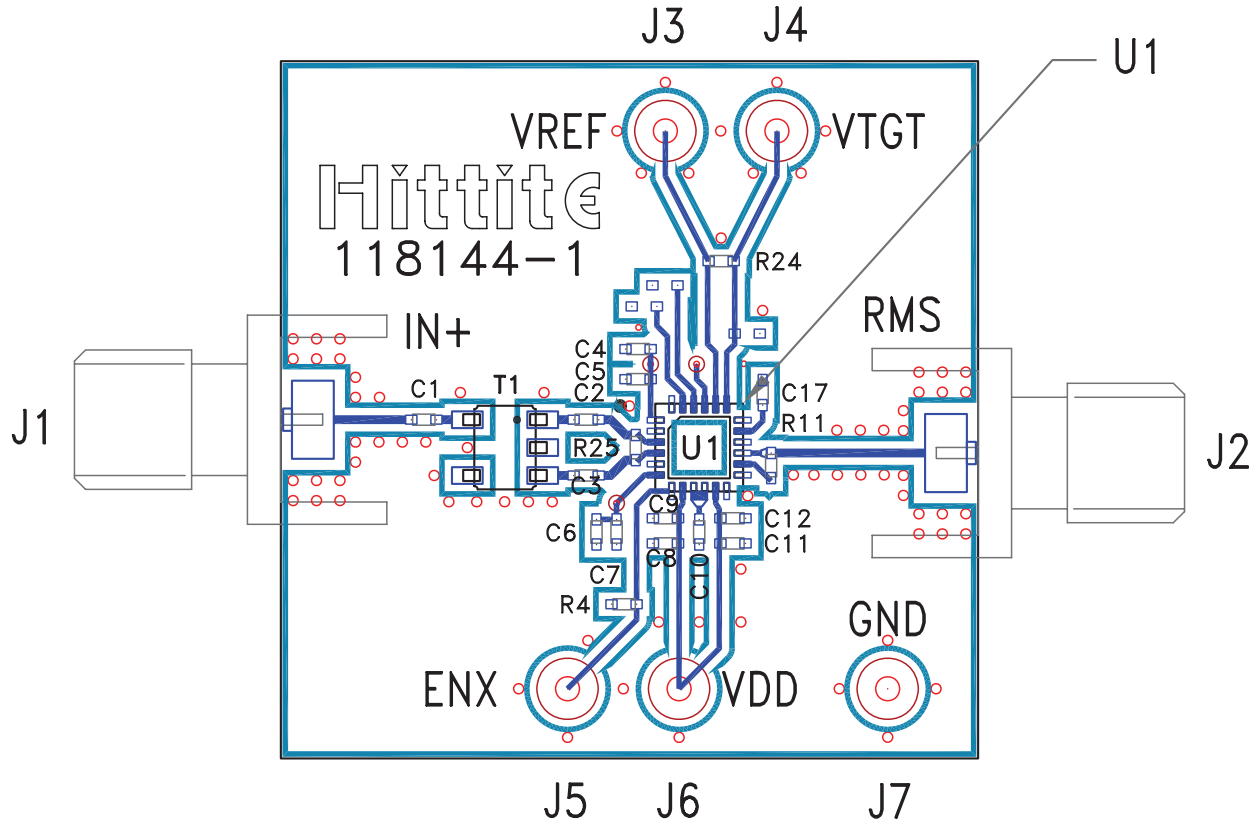
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Evaluation PCB



List of Materials for Evaluation PCB 118147 [1]

Item	Description
J1 - J2	PC Mount SMA connector
J3 - J7	DC Pins
C1 - C3	1 nF Capacitor, 0402 Pkg.
C4, C6, C8, C11, C17	0.1 μ F Capacitor, 0402 Pkg.
C5, C7, C9, C12	100 PF Capacitor, 0402 Pkg.
C10	1000 PF Capacitor, 0402 Pkg.
R25	68 Ω Resistor, 0402 Pkg.
R11, R24	0 Ω Resistor, 0402 Pkg.
R4	10k Ω Resistor, 0402 Pkg.
T1	1:1 Balun, M/A-COM ETC1-1-13
U1	HMC610LP4 / HMC610LP4E Logarithmic Detector / Controller
PCB [2]	118144 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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Notes