Unit: mm



TOSHIBA Diode Silicon Epitaxial Planar Type

HN1D01F

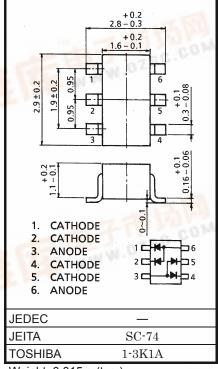
Ultra-High-Speed Switching Applications

Small package

Low forward voltage : V_F(3) = 0.92 V (typ.)
 Fast reverse recovery time: t_{rr} = 1.6 ns (typ.)
 Small total capacitance : C_T = 2.2 pF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Maximum (peak) reverse voltage	V_{RM}	85	V	
Reverse voltage	V_{R}	80	V	
Maximum (peak) forward current	I _{FM}	300 (*)	mA	
Average forward current	IO	100 (*)	mA	
Surge current (10 ms)	I _{FSM}	2 (*)	Α	
Power dissipation	Р	300 (*)	mW	
Junction temperature	Tiere (125	°C	
Storage temperature	T _{stg}	-55~125	°C	



Weight: 0.015 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in

temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

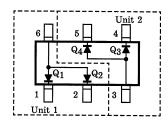
(*) These are the Absolute Maximum Ratings for a single diode (Q1 or Q2 or Q3 or Q4). If Unit 1 and Unit 2 are used independently or simultaneously, the Absolute Maximum Ratings per diode are 75% of those of a single diode.

Electrical Characteristics (Q₁, Q₂, Q₃, Q₄ Common, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit	
Forward voltage	V _{F (1)}	_	I _F = 1 mA		0.61	150	Tre -	
	V _{F (2)}	_	I _F = 10 mA	- 4	0.74	_	V	
	V _{F (3)}	-	I _F = 100 mA	_	0.92	1.20		
Reverse current	I _{R (1)}	1076	V _R = 30 V	_	_	0.1		
	I _{R (2)}	_	V _R = 80 V	_	_	0.5	μA	
Total capacitance	C _T	_	V _R = 0, f = 1 MHz	_	2.2	4.0	pF	
Reverse recovery time	t _{rr}	_	I _F = 10 mA (Fig. 1)	_	1.6	4.0	ns	



Pin Assignment (Top View)



Marking

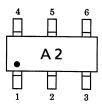
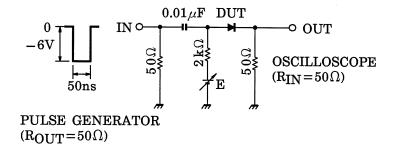
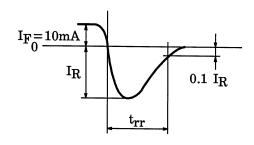


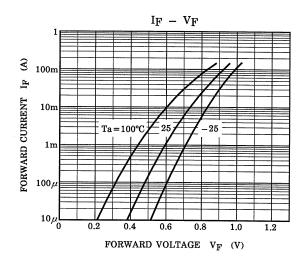
Fig. 1. Reverse Recovery Time (t_{rr}) Test Circuit

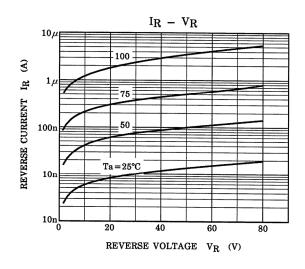
INPUT WAVEFORM

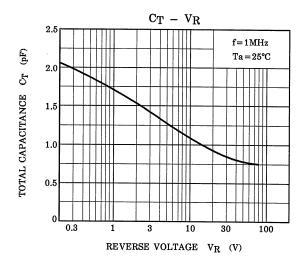


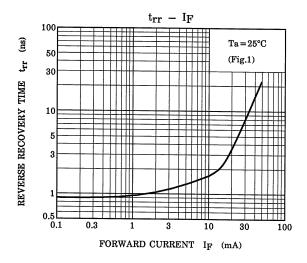
OUTPUT WAVEFORM











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20070701-EN GENERAL

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