Agilent Technologies
Innovating the HP Way

Silicon Bipolar RFIC 100 MHz Vector Modulator

Technical Data

HPMX-2005

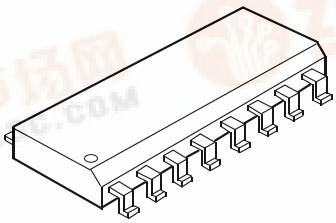
Features

- 25 - 250 MHz Output Frequency
- -5 dBm Peak P_{out}
- Unbalanced 50 Ω Ouptut Match
- Internal 90° Phase Shifter
- 5 V, 15 mA Bias
- SO-16 Surface Mount Package

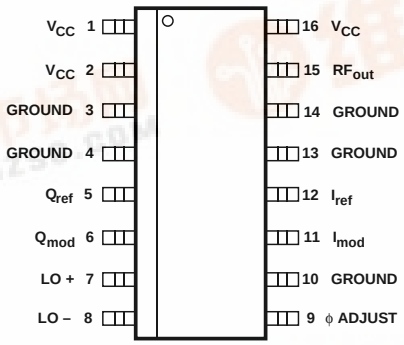
Applications

- Dual Conversion Cellular Telephone and PCS Handsets
- Dual Conversion ISM Band Transmitters and LANs
- Direct Conversion Digital Transmitters for 25-250 MHz

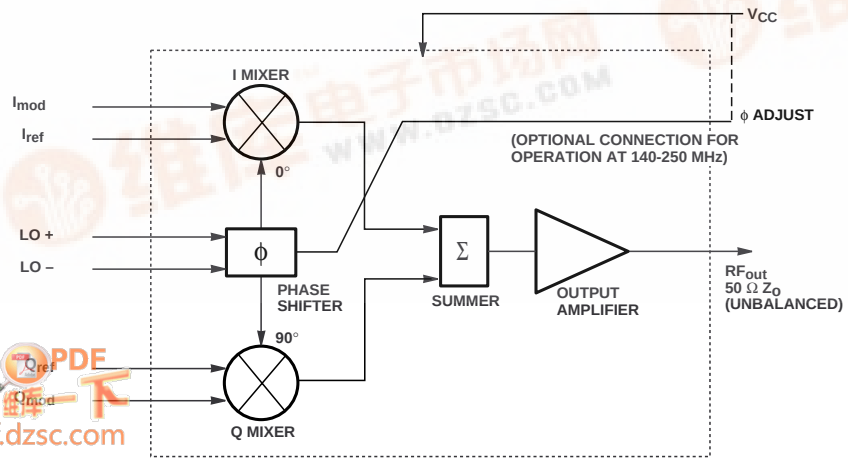
Plastic SO-16 Package



Pin Configuration



Functional Block Diagram



Description

Agilent's HPMX-2005 is a silicon RFIC vector modulator housed in a SO-16 surface mount plastic package. This IC can be used for direct modulation at output frequencies from 25 to 250 MHz, or, in combination with an up-converting mixer, for dual or multiple conversion modulation to higher frequencies. The IC contains two matched Gilbert cell mixers, an RC phase shifter, a summer, and an output amplifier.

This RFIC is well suited to portable and mobile cellular telephone applications such as North American Digital Cellular, GSM, and Japan Digital Cellular, and to Personal Communications Systems such as DCS-1800 or handyphones. It is also useful for applications in 900 MHz, 2.4 GHz and 5.7 GHz ISM (Industrial-Scientific-Medical) bands requiring digital modulation, such as Local Area Networks (LANs).

The HPMX-2005 is fabricated with Agilent's 25 GHz ISOSAT-II process, which combines stepper lithography, self-alignment, ion-implantation techniques, and gold metallization to produce state of the art RFICs.

HPMX-2005 Absolute Maximum Ratings, T_A = 25°C

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation [2,3]	mW	500
LO_{in}	LO Input Power	dBm	15
V_{CC}	Supply Voltage	V	10[4]
ΔV_{Imod}, ΔV_{Qmod}	Swing of V_{Imod} about V_{Iref} or V_{Qmod} about V_{Qref}	V_{p-p}	5[4]
V_{Iref}, V_{Qref}	Reference Input Levels	V	5
T_{STG}	Storage Temperature	°C	-65 to 150
T_j	Junction Temperature	°C	150

Thermal Resistance[2]:
θ_{jc} = 125°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_C = 25°C (T_C is defined to be the temperature at the ends of pin 3 where it contacts the circuit board).
3. Derate at 8 mW/°C for T_C > 87°C.
4. This voltage must not exceed V_{CC} by more than 0.8 V.

HPMX-2005 Guaranteed Electrical Specifications, T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 100 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_d	Device Current	mA		14	17
P_{out}	Output Power V_{Imod} = V_{Qmod} = 3.25 V	dBm	-7	-5	
LO_{leak}	P_{out} - LO at Output V_{Imod} = V_{Qmod} = 2.5 V	dBc	30	36	
ε_{mod}	Average Modulation Error $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2} = 0.75$ V	%		2.5	5

HPMX-2005 Summary Characterization Information. T_A = 25°C, Z_O = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 100 MHz (Unbalanced Input), V_{Iref} = V_{Qref} = 2.5 V (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Typ.
R_{in}	Input Resistance (I_{mod} to I_{ref} or Q_{mod} to Q_{ref})	Ω	10 k
R_{in-gnd}	Input Resistance to Ground (Any I, Q Input to Ground)	Ω	10 k
$VSWR_{LO}$	LO VSWR (50 Ω) 25 - 200 MHz Bandwidth		1.5:1
$VSWR_O$	Output VSWR (50 Ω) 25 - 200 MHz Bandwidth		2.5:1
-	Output Noise Floor V_{Imod} = V_{Qmod} = 3.25 V	dBm/Hz	-134
IM_3	DSB Third Order Intermodulation Products	dBc	33
A_i	RMS Amplitude Error	dB	0.15
P_i	RMS Phase Error	degrees	1.0

HPMX-2005 Pin Descriptions

V_{CC} (pins 1, 2 & 16)

These three pins provide DC power to the RFIC, and are connected together internal to the package. They should be connected to a 5 V supply, with appropriate AC bypassing (1000 pF typ.) used near the pins, as shown in figures 1 and 2.**The voltage on these pins should always be kept *at least 0.8 V more positive* than the DC level on any of pins 5, 6, 11, or 12.** Failure to do so may result in the modulator drawing sufficient current through the data or reference inputs to damage the IC (see also Figure 5).

Ground (pins 3, 4, 10, 13 & 14)

These pins should connect with minimal inductance to a solid ground plane (usually the backside of the PC board). Recommended assembly employs multiple plated through via holes where these leads contact the PC board.

I_{ref} (pin 12) and Q_{ref} (pin 5) I_{mod} (pin 11) and Q_{mod} (pin 6) Inputs

The I and Q inputs are designed for unbalanced operation but can be driven differentially with similar performance. The recommended level of unbalanced I and Q signals is 1.5 V_{p-p} with an average level of 2.5 V above ground. The reference pins should be DC biased to this average data signal level (V_{CC}/2 or 2.5 V typ.). For single ended drive, pins 5 and 12 can be tied together. For differential operation, 0.75 V_{p-p} signals may be applied across the I_{mod}/I_{ref} and the Q_{mod}/Q_{ref} pairs. The average level of all four signals should be about 2.5 V above ground. The impedance between I_{in} or Q_{in} and ground is typically 10 kΩ and the impedance between I_{mod} and I_{ref} or Q_{mod} and Q_{ref} is typically 10 kΩ. The input bandwidth typically exceeds 40 MHz. It is possible to reduce LO leakage through the IC by applying slight DC imbalances between I_{mod} and I_{ref} and/or Q_{mod} and Q_{ref} (see page 9). All performance data shown on this data sheet was taken with unbalanced I/Q inputs.

LO Input (pins 7 and 8)

The LO input of the HPMX-2005 is balanced (differential) and matched to 50 Ω. For drive from a unbalanced LO, pin 7 should be AC coupled to the LO using a 50 Ω transmission line and a blocking capacitor (1000 pF typ.), and pin 8 should be AC grounded (1000 pF capactitor typ.), as shown in figure 1. For drive from a differential LO source, 50 Ω transmission lines and blocking capacitors (1000 pF typ.) are used on both pins 7 and 8, as shown in figure 2. The internal phase shifter allows operation from 25 to 200 MHz (or to 250 MHz by using pin 9 — see below). The recommended LO input level is -12 dBm. All performance data shown on this data sheet was taken with unbalanced LO operation.

Phase Adjust (pin 9)

Applying a DC bias to this pin alters the frequency range of the internal RC phase shifter. In normal operation, this pin is not connected. (Do not ground this pin!) For operation at LO frequencies above 140 MHz, superior modulation error can be achieved by connecting pin 9 to V_{CC} (5 V). The resulting changes in performance are shown in figures 13 through 18. Use of pin 9 extends the operating range to beyond 250 MHz.

RF Output (pin 15)

The RF output of the HPMX-2005 is configured for unbalanced operation, and connects directly to an emitter follower in the output stage of the IC. The output impedance is appropriate for connection without further impedance matching to transmission lines of characteristic impedance between 50 Ω and 150 Ω. The reflection coefficients are given in figure 11. A DC blocking capacitor (1000 pF typ.) is required on this pin.

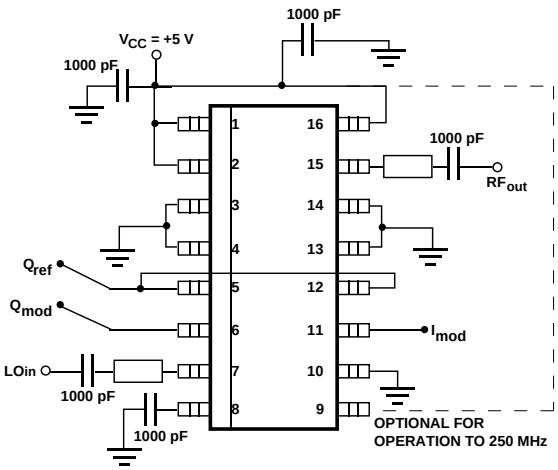


Figure 1. HPMX-2005 Connections Showing Unbalanced LO and I/Q Inputs.

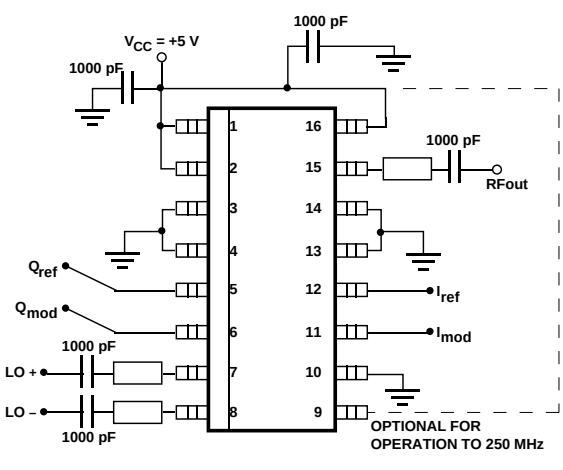


Figure 2. HPMX-2005 Connections Showing Differential LO and I/Q Inputs.

HPMX-2005 Typical Data Measurement

Direct measurement of the amplitude and phase error at the output is the most accurate way to evaluate modulator performance. By measuring the error directly, all the harmonics, LO leakage, etc. that show up in the output signal are accounted for. Figure 3 below shows the test setup that was used to create the amplitude and phase error plots (figures 19 and 21).

Amplitude and phase error are measured by using the four channel power supply to simulate I and Q input signals. Real 1.5 V_{p-p} I and Q signals would swing 0.75 volts above and below an average 2.5 V level, therefore, a logic "high" level input is simulated by applying 3.25 V, and a logic "low" level by applying 1.75 V to the I and/or Q inputs.

Amplitude and phase are measured by setting the network analyzer for an S_{21} measurement at the center frequency of choice. Set the port 1 stimulus level to the LO level you intend to use in your circuit (-12 dBm for the data sheet).

By adjusting the V_i and V_q settings you can step around the I/Q vector circle, reading magnitude and phase at each point. The relative values of phase and gain (amplitude) at the various points will indicate the accuracy of the modulator. Note: you must use very low ripple power supplies for the reference, V_{Imod}, and V_{Qmod} supplies. Ripple or noise of only a few millivolts will appear as wobbling phase readings on the network analyzer.

The same test setup shown below is used to measure input and output VSWR, reverse isolation, and power vs. frequency. V_{Imod} and V_{Qmod} are set to 3.25 V and the appropriate frequency ranges are swept. S_{11} provides input VSWR data, S_{22} provides output VSWR data and S_{12} provides reverse isolation data. S_{21} provides power output (add the source power to the S_{21} derived gain).

LO leakage data shown in figure 17 is generated by setting V_{Imod} = V_{Qmod} = V_{Iref} = V_{Qref} = 2.5 volts then performing an S_{21} sweep. Since phase is not important for these measurements, a scalar network analyzer or a signal generator and spectrum analyzer could be used.

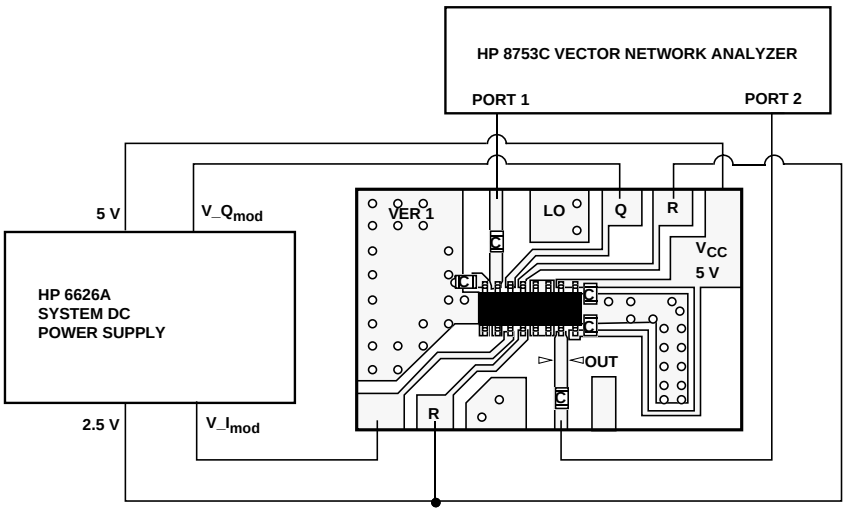


Figure 3: Test Setup for Measuring Amplitude and Phase Error, Input and Output VSWR, Reverse Isolation and LO Leakage of the Modulator.

HPMX-2005 Typical Performance

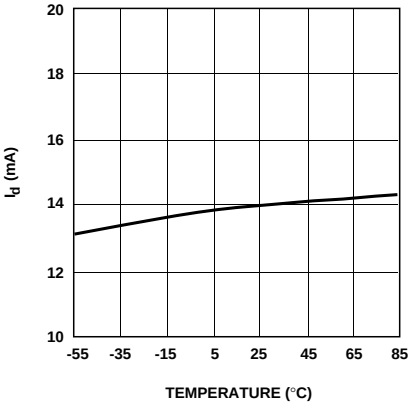


Figure 4. HPMX-2005 Device Current vs. Temperature. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

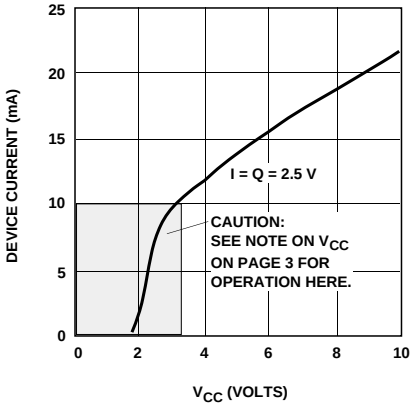


Figure 5. HPMX-2005 Device Current vs. Voltage. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

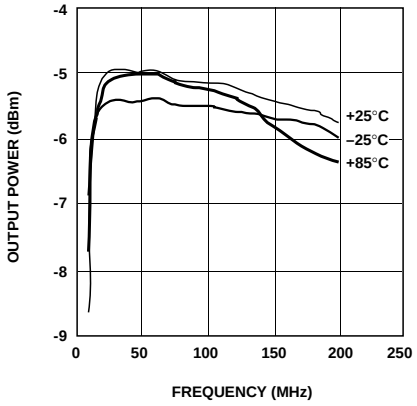


Figure 6. HPMX-2005 Power Output vs. Frequency and Temperature. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V.

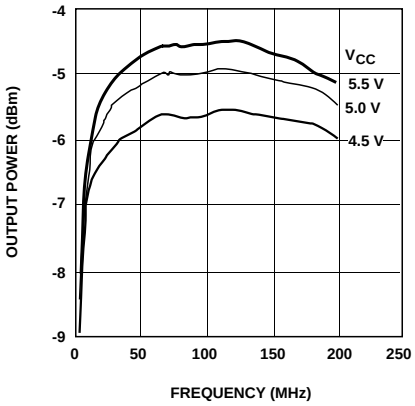


Figure 7. HPMX-2005 Power Output vs. Frequency and Supply Voltage. LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

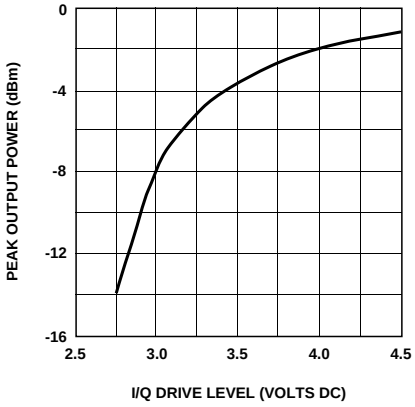


Figure 8. HPMX-2005 Power Output vs. I/Q Drive Level at 100 MHz. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod}, T_A = 25°C.

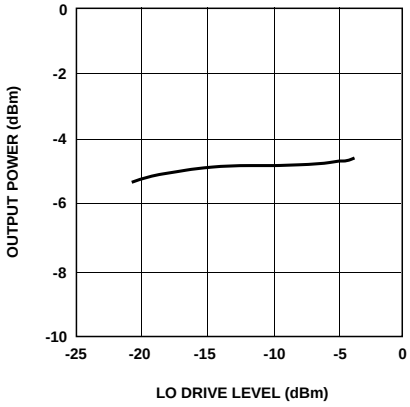


Figure 9. HPMX-2005 Power Output vs. LO Drive Level at 100 MHz. V_{CC} = 5 V, V_{Iref} = V_{Qref} = 2.5 V, V_{Imod} = V_{Qmod} = 3.25 V, T_A = 25°C.

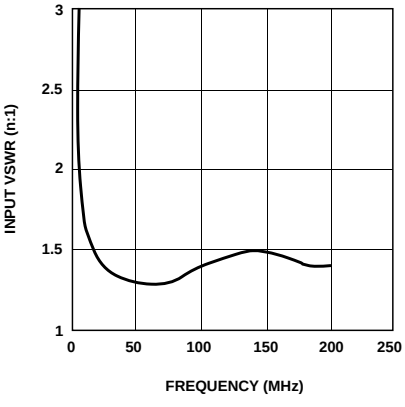


Figure 10. HPMX-2005 LO VSWR vs. Frequency. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

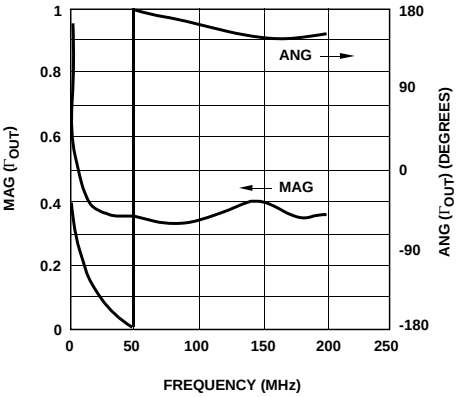


Figure 11. HPMX-2005 Output Reflection Coefficient vs. Frequency. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

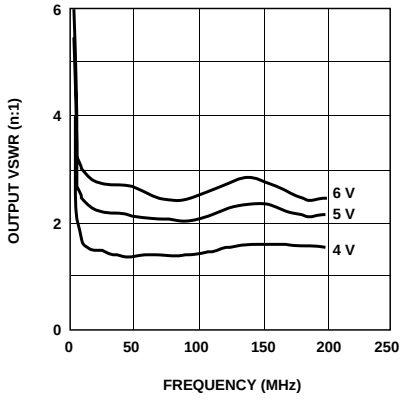


Figure 12. HPMX-2005 Output VSWR vs. Frequency and Supply Voltage. LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

HPMX-2005 Typical Performance Using Phase Adjust

The HPMX-2005 has an internal phase shifter that in normal use (pin 9 open circuited) operates over a frequency range of 25 to 200 MHz. By applying 5 volts to pin 9, this frequency range can be raised to beyond 250 MHz. This page shows HPMX-2005 modulator performance with pin 9 tied to V_{CC} = 5 V for higher frequency operation. Using the Φ adjust has minimal effect on the VSWRs at the LO port.

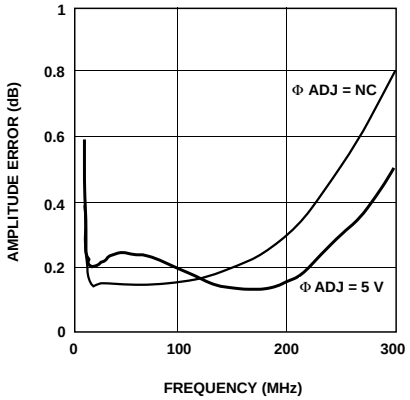


Figure 13. HPMX-2005 RMS Amplitude Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

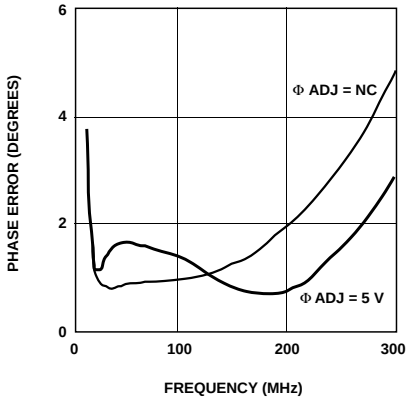


Figure 14. HPMX-2005 RMS Phase Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

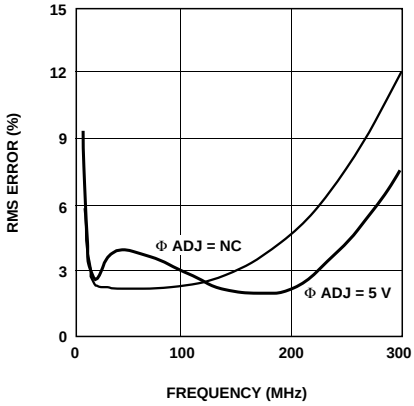


Figure 15. HPMX-2005 RMS Modulation Error vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C.

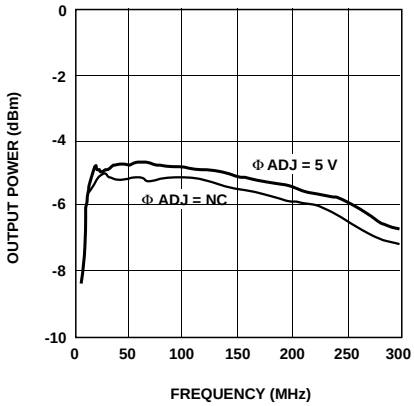


Figure 16. HPMX-2005 Output Power vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $V_{Imod} = V_{Qmod}$ = 3.25 V, T_A = 25°C.

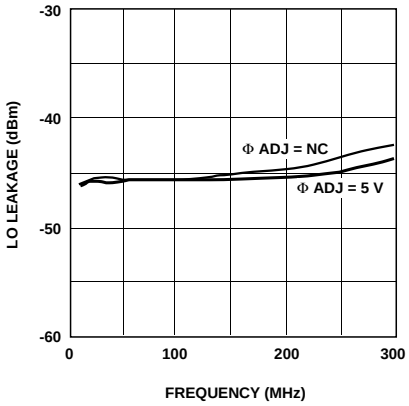


Figure 17. HPMX-2005 LO Leakage vs. Frequency and Φ Adjust. V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref} = V_{Imod} = V_{Qmod}$ = 2.5 V, T_A = 25°C.

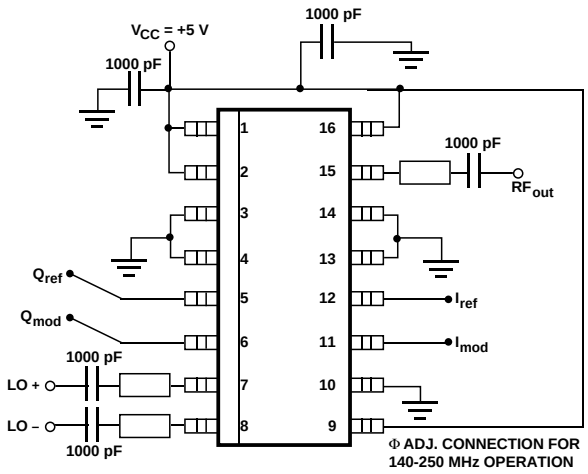


Figure 18. Connection of Pin 9 for Operation of the HPMX-2005 at Frequencies Between 140 MHz and 250 MHz.

HPMX-2005 Modulation Accuracy (Sample Part)

V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, $\sqrt{(V_{Imod} - 2.5)^2 + (V_{Qmod} - 2.5)^2}$ = 0.75 V, T_A = 25°C (unless otherwise noted).

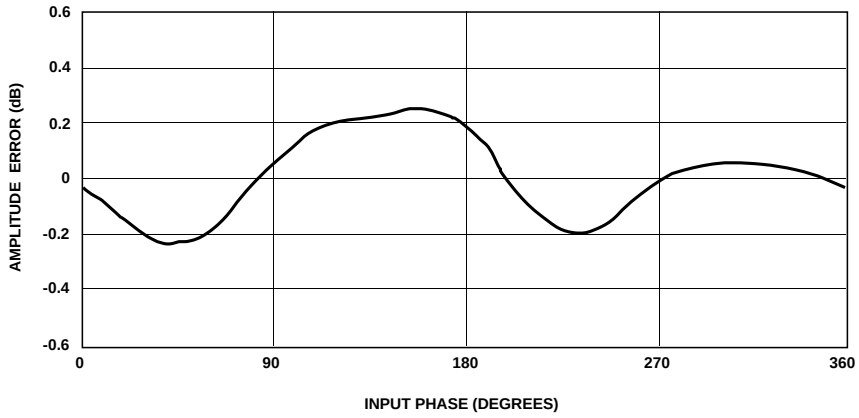


Figure 19. HPMX-2005 RMS Amplitude Error vs. Input Phase at 100 MHz.

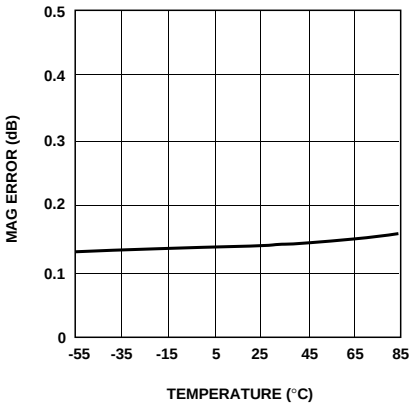


Figure 20. HPMX-2005 RMS Amplitude Error at 100 MHz vs. Temperature.

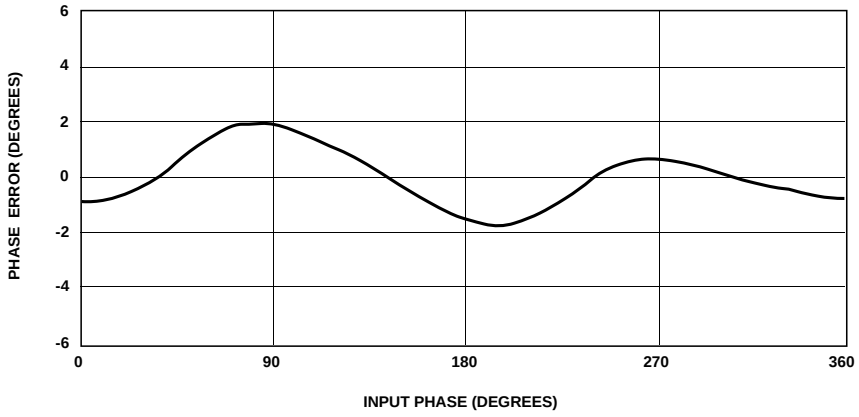


Figure 21. HPMX-2005 Phase Error vs. Input Phase at 100 MHz.

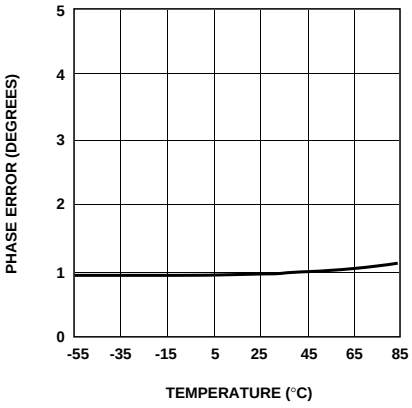


Figure 22. HPMX-2005 RMS Phase Error at 100 MHz vs. Temperature.

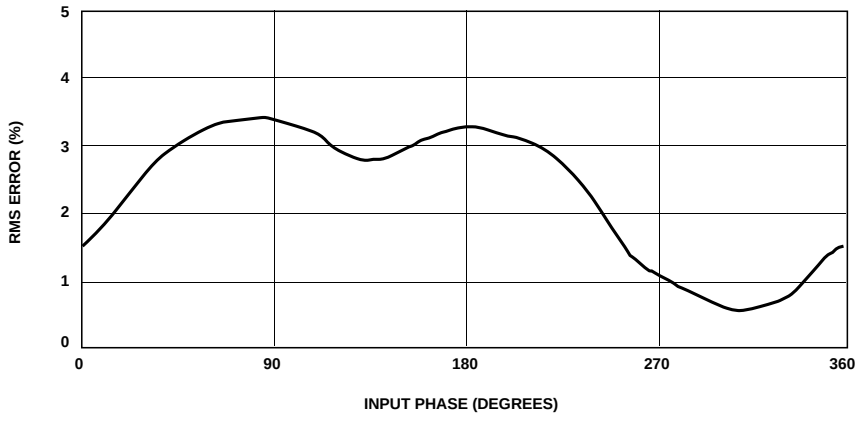


Figure 23. HPMX-2005 RMS Modulation Error vs. Input Phase at 100 MHz. This value is calculated from the values of amplitude and phase error.

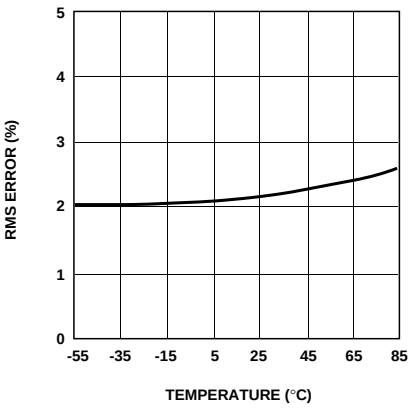


Figure 24. HPMX-2005 RMS Modulation Error at 100 MHz vs. Temperature.

HPMX-2005 Single and Double Sideband Performance

Single sideband (SSB) and double sideband (DSB) tests are sometimes used to evaluate modulator performance. Typical SSB and DSB output spectrum graphs for the HPMX-2005 are shown in figures 25 and 26 below. Figure 27 shows the test equipment setup used to generate this information.

For accurate measurements of modulator performance and LO suppression, the phase shift provided by the I and Q signal generators must be very close to 90 degrees and the amplitude of the two signals must be matched to within a few millivolts. The I,Q signal generator must put out low distortion signals or the spectrum analyzer will show high harmonic levels that reflect the performance of the signal generator, not the modulator.

HPMX-2005 Typical Sideband Performance Data

V_{CC} = 5 V, LO = -12 dBm, $V_{Iref} = V_{Qref}$ = 2.5 V, $V_{Imod} = V_{Iref}$ + 0.75 V $\sin(2\pi f_n t)$, $V_{Qmod} = V_{Qref}$ + 0.75 V $\cos(2\pi f_n t)$ for SSB, $V_{Imod} = V_{Qmod} = V_{Qref}$ + 0.75 V $\cos(2\pi f_n t)$ for DSB, f_n = 25 kHz, T_A = 25°C

Symbol	Parameters and Test Conditions	Units	SSB	DSB
P_{LSB}	Lower Sideband Power Output	dBc	-8	-11
LO_{leak}	LO Suppression	dBc	33	30
P_{USB}	Upper Sideband Power Output	dBm	-38	-11
IM_3	3rd Order Intermodulation Distortion Level	dBc	NA	33

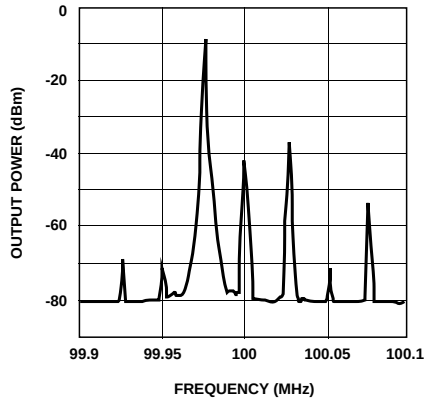


Figure 25. Single Sideband Output Spectrum.

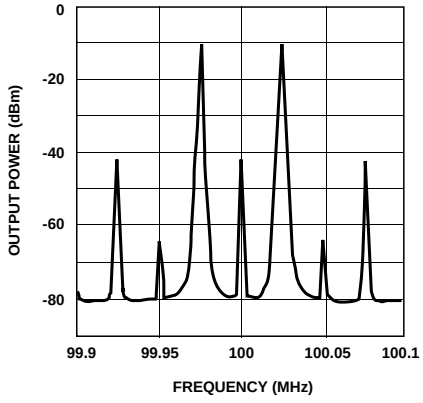


Figure 26. Double Sideband Output Spectrum.

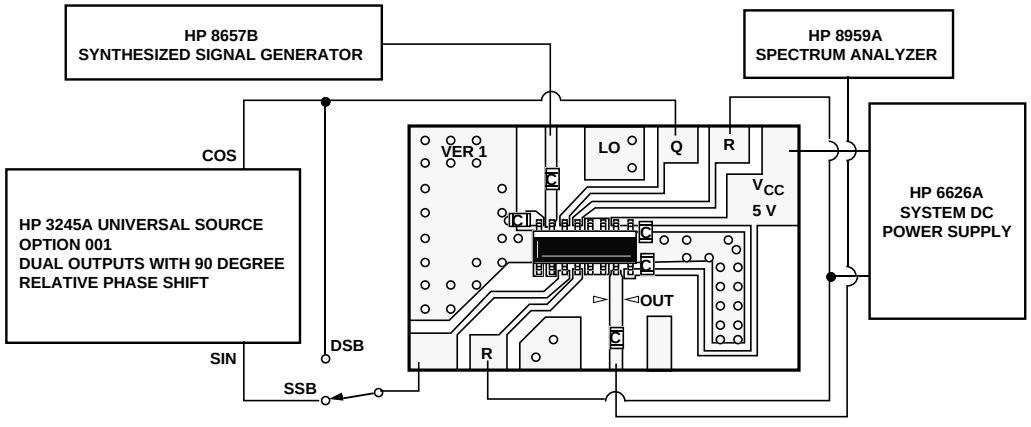


Figure 27. HPMX-2005 Single/Double Sideband Test Setup.

HPMX-2005 Using Offsets to Improve LO Leakage

It is possible to improve on the excellent performance of the HPMX-2005 for applications that are particularly sensitive to LO leakage. The amount and nature of the improvement are best understood by examining figures 28 and 29, below.

LO leakage results when normal variations in the wafer fabrication process cause small shifts in the values of the modulator IC's internal components. These random variations create an effect equivalent to slight DC imbalances at the input of each (I and Q) mixer. The DC imbalances at the mixer inputs are multiplied by ±1 at the LO frequency and show up at the output of the IC as LO leakage.

It is possible to externally apply small DC signals to the I and Q inputs and exactly cancel the internally generated DC offsets. This will result in sharply decreased LO leakage at precisely the frequency and temperature where the offsets were applied (see figure 28).

This improvement is not very useful if it doesn't hold up over frequency and temperature changes. The lower curve in figure 28 shows how the offset-adjusted LO leakage varies versus frequency. Note that it remains below -60 dBm over most of the frequency range shown. In the 20 MHz range centered at 100 MHz, the level is closer to -70 dBm.

Figure 29 shows the performance of the offset adjusted LO leakage over temperature. Note that the adjusted curve is at a level near -70 dBm over the entire temperature range.

The net result of using externally applied offsets with the HPMX-2005 is that an LO leakage level below -50 dBm can typically be achieved over both frequency and temperature.

The magnitude of the required external offset varies randomly from part to part and between the I and Q mixers on any given IC. Offsets can range from -35 mV to +35 mV. External offsets may be applied either by varying the average level of the I and Q modulating signals, or by varying the voltages at the I_{ref} and Q_{ref} pins of the modulator.

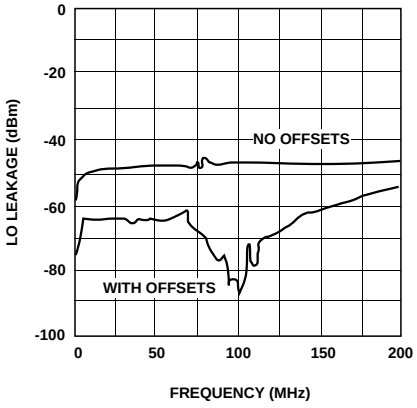


Figure 28. LO Leakage vs. Frequency Without DC Offsets and LO Leakage vs. Frequency with DC Offsets Adjusted for Minimum LO Leakage at 100 MHz. V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V, T_A = 25°C.

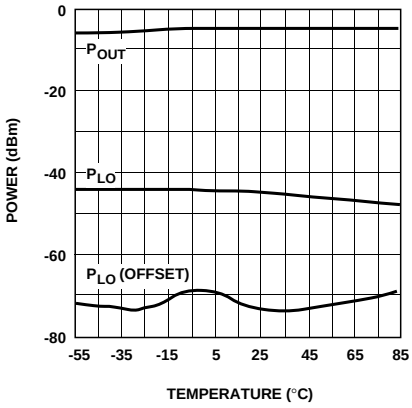


Figure 29. LO Leakage with No DC Offsets at 100 MHz vs. Temperature (Upper Curve) and LO Leakage with DC Offsets Adjusted for Minimum Leakage at 25°C vs. Temperature (Lower Curve). V_{CC} = 5 V, LO = -12 dBm, V_{Iref} = V_{Qref} = 2.5 V.

HPMX-2005 Modulation Spectrum Diagrams

Figure 30, below, shows the test set-up that was used to generate the GSM, JDC and NADC modulation spectrum diagrams that appear on the following page. The major differences between these tests are summarized in the table below.

The modulation spectra are created by setting the function generator to the appropriate bit-clock frequency. The pattern generator is set to produce a pseudorandom serial bit stream (n = 20) that is NRZ coded. The pseudorandom bit stream which simulates the serial data in a digital phone is fed to the base-band processor that splits it into a two bit parallel stream (I and Q) and then filters each according to the requirements of the digital telephone system being simulated. The I and Q signals from the baseband filter are then DC offset by 2.5 V using the op-amp circuit. The output of the modulator is monitored using a spectrum analyzer.

System	Bit Clock Frequency	Baseband Filter	Channel (LO) Frequency
GSM	270 kHz	0.3 GMSK (HP-8657B)	900 MHz
JDC	42 kHz	α = 0.5 π/4 DQPSK (HP-8657D)	950 MHz
NADC	48.6 kHz	α = 0.35 π/4 DQPSK (HP-8657D)	835 MHz

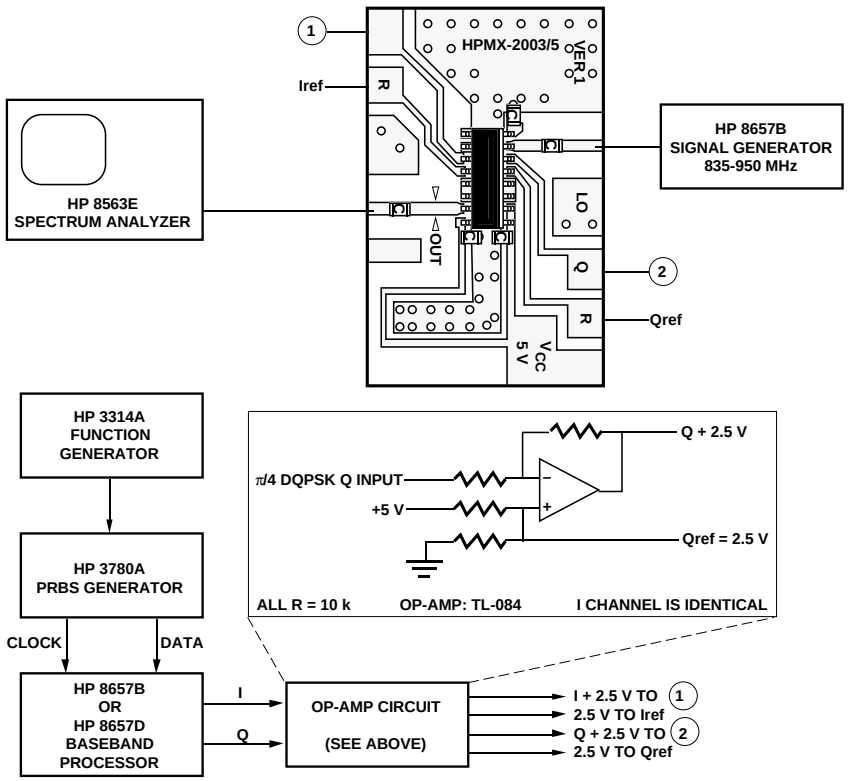


Figure 30. Test Equipment Setup for Modulation Spectrum Diagrams.

HPMX-2005 Cellular Telephone Modulation Spectrum Performance

T_A = 25°C (unless otherwise noted)

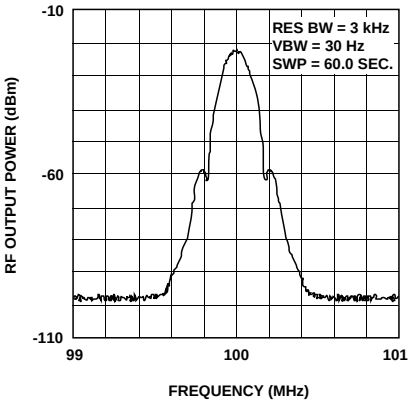


Figure 31. HPMX-2005 GSM Modulation Spectrum at -40°C.

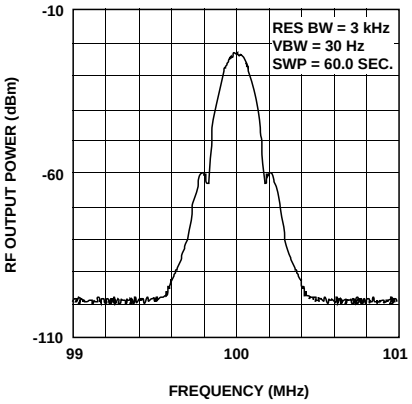


Figure 32. HPMX-2005 GSM Modulation Spectrum at 25°C.

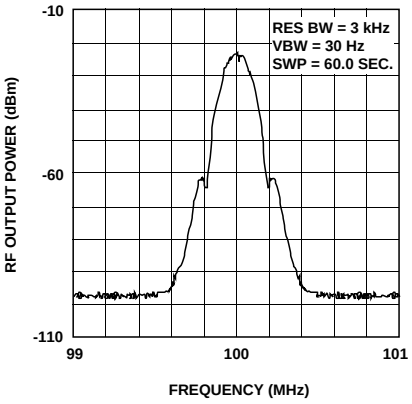


Figure 33. HPMX-2005 GSM Modulation Spectrum at 85°C.

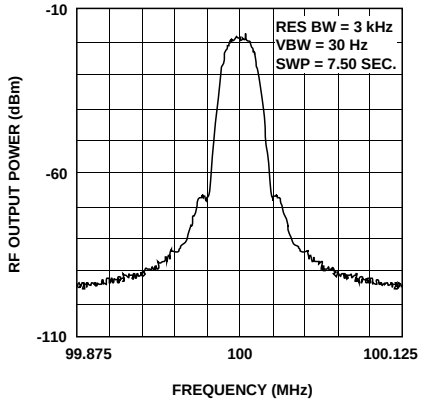


Figure 34. HPMX-2005 JDC Modulation Spectrum at -40°C.

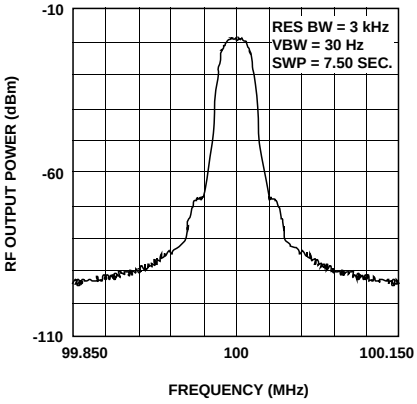


Figure 35. HPMX-2005 JDC Modulation Spectrum at 25°C.

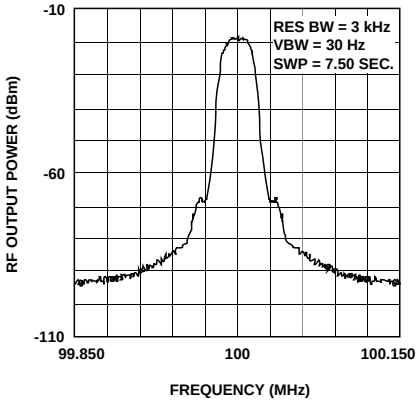


Figure 36. HPMX-2005 JDC Modulation Spectrum at 85°C.

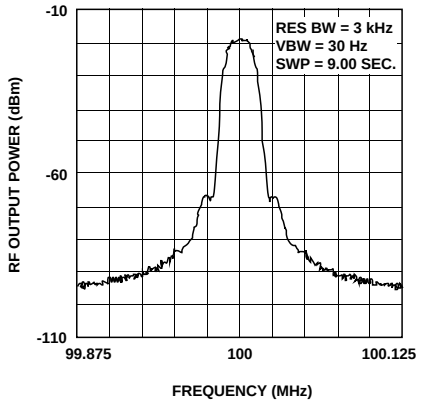


Figure 37. HPMX-2005 NADC Modulation Spectrum at -40°C.

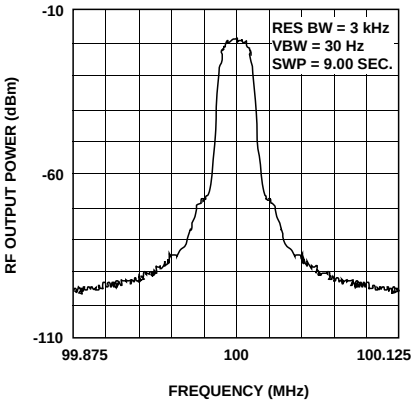


Figure 38. HPMX-2005 NADC Modulation Spectrum at 25°C.

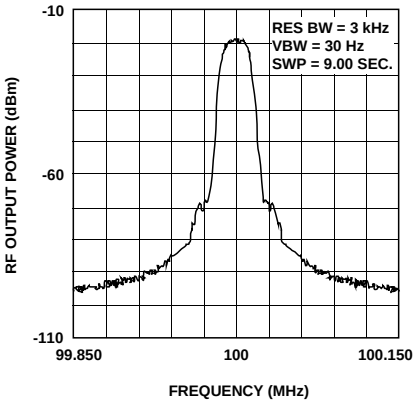


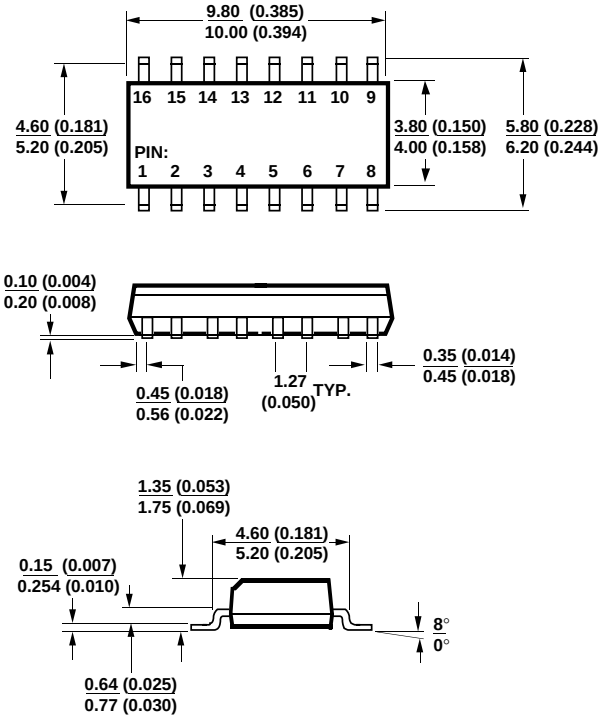
Figure 39. HPMX-2005 NADC Modulation Spectrum at 85°C.

Agilent Technologies
Innovating the HP Way

Part Number Ordering Information

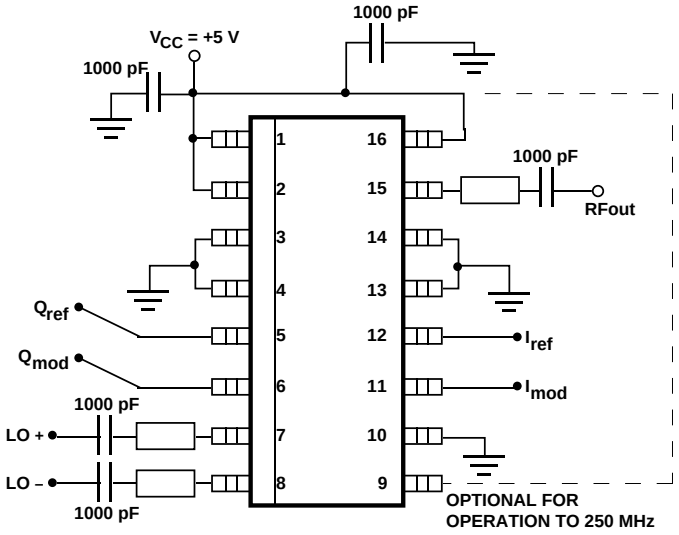
Part Number	Option	No. of Devices	Container
HPMX-2005		25 Min.	Tube
HPMX-2005	T10	1000	7" Reel

Package Dimensions
SO-16 Package



NOTE: DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPMX-2005 Test Board Layout



Finished board size 1.5" x 1" x 1/32"

Material: 1/32" epoxy/fiberglass, 1 oz. copper, both sides, fused tin/lead coating, both sides.

Note: white "+" marks indicate drilling locations for plated-through via holes to the groundplane on the bottom side of the board.

www.semiconductor.agilent.com

Obsoletes 5091-7968E
5965-9104E (11/99)