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HEWLETT PACKARD

Infrared IrDA® Compliant Transceiver

Technical Data

HSDL-2100

Features

- Small Module Package
  - height of 5.5 mm max.
- Integrated EMI Shield
  - excellent Noise Immunity
- Lower I_{LEDA} Current
- IEC825-Class 1 Eye Safe
- Enhanced Reliability Performance
- Fully Compliant to IrDA 1.1 Specifications
  - excellent Nose-to-Nose operation
  - 2 Channels:
    - 2.4 Kb/s to 115.2 Kb/s
    - 576 Kb/s to 4.0 Mb/s
- Designed to Accommodate Light Loss with Cosmetic Windows
- Compatible with ASK, HP-SIR and TV Remote
- No Mode Programming Required
- Interfaces to Various Super I/O and Controller Devices

Applications

- Data Communication: Notebook Computers, Subnotebook Computers, Desktop Computers, Printers, PDAs, Fax/ Photocopier
- Digital Imaging: Digital Cameras, Photo Imaging Printers
- Digital Appliances: Internet Web TVs, Internet Appliances
- Industrials and Medical Instrumentation
  - General Data Collection Devices
  - Patient and Pharmaceutical Data Collection
- IR LANs

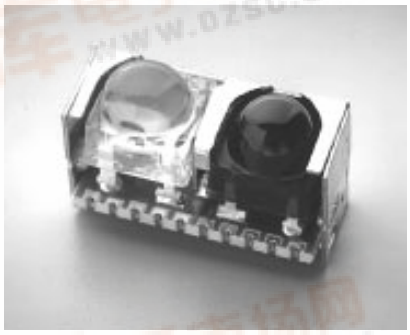
Description

The HSDL-2100 is a new generation low-cost Infrared (IR) transceiver module that provides the interface between logic and IR signals for through-air, serial, half-duplex IR data links and is compliant to IrDA Physical Layer Specification 1.1. This module is also IEC825-Class 1 Eye Safe.

Package

This IR module provides two output signals, RXD-A for signal rates from 2.4 Kb/s to 115.2 Kb/s and RXD-B for signal rates of 0.576 Mb/s to 4.0 Mb/s.

HSDL-2100 consists of the following basic elements: an Optical SubAssembly (OSA) and an Electrical SubAssembly (ESA) combination with an integrated EMI shield.



I/O pins configuration table is shown on page 2. HSDL-2100 block diagram and recommended application circuit is illustrated in Figure 1 on page 3. The IR transceiver module package outline and recommended PCBoard Pad layout, (Option #001 — Integrated EMI shield with guide pins) is illustrated in Figure 2 on page 4.

Benefits

This combination of an integrated EMI shield and transceiver sub-assembly utilizes existing in-house high-volume assembly processes ensuring high quality and high-volume supply. An integrated EMI shield helps to ensure low EMI emissions and high immunity to EMI fields, enhancing reliable performance.

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A brief description of the 2 basic sub-assemblies, *O*ptical *S*ub*A*ssembly (OSA) and *E*lectrical *S*ub*A*ssembly (ESA), is on page 2.

Applications Information

The Applications Engineering group, in the Hewlett-Packard Communications Semiconductor Solutions Division, is available to assist you with the technical understanding associated with this IR transceiver module. You can contact them through your local Hewlett-Packard sales representative for additional details.

Optical SubAssembly

The Optical SubAssemblies (OSA) includes a Transmitter and a Receiver. The transmitter has a discrete emitter that utilizes a high speed, high efficiency, Transparent Substrate, double heterojunction, Aluminum Gallium Arsenide (TS AlGaAs) LED technology with an integral lens in a clear molded package. The transmitter lens is optimized for speed, efficiency, and distance at an emission wavelength of 870 nm.

The receiver utilizes a discrete silicon PIN photodiode with an integral lens in a molded package and contains a dye to absorb visible light. The receiver lens magnifies the effective area of the PIN diode to enhance sensitivity. The power supply for the PIN and preamplifier are filtered to attenuate noise from external sources.

Electrical SubAssembly

The Electrical SubAssembly (ESA) consists of a printed circuit board on which a bipolar silicon Integrated Circuit (IC) and various surface-mount passive circuit elements are attached. The IC contains an LED driver and a receiver providing two output signals, RXD-A and RXD-B.

I/O Pins Configuration Table

Pin	Description	Symbol
1	LED Anode	LEDA
2	Transmitter Data Input	TXD
3	Receiver Data Output – Channel B	RXD-B
4	Receiver Data Output – Channel A	RXD-A
5	Threshold Capacitor	CX3
6	Ground	GND
7	Supply Voltage	V_{CC}
8	Averaging Capacitor	CX4
9	Ground (Analog)	GND
10	PIN Bypass Cap	CX1

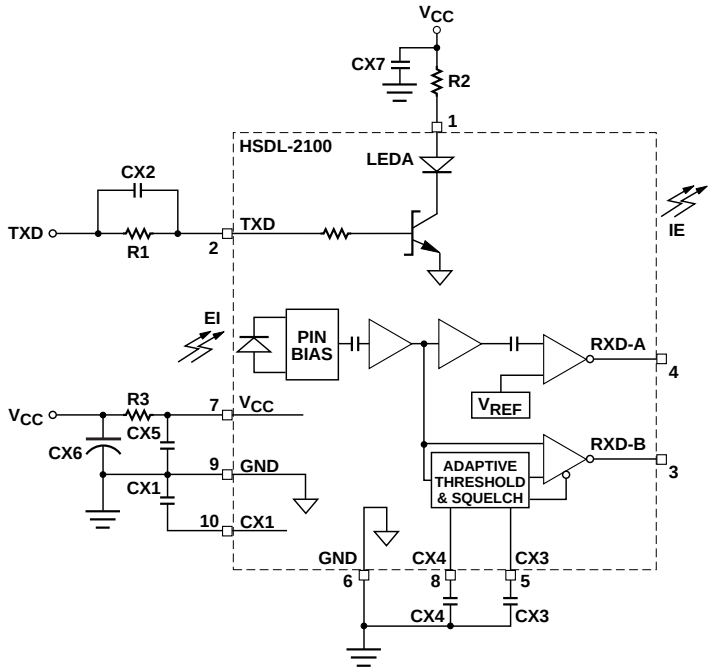


Figure 1. HSDL-2100 Block Diagram and Application Circuit.

Recommended Application Circuit Components

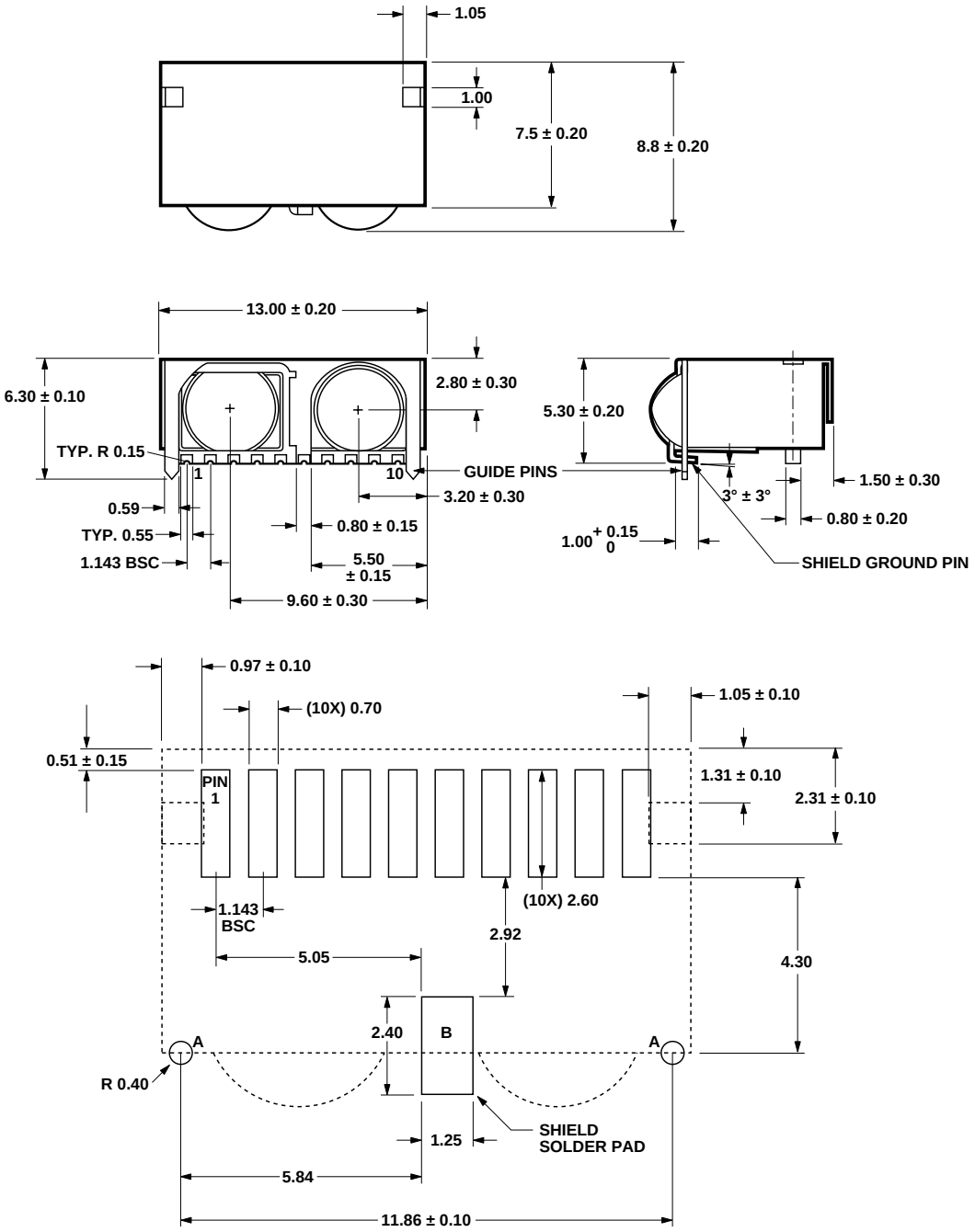
Component	Recommended Value
R1	560 Ω, ± 5%, 0.125 Watt
R2	4.7 Ω, ± 5%, 0.5 Watt
R3[1]	10 Ω, ± 5%, 0.125 Watt
CX1[2]	0.47 µF, ± 10%, X7R Ceramic
CX2	220 pF, ± 10%, X7R Ceramic
CX3[4]	4700 pF, ± 10%, X7R Ceramic
CX4	0.010 µF, ± 10%, X7R Ceramic
CX5[2]	0.47 µF, ± 20%, X7R Ceramic ≤ 5 mm lead length
CX6	6.8 µF Tantalum. Larger value recommended for noisy supplies or environments.
CX7[3]	0.47 µF, ± 20%, X7R Ceramic.

Notes:

1. In environments with noisy power supplies, supply rejection can be enhanced by including R3 as shown in application circuit.
2. CX1 and CX5 must be placed within 0.7 cm of the HSDL-2100 to obtain optimum noise immunity.
3. Only necessary in applications where transmitter switching causes more than a 50 mV ripple on V_{CC}.
4. CX3 may be replaced with 1000 pF for MIR, FIR application performance. For FIR application used 4700 pF as shown in application circuit.

Package Outline with Dimension and Recommended PCBoard Pad Layout

(Option #001 — Integrated EMI shield with Guide Pins.)

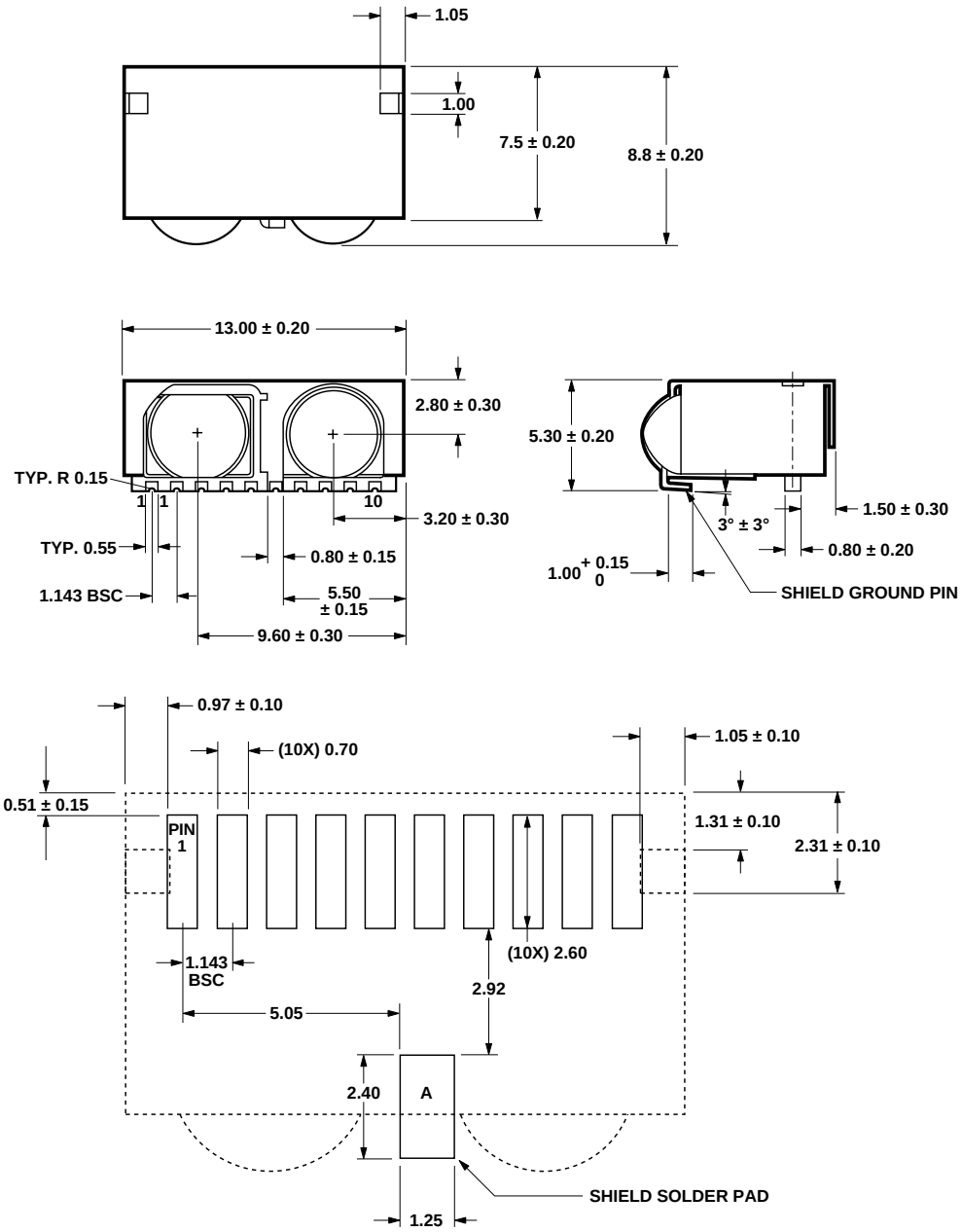


NOTES:
1. RECOMMENDED SOLDER STENCIL TO BE 5 TO 6 MILS THICK.
2. LETTER 'A' INDICATES LOCATION OF THROUGH HOLE FOR SHIELD GUIDE PIN.
2. LETTER 'B' INDICATES LOCATION OF SHIELD SOLDERED GROUNDING PAD.

Figure 2.

Package Outline with Dimension and Recommended PCBoard Pad Layout

(Option #002 — Integrated EMI shield without Guide Pins.)



NOTES:
1. RECOMMENDED SOLDER STENCIL TO BE 5 TO 6 MILS THICK.
2. LETTER 'A' INDICATES LOCATION OF SHIELD SOLDERED GROUNDING PAD.

Figure 3.

Truth Table

Inputs		Outputs		
TXD	**EI**	**IE (LED)**	**RXD-A**	**RXD-B**
V_{IH}	X	High (On)	NV	NV
V_{IL}	EI_H[1]	Low (Off)	Low[3]	NV
V_{IL}	EI_H[2]	Low (Off)	NV	Low[3]
V_{IL}	EI_L	Low (Off)	High	High

X = Don't care; NV = Not Valid

Notes:

1. In-Band EI ≤ 115.2 Kb/s.
2. In-Band EI ≥ 1.15 Mb/s.
3. Logic Low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.

Absolute Maximum Ratings[4]

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	-20	85	°C	
Operating Temperature	T_A	0	70	°C	
Average LED Current	I_{LED}(DC1)		100	mA	
Average LED Current	I_{LED}(DC2)		165	mA	≤ 90 ms Pulse Width, ≤ 25% Duty Cycle
Repetitive Pulsed LED Current	I_{LED}(RP)	350[5]	660[5]	mA	≤ 90 ms Pulse Width, ≤ 25% Duty Cycle
Peak LED Current	I_{LED}(PK)		750	mA	≤ 2 ms Pulse Width, ≤ 10% Duty Cycle
LED Anode Voltage	V_{LEDA}	-0.5	7	V	
Supply Voltage	V_{CC}	0	7	V	
Transmitter Data Input Current	I_{TXD}(DC)	-12	12	mA	
Receiver Data Output Voltage	V_{RXD-A} V_{RXD-B}	-0.5 -0.5	V_{CC} + 0.5 V_{CC} + 0.5	V V	

Notes:

4. For implementations where case to ambient thermal resistance ≤ 50°C/W.
5. See the thermal derating curves on pages 10 and 11 for maximum operating conditions in order to maintain T junction < 125°C.

Note: Performance is guaranteed in the operating temperature range of 0°C to 70°C. The information provided outside of this range is for reference only.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Operating Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	
Logic High Transmitter Input Voltage	V_{IH}(TXD)	4.25	5.25	V	[2]
Logic Low Transmitter Input Voltage	V_{IL}(TXD)	0	0.3	V	[2]
Logic High Receiver Input Irradiance	EI_H	0.0036 0.0090	500 500	mW/cm^2 mW/cm^2	For in-band signals ≤ 116 kb/s[1] For in-band signals ≤ 1.0 Mb/s[1]
Logic Low Receiver Input Irradiance	EI_L		0.3	μW/cm^2	For in-band signals[1]
LED (Logic High) Current Pulse Amplitude	I_{LEDA}	400	560	mA	[3]
Receiver Setup Time			1	ms	For full sensitivity after transmitting
Receiver Signal Rate RXD-A		2.4	115	Kb/s	
Receiver Signal Rate RXD-B		0.58	4	Mb/s	
Ambient Light					See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels.

Notes:

1. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
2. With R1, CX2 Input network and where t_r (V_I) and t_f (V_I) ≤ 5 ns. See Application Circuit for component values. The driver gate for this input should be able to source and sink ± 6 mA(DC) and ± 50 mA(pk). TXD refers to the node on the driver gate side of R1, CX2 on application circuit.
3. See the thermal derating curves on pages X and Y for maximum operating conditions in order to maintain T junction < 125°C.

Electrical and Optical Specifications

Specifications hold over the Recommended Operating Conditions unless otherwise noted. Test Conditions represent worst case values for the parameters under test. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25°C and 5 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Receiver Data Output Voltage	Logic Low	V_{OL}(RXD-A)[2]			0.5	V	I_O(RXD-A) = 1.0 mA. For in-band EI ≥ 3.6 μW/cm^2, $\phi_{1/2}$ ≤ 15°
	Logic Low	V_{OL}(RXD-B)[2]			0.5	V	I_O(RXD-B) = 1.0 mA. For in-band EI ≥ 9.0 μW/cm^2, $\phi_{1/2}$ ≤ 15°
	Logic High	V_{OH}(RXD-A)	V_{CC} - 0.6			V	I_{OH}(RXD-A) = -20 μA. For in-band EI ≤ 0.3 μW/cm^2
	Logic High	V_{OH}(RXD-B)	V_{CC} - 1.2			V	I_{OH}(RXD-B) = -20 μA. For in-band EI ≤ 0.3 μW/cm^2
	Viewing Angle	$2\phi_{1/2}$	30			degrees	
Effective Detector Area				0.1		cm^2	
Transmitter Radiant Intensity	Logic High Intensity	EI_H	100	177	500	mW/SR	V_{IH}(TXD) = 4.25 V[1], I_{LEDA} = 400 mA, T_A = 25°C, $\theta_{1/2}$ ≤ 15°
	Peak Wavelength	λp		875		nm	
	Spectral Line Half Width	$\Delta\lambda_{1/2}$		35		nm	
	Viewing Angle	$2\theta_{1/2}$	30		60	degrees	
Transmitter Data Input Current	Logic Low	I_L(TXD)	-2		2	μA	Gnd ≤ V_{IL}(TXD) ≤ 0.3 V[1]
	Logic High	I_H(TXD)	5.4		6.6	mA	V_{IH}(TXD) = 4.25 V[1]
LED Anode On State Voltage		V_{ON}(LEDA)			2.78	V	I_{LEDA} = 400 mA, 25°C V_{IH}(TXD) = 4.25 V[1]
LED Anode Off State Leakage		I_{LK} (LEDA)			250	μA	V_{LEDA} = V_{CC} = 5.25 V, V_{IL}(TXD) = 0.3 V[1]
Supply Current	Idle	I_{CC1}		3	5.1	mA	V_{CC} = 5.25 V, V_I(TXD) = V_{IL}, EI = 0
	Active Receiver	I_{CC2}		4	22	mA	V_{CC} = 5.25 V, V_I(TXD) = V_{IL} EI ≤ 500 mW/cm^2
Receiver Peak Sensitivity Wavelength		λp		880		nm	

Notes:

1. With R1, CX2 input network. See Application Circuit for component values. TXD refers to driver gate of R1, CX2 on application circuit.
2. Logic Low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.

Switching Specifications

Specifications hold over the Recommended Operating Conditions unless otherwise noted. Test Conditions represent worst case values for the parameters under test. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25°C and 5 V unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Transmitter Radiant Intensity Pulse Width	tpw (IE)	1.5	1.6	1.8	µs	tpw (TXD) = 1.6 µs at 115.2 K pulses/second
		115	125	135	ns	tpw (TXD) = 125 ns at 2.0 M pulses/second
Transmitter Radiant Intensity Rise and Fall Times	t_r(IE), t_f(IE)			40	ns	tpw (TXD) = 125 ns at 2.0 M pulses/second
RXD-A Pulse Width	tpw (RXD-A)	1		7.5	µs	[1] $\phi_{1/2} \leq 15°$
RXD-B Pulse Width	tpw (RXD-B)	75		175	ns	[2] $\phi_{1/2} \leq 15°$
RXD-B Pulse Width (ASK)		0.7	1	1.3	µs	[3] 500 kHz/50% duty cycle carrier ASK
Receiver Latency Time	t_L(RXD-B) t_L(RXD-A)		0.5	1	ms	[1][2]

Notes:

1. For In-Band signals ≤ 115.2 Kb/s where 3.6 µW/cm^2 ≤ EIL ≤ 500 mW/cm^2.
2. For In-Band signals, 125 ns PW, 4 Mb/s, 4 PPM where 9.0 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
3. Pulse width specified is the pulse width of the second 500 kHz carrier pulse received in a data bit. The first 500 kHz carrier pulse may exceed 2 µs in width, which will not affect correct demodulation of the data stream. An ASK and DASK system using the HSDL-2100 has been shown to correctly receive all data bits for 9 µW/cm^2 < EI < 500 mW/cm^2 incoming signal strength. ASK or DASK should use the RXD B channel only.

Reflow Profile

Figure 4 in page 10 is a straight line representation of a nominal temperature profile for a convective IR reflow solder process. The temperature profile is divided into four process zones with four ΔT/Δtime temperature change rates. The ΔT/Δtime temperature change rates are detailed in Table below Figure 4. The temperatures are measured at the component to printed-circuit (pc) board connections.

In **process zone P1,** the pc board and SMT HSDL-2100 castellation I/O pins joints are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3° per second to allow for even heating of both the pc board and the SMT HSDL-2100 castellation I/O pins joints.

Process zone P2 should be of sufficient time duration to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed -3°C (-5.4°F) per second maximum. This limitation is necessary to allow the pc board and SMT HSDL-2100 castellation I/O pins joints to change dimensions evenly, putting minimal stresses on the SMT HSDL-2100 transceiver packages.

The Temperature Profile for a Nominal Convective IR Reflow Solder Process
See the Table below for Δ Temperature (RX) Values.

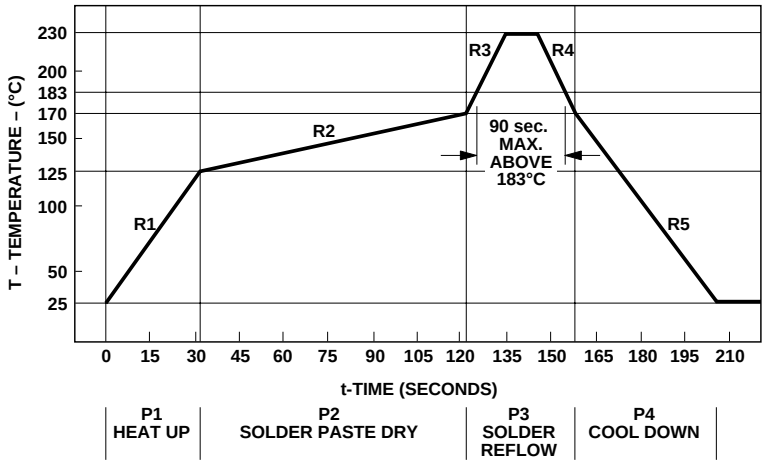


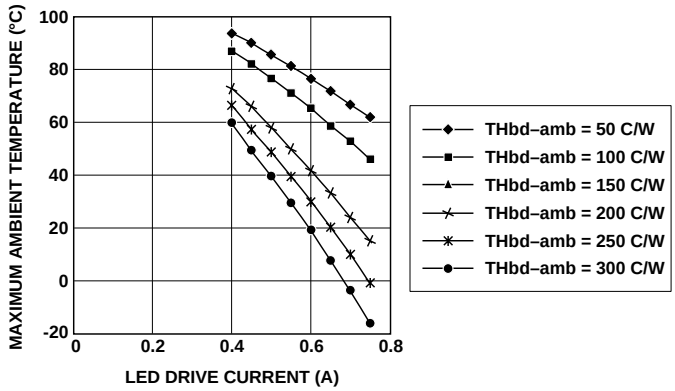
Figure 4.

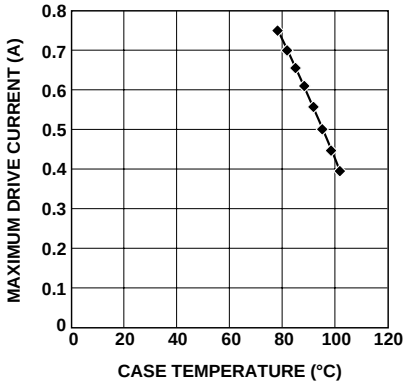
TABLE FOR CONVECTIVE PROCESS ZONES, SEE FIGURE 4.

PROCESS ZONE	SYMBOL	ΔT	ΔT/ΔTIME
HEAT UP	P1, R1	25°C TO 125°C	3°C/s MAX.
SOLDER PASTE DRY	P2, R2	125°C TO 170°C	0.5°C/s MAX.
SOLDER REFLOW	P3, R3 R4	170°C TO 230°C (235°C MAX.) 230°C TO 170°C	4°C/s TYP. -4°C/s TYP.
COOL DOWN	P4, R5	170°C TO 25°C	-3°C/s MAX.

Thermal Derating Curves

These 2 graphs show maximum allowable LED drive current as a function of ambient temperature and the designer's PCB-to-ambient thermal resistance.





JUNCTION TO CASE MEASUREMENTS FOR HSDL-2100

I_F (A)	MAX. CASE TEMPERATURE (°C)
0.4	101.3
0.45	98.4
0.5	95.3
0.55	92.1
0.6	88.7
0.65	85.2
0.7	81.6

Tape and Reel Dimensions

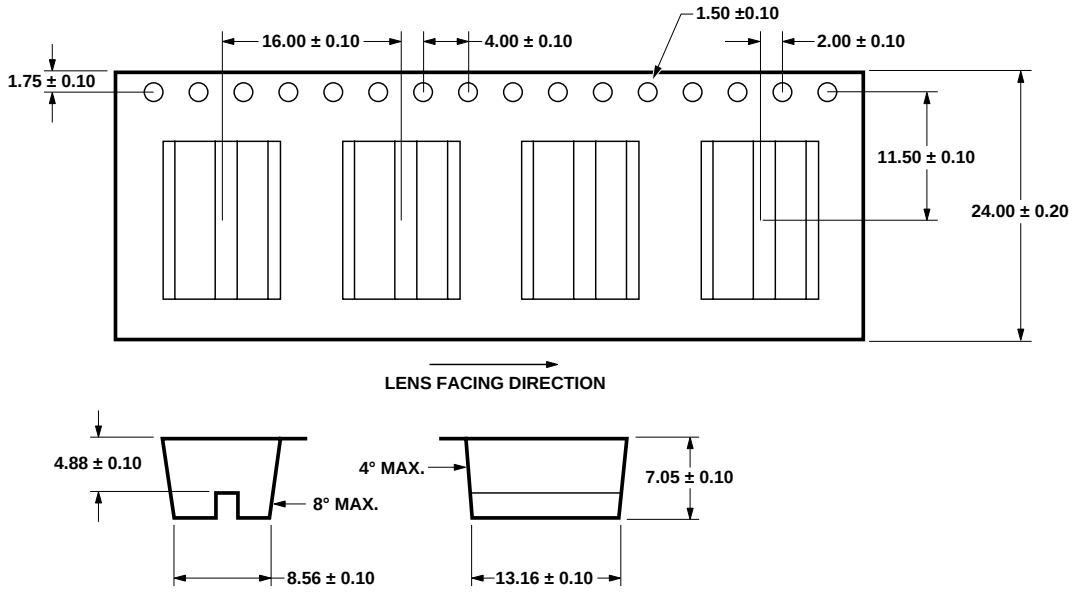


Figure 5.

Reel for 24 mm Tape

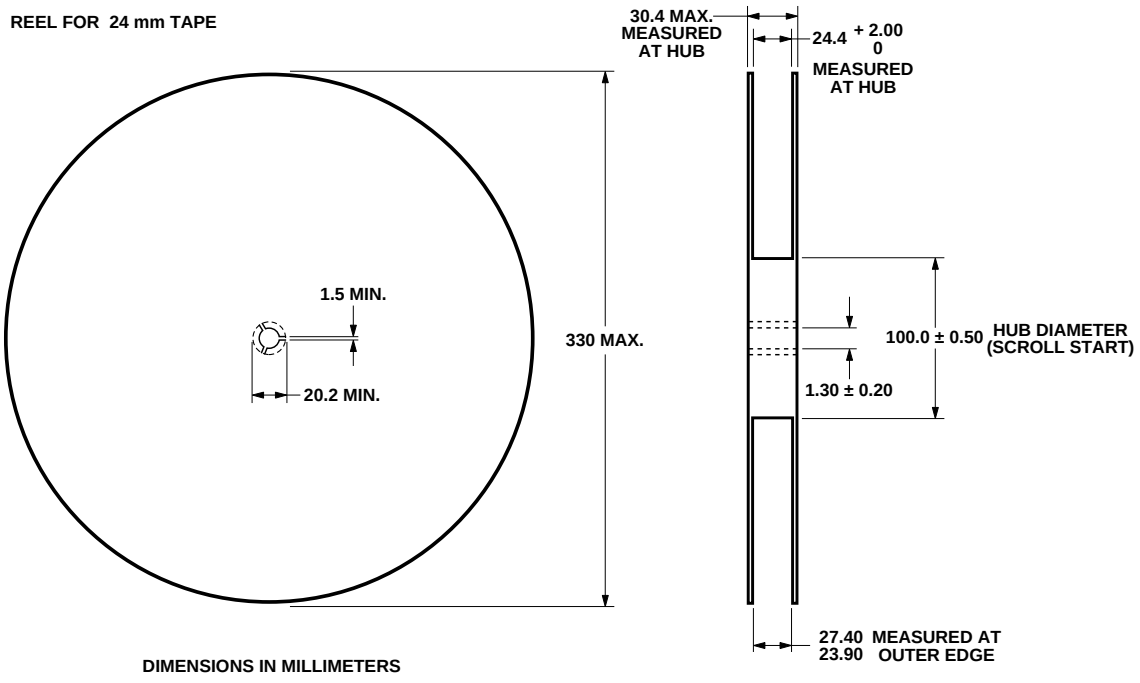


Figure 6.

Appendix A.
Test Methods
A.1. Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic field:
3 V/m maximum (refer to IEC 801-3, severity level 3 for details).

2. Sunlight: 10 kilolux maximum at the optical port.
This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width less than 50 nm biased to provide 490 $\mu W/cm^2$ (with no modulation) at the optical port. The light source faces the optical port. This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting: 1000 lux maximum.
This is produced with general service, tungsten-filament, gas-filled, inside-frosted lamps in the 60 Watt to 150 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 degrees Kelvin range and a spectral peak in the 850 nm to 1050 nm range.

4. Fluorescent Lighting: 1000 lux maximum.
This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 $\mu W/cm^2$ minimum and 0.3 $\mu W/cm^2$ peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz. Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

All HP IR transceivers are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1. AEL Class 1 LED devices are considered eye safe. See Hewlett-Packard Application Note 1094 for more information.

Appendix B. SMT Assembly Methods

1.0 Solder Pad, Mask and Metal Solder Stencil Adapter

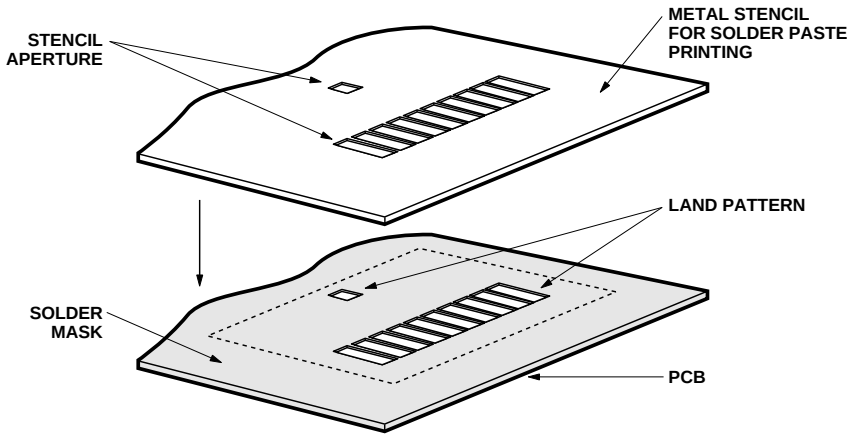


Figure 1.0. Stencil and PCB.

1.1. Recommended Land Pattern for HSDL-2100

Dim.	mm	Inches
a	2.6	0.1
b	0.7	0.03
c (pitch)	1.14	0.05
d	2.4	0.09
e	1.25	0.05
f	4.22	0.17
g	5.05	0.2

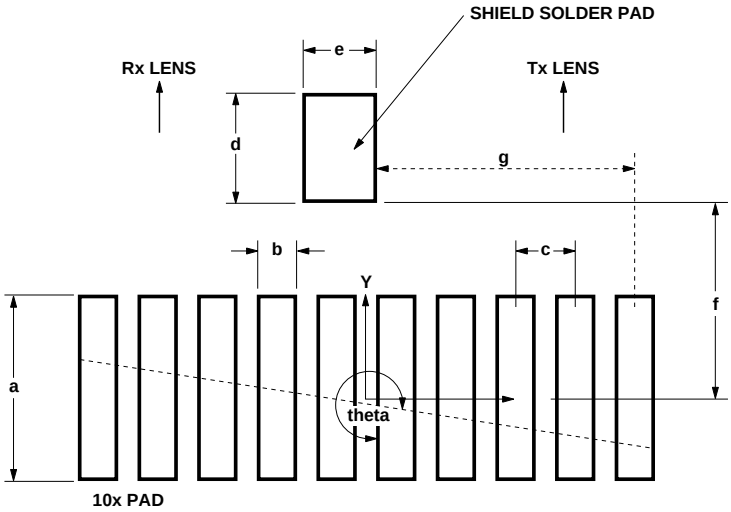
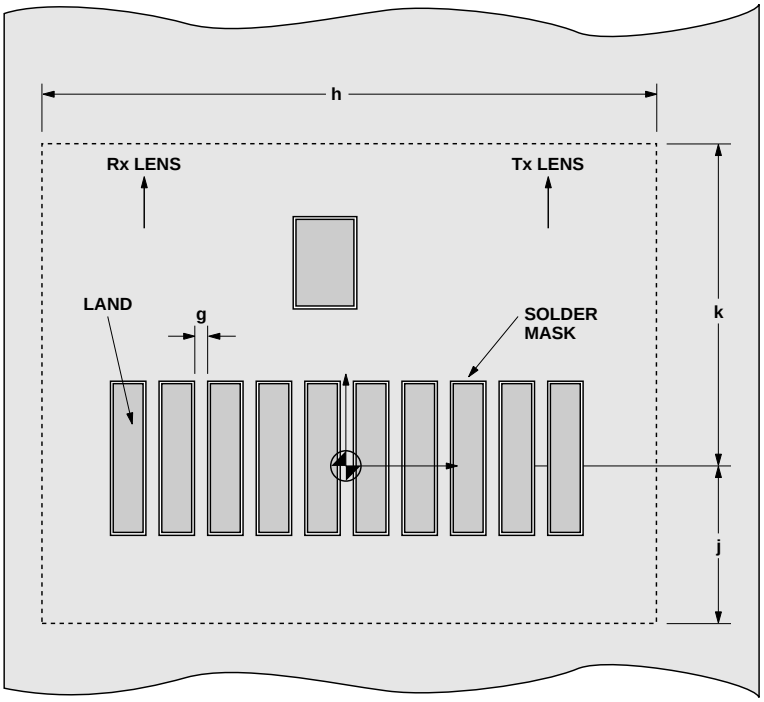


Figure 2.0. Top View of Land Pattern.

1.2. Adjacent Land Keepout and Solder Mask Areas

Dim.	mm	Inches
g	min. 0.15	min. 0.006
h	13.4	0.53
k	7.2	0.28
j	2.1	0.08

- Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.
- **"g"** is the minimum solder resist strip width required to avoid solder bridging adjacent pads. Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.



DIM.	mm	INCHES
g	MIN. 0.15	MIN. 0.006
h	13.4	0.53
k	7.2	0.28
j	2.1	0.08

• ADJACENT LAND KEEP-OUT IS THE MAXIMUM SPACE OCCUPIED BY THE UNIT RELATIVE TO THE LAND PATTERN. THERE SHOULD BE NO OTHER SMD COMPONENTS WITHIN THIS AREA.

• "g" IS THE MINIMUM SOLDER RESIST STRIP WIDTH REQUIRED TO AVOID SOLDER BRIDGING ADJACENT PADS.

NOTE: WET/LIQUID PHOTO-IMAGEABLE SOLDER RESIST/MASK IS RECOMMENDED.

Figure 3.0. PCBA — Adjacent Land Keep-out and Solder Mask.

2.0. Recommended Solder Paste/Cream Volume for Castellation Joints.
The printed solder paste volume required per castellation pad is 0.36 cubic mm ± 15% (based on either on-clean or aqueous solder cream types with typically 60 to 65% solid content by volume).

2.1. Recommended Metal Solder Stencil Aperture.
To ensure adequate printed solder paste volume, the following combination of metal stencil aperture and metal stencil thickness should be used:

See Figure 4.0			
t, nominal stencil thickness		**l, length of aperture**	
mm	**inches**	**mm**	**inches**
0.127	0.005	3.8 ± 0.1	0.150 ± 0.004
0.152	0.006	3.4 ± 0.1	0.134 ± 0.004
0.203	0.008	2.7 ± 0.1	0.106 ± 0.004
w, the width of aperture is fixed at 0.7 mm (0.028 inches)			

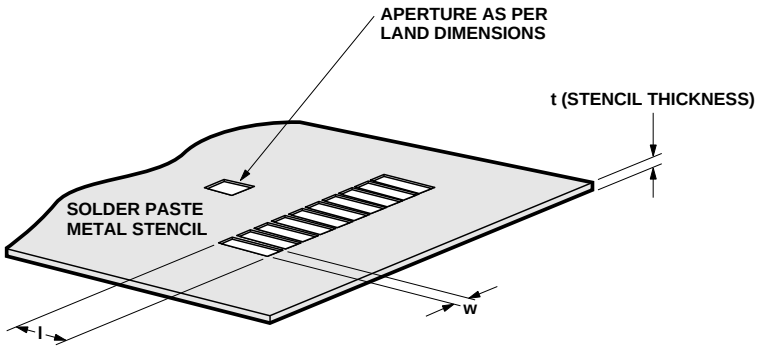


Figure 4.0. Solder Paste Stencil/Aperture.

3.0. Pick and Place Misalignment Tolerance and Product Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, **the HSDL-2100 will self align** after solder reflow. Units should be properly reflowed in IR-Hot Air convection oven using the recommended reflow profile. The direction of board travel does not matter.

Allowable Misalignment Tolerance

X - Direction	< = 0.2 mm (0.008 inches)
***Theta* - Direction**	± 3 degrees

3.1. Tolerance for X-axis Alignment of Castellation.

Misalignment of castellation to the land pad should not exceed 0.2 mm or approximately half the width of the castellation during placement of the unit. The castellations will completely self-align to the pads during the solder reflow.

3.2. Tolerance for Rotational (Theta) Misalignment.

Units when mounted should not be rotated more than ± 3 degrees with reference to center X–Y as specified in Figure 2.0.

Units with a Theta misalignment of more than 3 degrees does not completely self-align after reflow. Units with ± 3 degrees rotational or Theta misalignment self-aligns completely after solder reflow.

3.3. Y-axis Misalignment of Castellation.

In the Y direction, the unit does not self align after solder reflow. This should not be an issue as the length of the pad (2.6 mm) is sufficient for a misplacement accuracy of ± 0.2 mm from center of Y-axis as shown in Figure 5.0 below. There is still more than sufficient space for a proper strong solder fillet to be fully formed on both sides of the castellation joints.

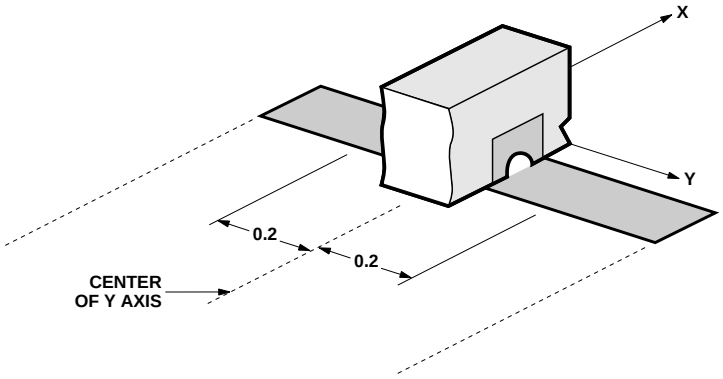


Figure 5.0 Section of a castellation in Y-axis

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