Agilent HSDL-3200 IrDA® Data 1.4 Compliant 115.2 Kb/s Infrared Transceiver

Data Sheet

Description

The HSDL-3200 is a new generation of low-cost Infrared (IR) transceiver module from Agilent Technologies. It features the smallest footprint in the industry at 2.5 H x 8.0 W x 3.0 D mm. The supply voltage can range from 2.7 V to 3.6 V. The LED drive current of 25 mA assures that link distances meet the IrDA Data 1.4 (low power) physical layer specification.

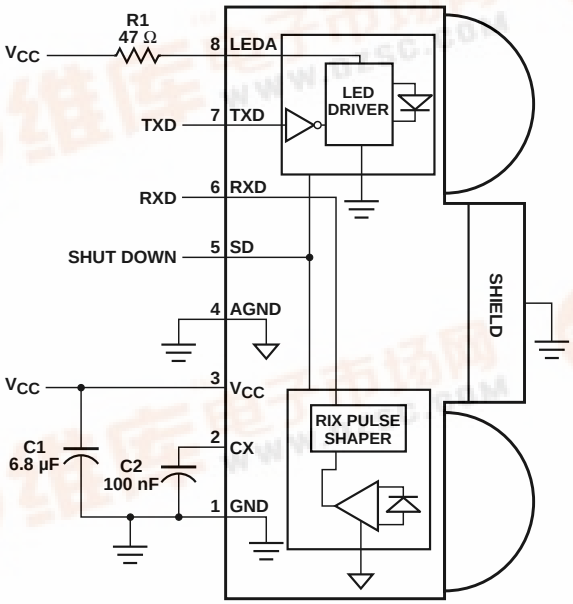
The HSDL-3200 meets the link distance of 20 cm to other low power devices, and 30 cm to standard 1 meter IrDA devices.

Features

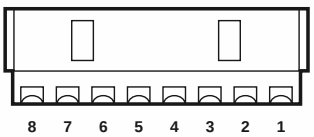
- Fully compliant to IrDA data 1.4 low power specifications
- Ultra small package
- Minimal height: 2.5 mm
- 2.7 to 3.6 V_{CC}
- Low shutdown current
  - 10 nA Typical
- Complete shutdown
  - TXD, RXD, PIN diode
- Three external components
- Temperature performance guaranteed, –25°C to +85°C
- 25 mA LED drive current
- Integrated EMI shield
- IEC825-1 Class 1 eye safe
- Edge detection input
  - Prevents the LED from long turn-on time
- Lead-free and RoHS compliant

Applications

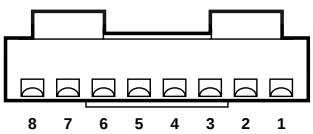
- Mobile telecom
  - Cellular phones
  - Pagers
  - Smart phones
- Data communication
  - PDAs
  - Portable printers
- Digital imaging
  - Digital cameras
  - Photo-imaging printers
- Electronic wallet



HSDL-3200#021 Pinout



HSDL-3200-028 Pinout



Agilent Technologies

I/O Pins Configuration Table

Pin	Description	Symbol	Active	Note
1	Ground	GND		
2	Pin Bypass Capacitor	CX		
3	Supply Voltage	V_{CC}		
4	Analog Ground	AGND		
5	Shut Down	SD	High	1
6	Receiver Data Output	RXD	Low	
7	Transmitter Data Input	TXD	High	
8	LED Anode	LEDA		

Note:
1. The shutdown pin (SD) must be driven either high or low. Do NOT float the pin.

Transceiver I/O Truth Table

Inputs			Outputs		
TXD	**Light Input to Receiver**	**SD**	**LED**	**RXD**	**Notes**
High	Don't Care	Low	On	Not Valid	
Low	High	Low	Off	Low	2, 3
Low	Low	Low	Off	High	
Don't Care	Don't Care	High	Off	High	

Notes:
2. In-Band IrDA signals and data rates ≤115.2 Kb/s.
3. RXD Logic Low is a pulsed response. The condition is maintained for a duration dependent on pattern and strength of the incident intensity.

Ordering Information

The ordering information is as shown in the table below. There are two options available.

Front Option	
#021	Taped and 13" Reel packaging, 2500 per reel
Top Option	
–028	Taped and 13" Reel Packaging, 2500 per reel

Recommended Application Circuit Components

Component	Recommended Value	Note
R1	47 Ω, ± 1%, 0.125 Watt	
C1	6.8 µF, ± 20%, Tantalum	4
C2	100 nF, ± 20%, X7R Ceramic	

Note:
4. C1 must be placed within 0.7 cm of the HSDL-3200 to obtain optimum noise immunity.

Caution: *The BiCMOS inherent to this design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	–40	100	°C	
Operating Temperature	T_A	–25	85	°C	
DC LED Current	I_{LED} (DC)		20	mA	
Peak LED Current	I_{LED} (PK)		80	mA	≤ 90 µs Pulse Width, ≤25% Duty Cycle
LED Anode Voltage	V_{LEDA}	–0.5	7	V	
Supply Voltage	V_{CC}	0	7	V	
Input Voltage TXD, SD	V_I	0	V_{CC} +0.5	V	
Output Voltage RXD	V_O	–0.5	V_{CC} +0.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions	Notes
Operating Temperature	T_A	–25	85	°C		
Supply Voltage	V_{CC}	2.7	3.6	V		
Logic High Voltage TXD, SD	V_{IH}	2/3 V_{CC}	V_{CC}	V		
Logic Low Voltage TXD, SD	V_{IL}	0	1/3 V_{CC}	V		
Logic High Receiver Input Irradiance	EI_H	0.0081	500	mW/cm^2	For in-band signals.	5
Logic Low Receiver Input Irradiance	EI_L		0.3	µW/cm^2	For in-band signals.	5
LED Current Pulse Amplitude	I_{LEDA}	25	80	mA	Guaranteed at 25°C	
Receiver Signal Rate		2.4	115.2	Kb/s		
Ambient Light					See “Test Methods” on page 12 for details	

Note:

5. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.

Electrical and Optical Specifications

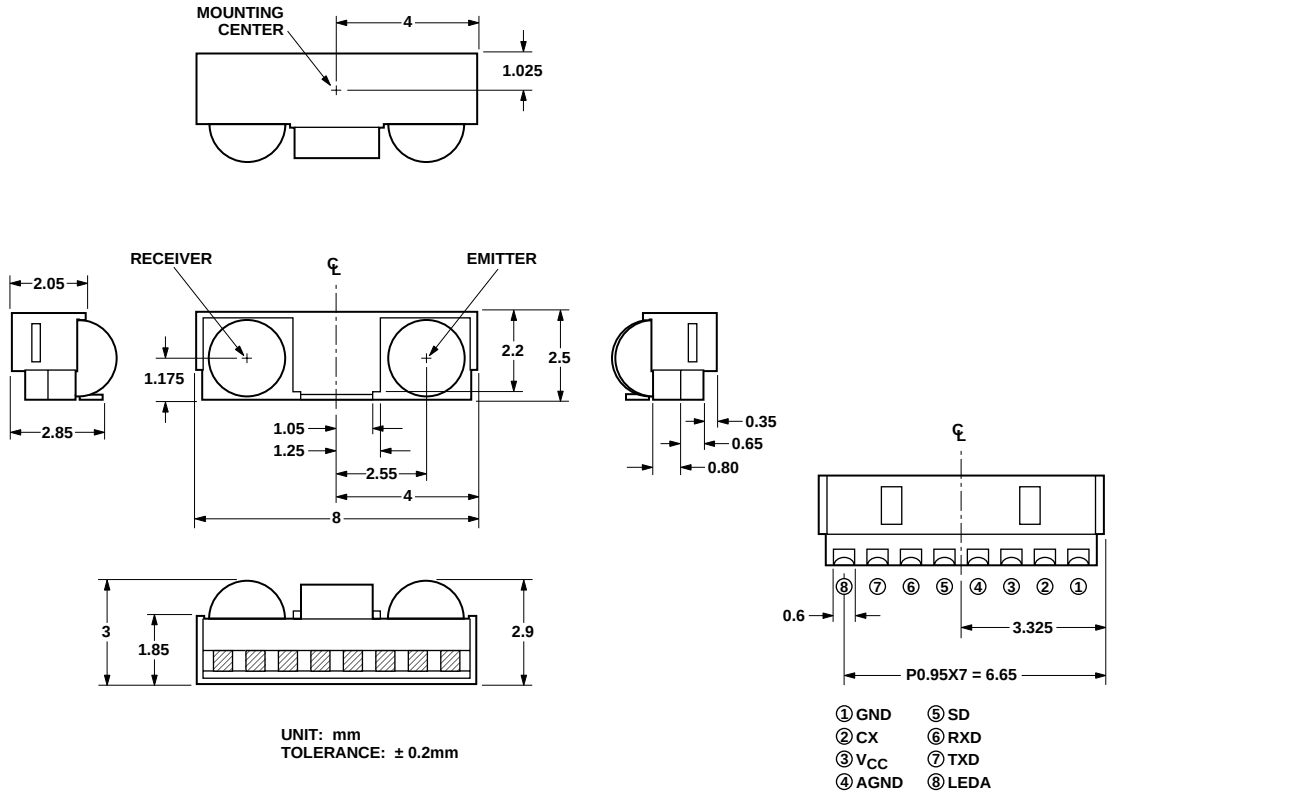
Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions can be anywhere in their operating range. All typical values are at 25°C and 3.0 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Note
Receiver								
RXD Output Voltage	Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 µA, For in-band EI	6
	Logic High	V_{OH}	V_{CC} –0.2		V_{CC}	V	I_{OH} = –200 µA, For in-band EI ≤0.3 µW/cm^2	
Viewing Angle		$2\phi_{1/2}$	30			°		
Peak Sensitivity Wavelength		λp		880		nm		
RXD Pulse Width		tpw	1.5	2.5	4.0	µs		6
RXD Rise and Fall Times		tr, tf		25	100	ns	tpw (EI) = 1.6 µs, C_L = 10 pF	
Receiver Latency Time		t_L		25	50	µs		6
Receiver Wake Up Time		t_W		50	100	µs		7
Transmitter								
Radiant Intensity		EI_H	4	8	28.8	mW/Sr	I_{LEDA} = 25 mA, T_A = 25°C, $\theta_{1/2}$ ≤15°	
Peak Wavelength		λp		875		nm		
Spectral Line Half Width		$\Delta\lambda_{1/2}$		35		nm		
Viewing Angle		$2\theta_{1/2}$	30		60	°		
Optical Pulse Width		tpw	1.5	1.6	2	µs	tpw (TXD) = 1.6 µs	
Optical Rise and Fall Times		tr (EI) tf (EI)			600	ns	tpw (TXD) = 1.6 µs	
Maximum Optical Pulse Width		tpw (max)		20	50	µs	TXD pin stuck high	
LED Anode On State Voltage		V_{ON} (LEDA)			1.6	V	I_{LEDA} = 25 mA, V_{IH} (TXD) = 2.7 V	
LED Anode Off State Leakage		I_{LK} (LEDA)		0.01	1.0	µA	V_{LEDA} = V_{CC} = 3.6 V, V_I (TXD) ≤ 1/3 V_{CC}	
Transceiver								
TXD and SD Input Current	Logic Low	I_L	–1	–0.01	1	µA	0 ≤ V_I ≤ 1/3 V_{CC}	
	Logic High	I_H		0.01	1	µA	V_I ≥ 2/3 V_{CC}	
Supply Current	Shutdown	I_{CC1}		10	200	nA	V_{CC} = 3.6 V, V_{SD} ≥ V_{CC} –0.5	
	Idle	I_{CC2}		2.5	4	mA	V_{CC} = 3.6 V, V_I (TXD) ≤ 1/3 V_{CC}, EI = 0	
	Active Receiver	I_{CC3}		2.6	5	mA	V_{CC} = 3.6 V, V_I (TXD) ≤ 1/3 V_{CC}	8, 9

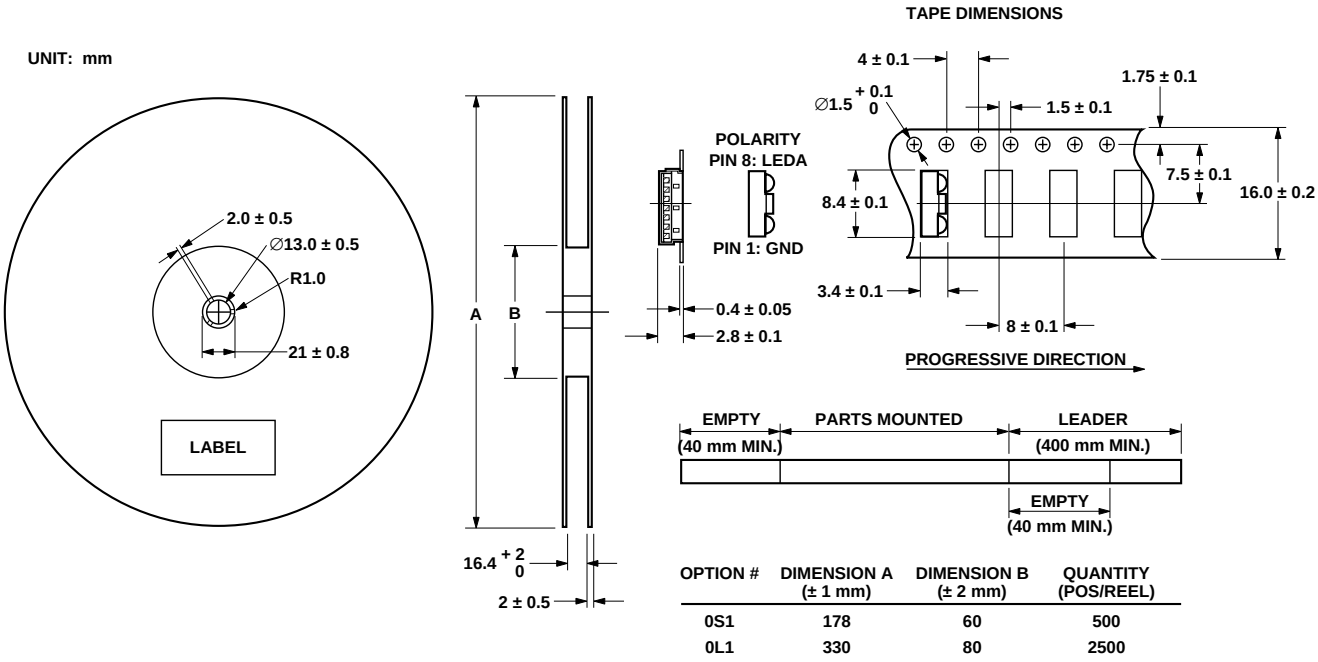
Notes:

6. For in-band signals ≤ 115.2 Kb/s where 8.1 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
7. Wake up time is measured from SD pin high to low transition or V_{CC} power on to valid RXD output.
8. Typical value is at EI = 10 mW/cm^2.
9. Maximum value is at EI = 500 mW/cm^2.

HDSL-3200#021 Package Dimensions

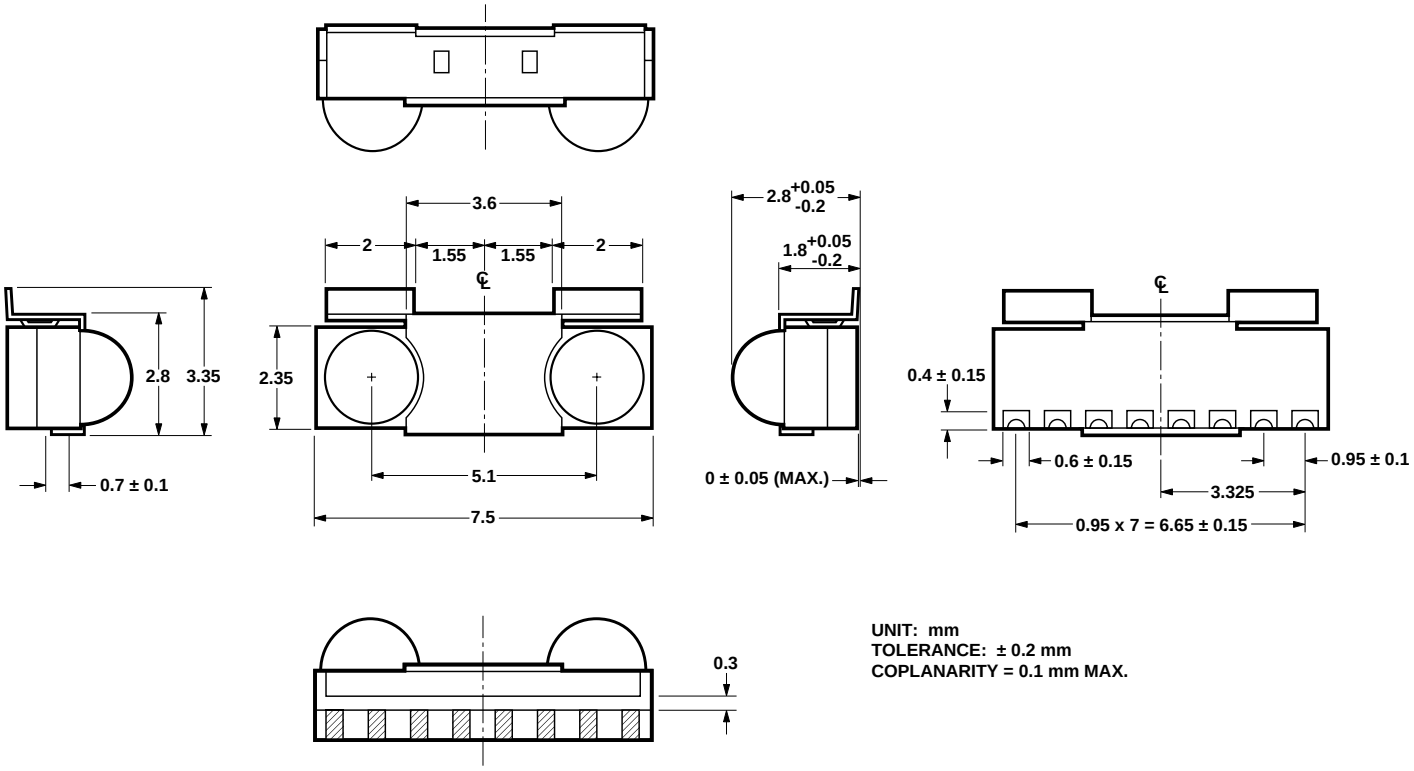


HSDL-3200#021 Tape and Reel Dimensions



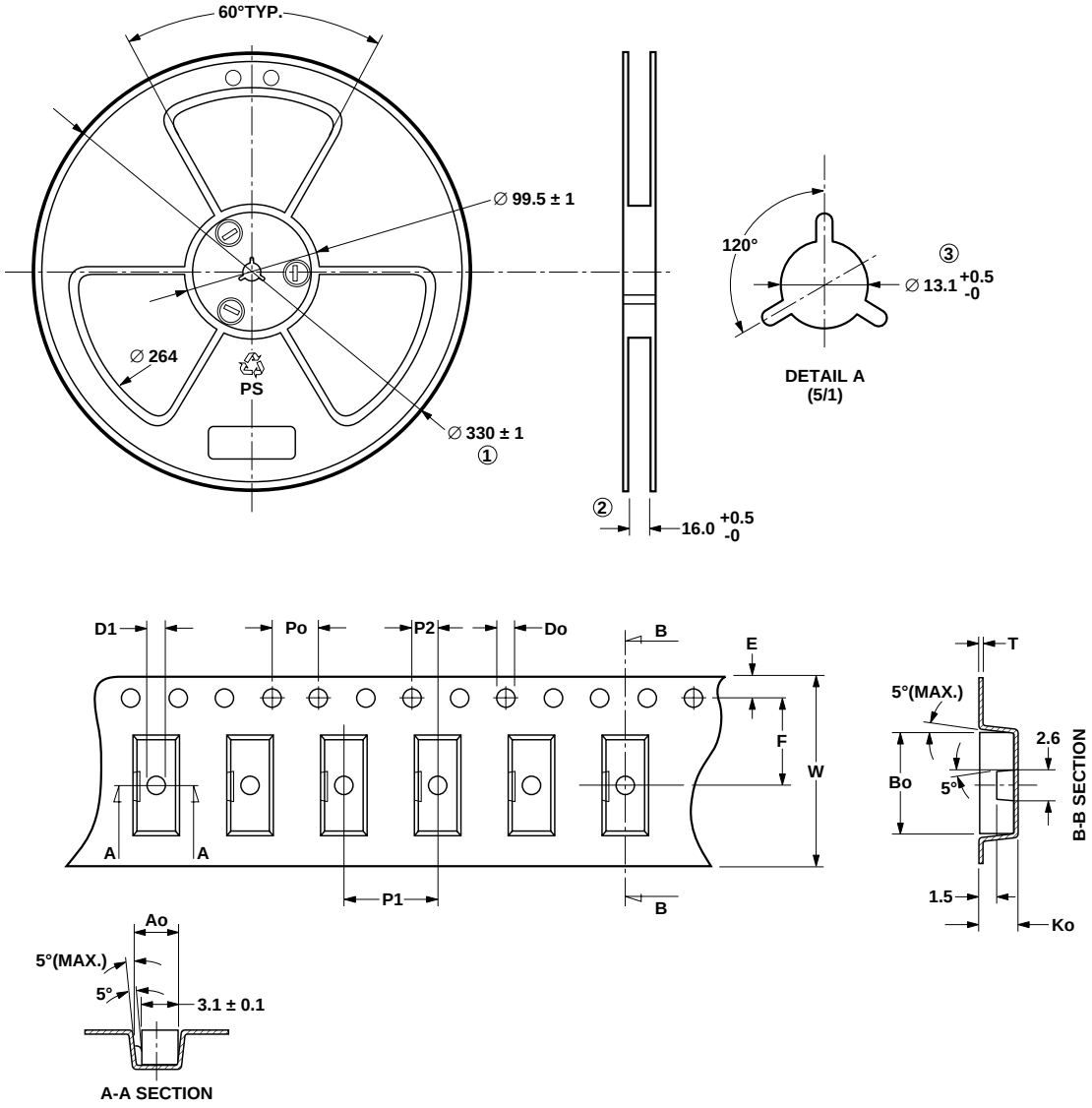
OPTION #	DIMENSION A (± 1 mm)	DIMENSION B (± 2 mm)	QUANTITY (POS/REEL)
0S1	178	60	500
0L1	330	80	2500

HSDL-3200-028 Package Outline



UNIT: mm
TOLERANCE: ± 0.2 mm
COPLANARITY = 0.1 mm MAX.

HSDL-3200-028 Tape and Reel Dimensions

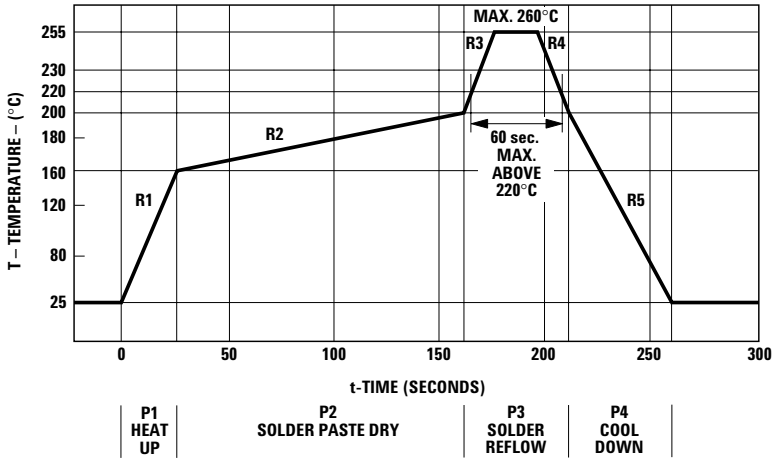


UNIT: mm

SYMBOL	Ao	Bo	Ko	Po	P1	P2	T
SPEC	3.65 ± 0.10	7.90 ± 0.10	2.75 +0.05 - 0.10	4.00 ± 0.10	8.00 ± 0.10	2.00 ± 0.10	0.40 ± 0.10
SYMBOL	E	F	Do	D1	W	10Po	
SPEC	1.75 ± 0.10	7.50 ± 0.10	1.55 ± 0.05	1.50 (MIN.)	16.00 ± 0.30	40.00 ± 0.20	

NOTES:
1. 10 SPROKET HOLE PITCH CUMULATIVE TOLERANCE IS ± 0.2 mm.
2. CARRIER CAMBER SHALL NOT BE MORE THAN 1 mm PER 100 mm THROUGH A LENGTH OF 250 mm.
3. Ao AND Bo MEASURED ON A PLACE 0.3 mm ABOVE THE BOTTOM OF THE PACKET.
4. Ko MEASURED FROM A PLACE ON THE INSIDE BOTTOM OF THE POCKET TO TOP SURFACE OF CARRIER.
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.

IR Transceiver Reflow Profile: Lead-free



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	4°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3	200°C to 255°C (260°C at 10 seconds max.)	4°C/s
	P3, R4	255°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3200 castellation I/O pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3200 castellation I/O pins.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3200 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3200 transceiver.

Moisture Proof Packaging

The HSDL-3200 is shipped in moisture proof packaging. Once opened, moisture absorption begins.

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	Below 60%

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 2 days if stored at the recommended storage conditions. If times longer than 2 days are needed, the parts must be stored in a dry box.

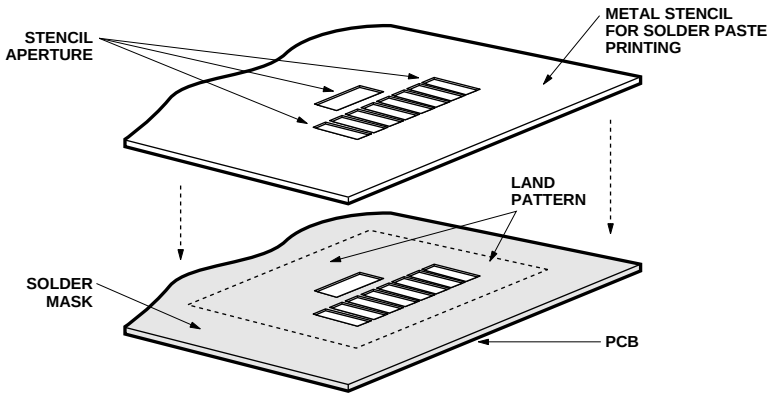
Baking

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

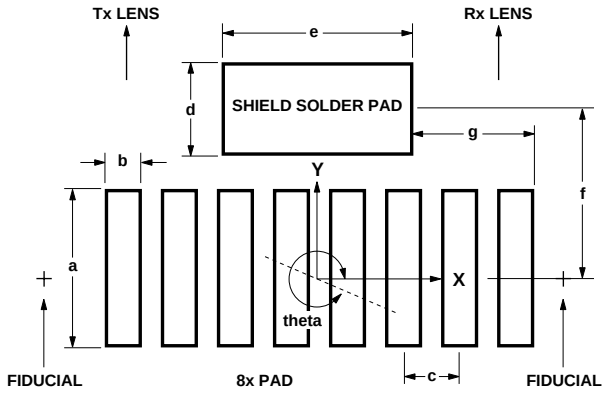
In Reels	60°C, t ≥ 48 hours
In Bulk	100°C, t ≥ 4 hours
	125°C, T ≥ 2 hours
	150°C, T ≥ 1 hour

Baking should only be done once.

Solder Pad, Mask and Metal Stencil

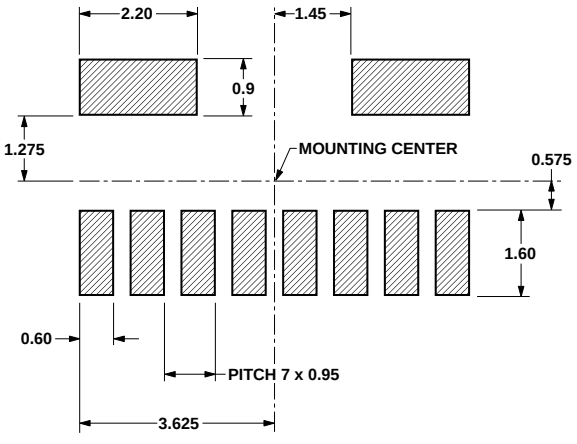


HSDL-3200#021 Recommended Land Pattern (Front Option)



DIMENSION	mm	INCHES
a	1.75	0.069
b	0.60	0.024
c (PITCH)	0.95	0.037
d	1.25	0.049
e	2.70	0.106
f	2.20	0.087
g	2.28	0.089

HSDL-3200-028 Recommended Land Pattern (Top Options)

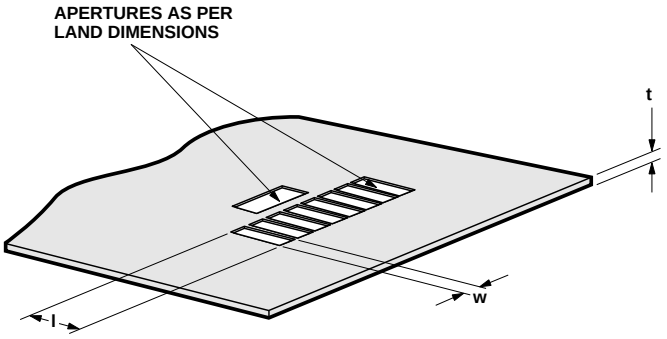


Recommended Metal Solder Stencil Aperture

It is recommended that only 0.127 mm (0.005 inches) or 0.11 mm (0.004 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. The following combination of metal stencil aperture and metal stencil thickness should be used:

w, the width of aperture is fixed at 0.55 mm (0.022 inches).

Aperture opening for shield pad is as per land pattern.



t, nominal stencil thickness		l, length of aperture	
mm	inches	mm	inches
0.127	0.005	1.75 ± 0.05	0.102 ± 0.002
0.11	0.004	2.4 ± 0.05	0.118 ± 0.002

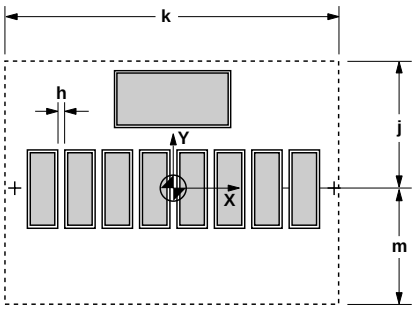
Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

"h" is the minimum solder resist strip width required to avoid solder bridging adjacent pads.

It is recommended that two fiducial crosses be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.



DIMENSION	mm	INCHES
h	MIN. 0.2	MIN. 0.008
k	8.2	0.323
j	2.6	0.102
m	3.0	0.118

Recommended Solder Paste/Cream Volume for Castellation Joints

Based on calculation and experiment, the printed solder paste volume required per castellation pad is 0.22 cubic mm (based on either no-clean or aqueous solder cream types with typically 60% to 65% solid content by volume). Using the recommended stencil will result in this volume of solder paste.

Pick and Place Misalignment Tolerance and Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, the HSDL-3200 will self-align after solder reflow. Units should be properly reflowed in IR/Hot Air convection oven using the recommended reflow profile. The direction of board travel does not matter.

Allowable Misalignment

Direction	Tolerance
x	≤0.2 mm (0.008 inches)
Theta	± 3 degrees

Tolerance for X-Axis Alignment of Castellation

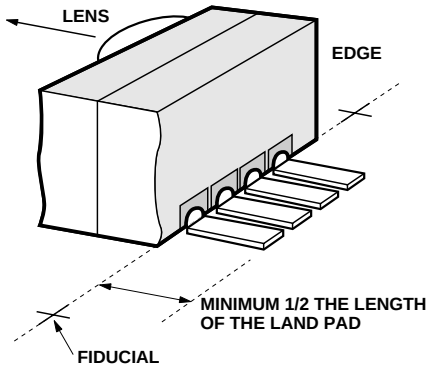
Misalignment of castellation to the land pad should not exceed 0.2 mm (0.008 in.), or about one half the width of the castellation during placement of the unit. The castellations will self-align to the pads during solder reflow.

Tolerance for Rotational (Theta) Misalignment

Units when mounted should not be rotated more than ± 3 degrees with reference to center X-Y as shown in the recommended land pattern. Units with rotational misalignment of more than ± 3 degrees will not completely self-align after reflow. Units with less than a ± 3 degree misalignment will self-align after solder reflow.

Y-Axis Misalignment of Castellation

In the Y direction, the HSDL-3200 does not self-align after solder reflow. It is recommended that it be placed in line with the fiducial mark (mid-length of land pad). This will enable sufficient land length (minimum of 1/2 land length) to form a good joint. See the drawing below.



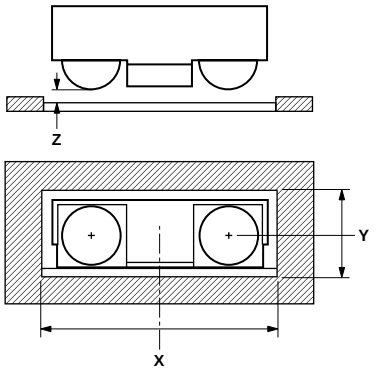
Marking Information

The unit is marked with a letter “B” and “YWWLL” for front options on the shield. Y is the year, WW is the workweek, and LL is the Lot information.

Window Design

To insure IrDA compliance, there are some constraints on the height and width of the optical window. The minimum dimensions ensure that the IrDA cone angles are met, and there is no vignetting, and the maximum dimensions ensure that the effects of stray light are minimized. The minimum size corresponds to a cone angle of 30 degrees, the maximum to a cone angle of 60 degrees.

The drawing below shows the module positioned in front of a window.



X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3200 to the back of the window.

The distance from the center of the LED lens to the center of the photodiode lens is 5.1 mm.

The equations that determine the size of the window are as follows:

$X = 5.1 + 2(Z + D) \tan \theta$
$Y = 2(Z + D) \tan \theta$

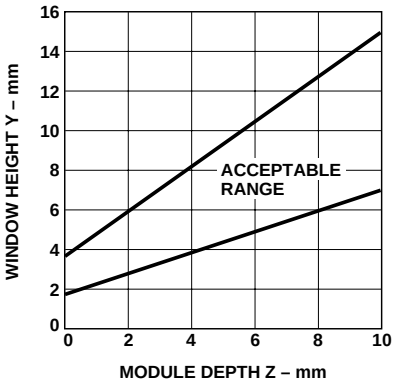
Where θ is the required half angle for viewing. For the IrDA minimum, it is 15 degrees, for the IrDA maximum it is 30 degrees. (D is the depth of the LED image inside the part, 3.17 mm.) These equations result in the following tables and graphs:

Minimum and Maximum Window Sizes

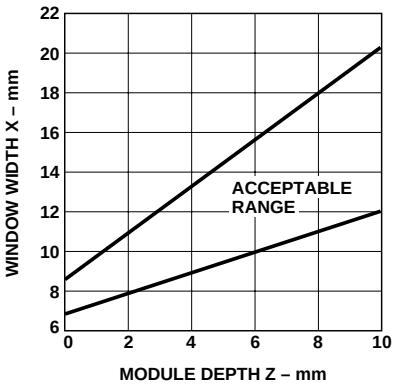
Dimensions are in mm.

Depth (Z)	Y Min.	X Min.	Y Max.	X Max.
0	1.70	6.80	3.66	8.76
1	2.23	7.33	4.82	9.92
2	2.77	7.87	5.97	11.07
3	3.31	8.41	7.12	12.22
4	3.84	8.94	8.28	13.38
5	4.38	9.48	9.43	14.53
6	4.91	10.01	10.59	15.69
7	5.45	10.55	11.74	16.84
8	5.99	11.09	12.90	18.00
9	6.52	11.62	14.05	19.15
10	7.06	12.16	15.21	20.31

Window Height Y vs. Module Depth Z



Window Width X vs. Module Depth Z



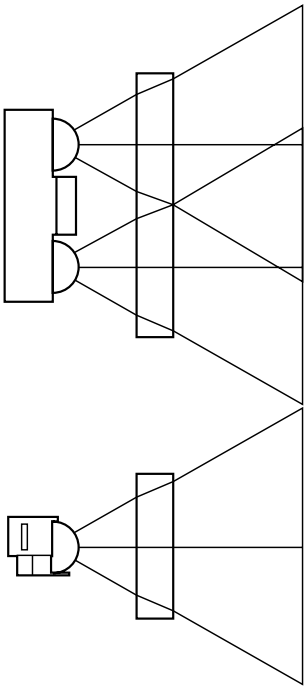
Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

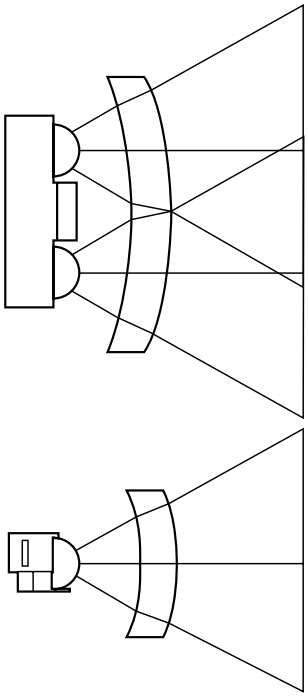
If the window must be curved for mechanical design reasons, place a curve on the back side of the window that has the same radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.

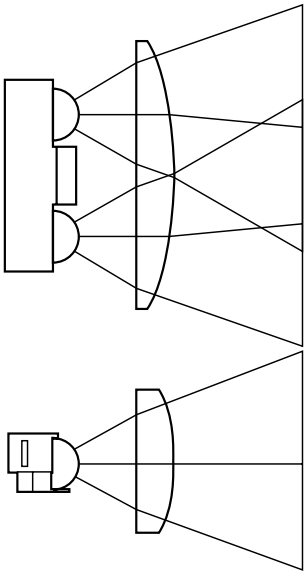
Flat Window



Curved Front and Back



Curved Front, Flat Back



Test Methods

Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic field:
   3 V/m maximum (please refer to IEC 801-3, severity level 3 for details).

2. Sunlight:
   10 kilolux maximum at the optical port. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased to provide 490 $\mu W/cm^2$ (with no modulation) at the optical port. The light source faces the optical port. This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting:
   1000 lux maximum. This is produced with general service, tungsten-filament, gas-filled, inside frosted lamps in the 60 Watt to 100 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 Kelvin range and a spectral peak in the 850 to 1050 nm range.

4. Fluorescent Lighting:
   1000 lux maximum. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 $\mu W/cm^2$ minimum and 0.3 $\mu W/cm^2$ peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

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Data subject to change.

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