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DATA SHEET

HSTL16918
9-bit to 18-bit HSTL-to-LVTTL memory address latch

Product data

2001 Jun 16

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Philips Semiconductors

9-bit to 18-bit HSTL-to-LVTTL memory address latch HSTL16918

FEATURES

- Inputs meet JEDEC HSTL Std. JESD 8–6, and outputs meet Level III specifications
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Packaged in 48-pin plastic thin shrink small outline package (TSSOP48)

DESCRIPTION

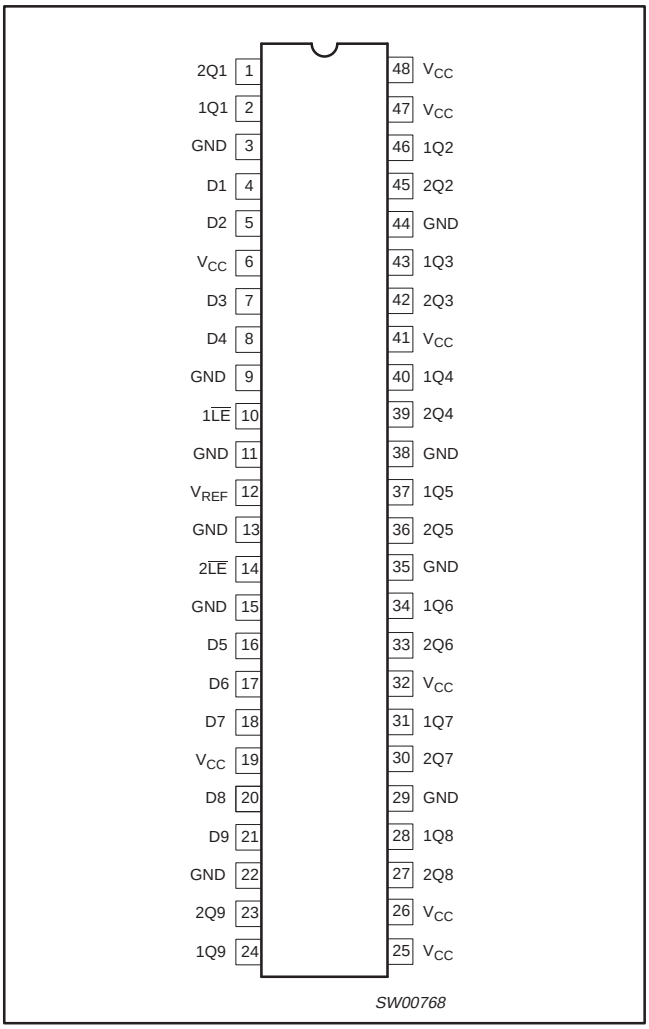
The HSTL16918 is a 9-bit to 18-bit D-type latch designed for 3.15 to 3.45 V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The HSTL16918 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable ($\overline{LE}$) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While $\overline{LE}$ is LOW the Q outputs of the corresponding nine latches follow the D inputs. When $\overline{LE}$ is taken HIGH, the Q outputs are latched at the levels set up at the D inputs.

The HSTL16918 is characterized for operation from 0 to +70 °C.

PIN CONFIGURATION



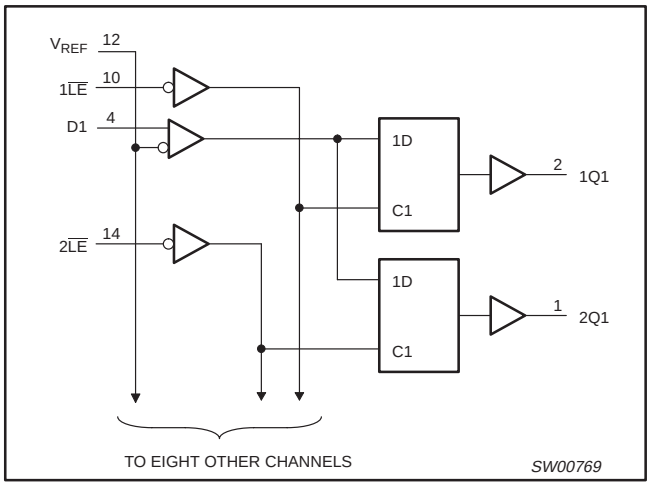
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-pin plastic thin shrink small outline package (TSSOP48)	0 to +70 °C	HSTL16918DGG	SOT362-1

PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
4, 5, 7, 8, 16, 17, 18, 20, 21	D[1–9]	Inputs
2, 46, 43, 40, 37, 34, 31, 28, 24	1Q[1–9]	Outputs
1, 45, 42, 39, 36, 33, 30, 27, 23	2Q[1–9]	
10	$1\overline{LE}$	Latch enable
14	$2\overline{LE}$	
12	V_{REF}	Reference voltage
6, 19, 25, 26, 32, 41, 47, 48	V_{CC}	Supply voltage
3, 9, 11, 13, 15, 22, 29, 35, 38, 44	GND	Ground

LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{LE}$	D	Q
L	H	H
L	L	L
H	X	Q_0 [1]

NOTE:
1. Output level before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply voltage range		–0.5 to +4.6	V
V_I	Input voltage range [2]		–0.5 to V_{CC} +0.5	V
V_O	Output voltage range [2]		–0.5 to V_{CC} +0.5	V
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current [3]	$V_O < 0$ or $V_O > V_{CC}$	±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	±50	mA
	Continuous current through each V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance [4]		89	°C/W
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This current flows only when the output is in the high state and $V_O > V_{CC}$.
4. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		3.15		3.45	V
V_{REF}	Reference voltage		0.68	0.75	0.9	V
V_I	Input voltage		0		1.5	V
V_{IH}	AC high-level input voltage	All inputs	V_{REF} + 200 mV			V
V_{IL}	AC low-level input voltage	All inputs			V_{REF} – 200 mV	V
V_{IH}	DC high-level input voltage	All inputs	V_{REF} + 100 mV			V
V_{IL}	DC low-level input voltage	All inputs			V_{REF} – 100 mV	V
I_{OH}	High-level output current				–24	mA
I_{OL}	Low-level output current				24	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ [1]	Max	
V_{IK}		V_{CC} = 3.15 V; I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 3.15 V; I_{OH} = –24 mA	2.4			V
V_{OL}		V_{CC} = 3.15 V; I_{OL} = 24 mA			0.5	V
I_I	Control inputs	V_{CC} = 3.45 V; V_I = 0 or 1.5 V			±5	µA
	Data inputs	V_{CC} = 3.45 V; V_I = 0 or 1.5 V			±5	µA
	V_{REF}	V_{CC} = 3.45 V; V_{REF} = 0.68 V or 0.9 V			90	µA
I_{CC}		V_{CC} = 3.45 V; V_I = 0 or 1.5 V		50	100	mA
C_I	Control inputs	V_{CC} = 0 or 3.3 V; V_I = 0 or 3.3 V		2		pF
	Data inputs	V_{CC} = 0 or 3.3 V; V_I = 0 or 3.3 V		2.5		pF
C_O	Outputs	V_{CC} = 0 V; V_O = 0 V		4		pF

NOTE:

1. All typical values are at V_{CC} = 3.3 V; T_{amb} = 25 °C.

TIMING REQUIREMENTS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} = 3.3 V ±0.15 V		UNIT
			Min	Max	
t_w	Pulse duration	$\overline{LE}$ LOW (Figure 1)	3		ns
t_{su}	Setup time	D before $\overline{LE}$ ↑ (Figure 2)	2		ns
t_h	Hold time	D after $\overline{LE}$ ↑ (Figure 2)	1		ns
t_{ldr}	Data race condition time [1]	D after $\overline{LE}$ ↓		0	ns

NOTE:

1. This is the maximum time after $\overline{LE}$ switches LOW that the data input can return to the latched state from the opposite state without producing a glitch on the output.

SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range; V_{REF} = 0.75 V.

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ±0.15 V		UNIT
				Min	Max	
t_{pd}	Propagation delay (Figure 3)	D	Q	1.9	3.4	ns
		$\overline{LE}$	Q	1.9	4.2	ns

SIMULTANEOUS SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range; V_{REF} = 0.75 V

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ±0.15 V		UNIT
				Min	Max	
t_{pd}	Propagation delay; all outputs switching (Figure 3)	D	Q	1.9	4.4	ns
		$\overline{LE}$	Q	1.9	5.2	ns

VOLTAGE WAVEFORMS

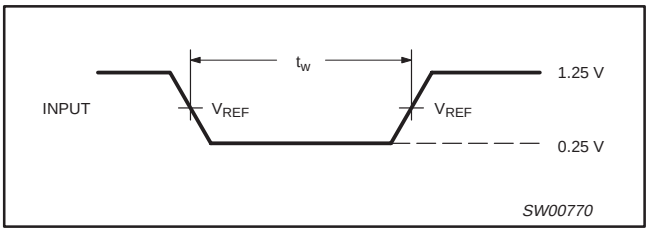


Figure 1. Pulse duration

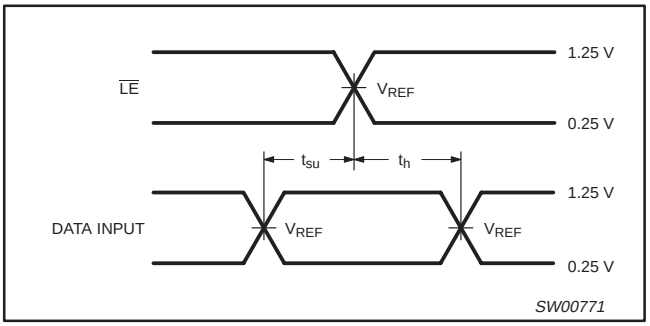


Figure 2. Setup and Hold times

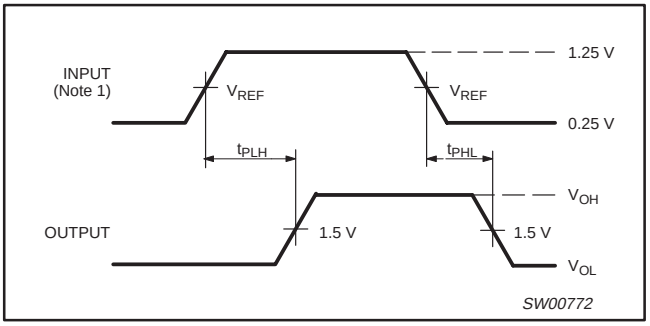
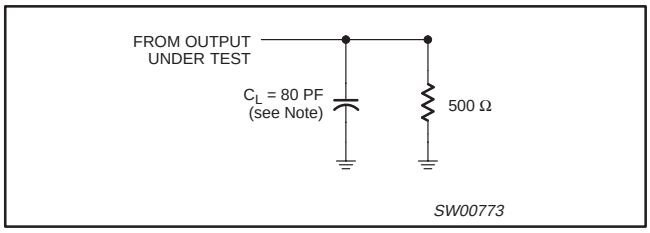


Figure 3. Propagation delay times

NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
2. The outputs are measured one at a time with one transition per measurement.
3. t_{PHL} and t_{PLH} are the same as t_{pd}.

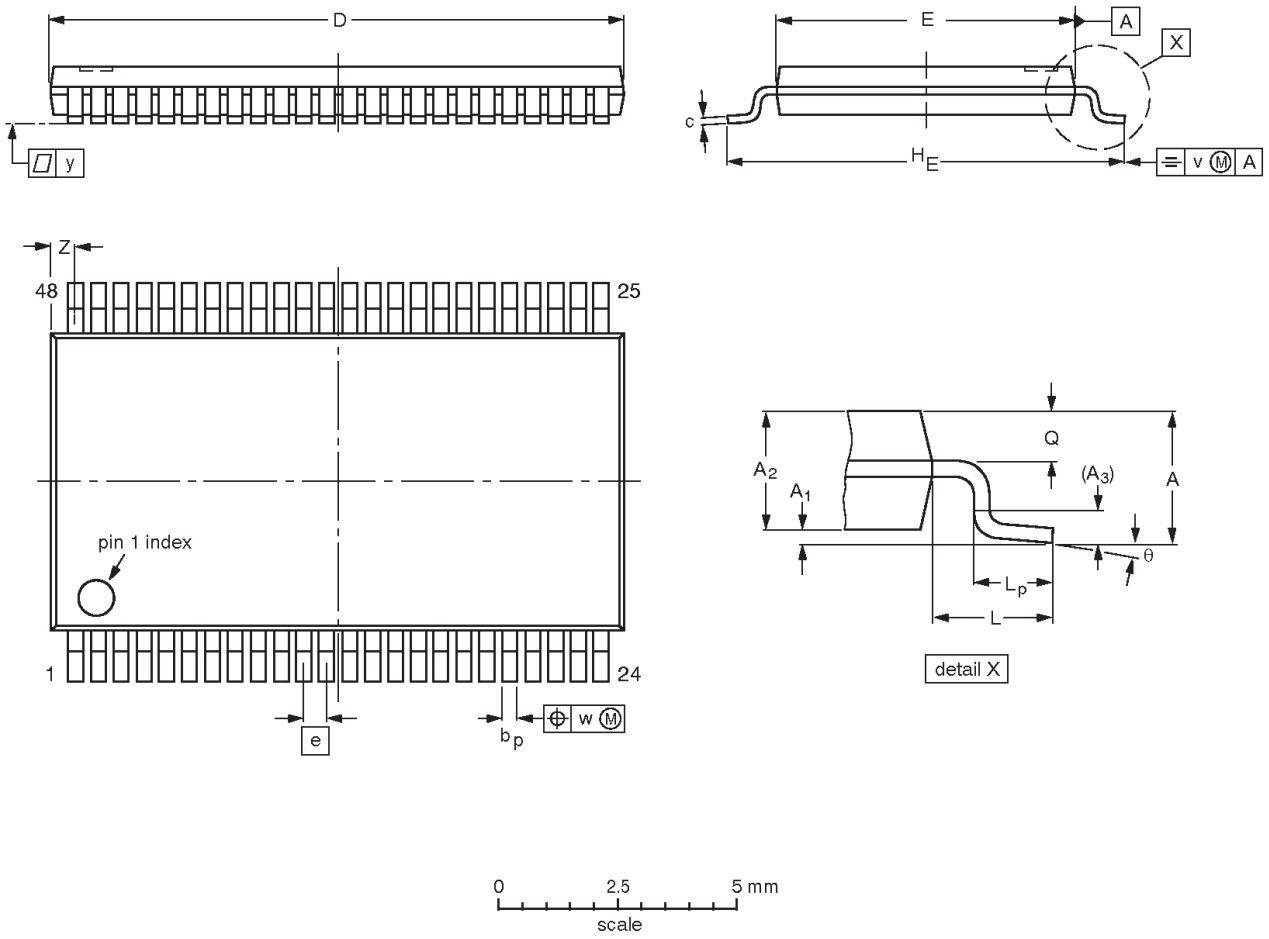
LOAD CIRCUIT



NOTE: C_L includes probe and jig capacitance.

Figure 4. Load circuit

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

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Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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