



HT1660

96×32 LCD Controller for I/O MCU

Technical Document

- [FAQs](#)
- [Application Note](#)

Features

- Operating voltage: 2.7V~5.2V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal oscillator or 32kHz frequency source input
- Standby current: <1μA at 3V, <2μA at 5V
- Internal resistor type: 1/6 bias or 1/5 bias, 1/32 duty, or 1/16 duty
- Three selectable LCD frame frequencies: 64Hz, 89Hz or 170Hz
- Max. 96×32 patterns, 96 segments and 32 commons
- 112 segments and 16 commons selectable by command method
- Built-in bit-map display RAM: 3072 bits (=96×32 bits)
- Built-in internal resistor type bias generator
- Six-wire interface (four data wires)
- Eight kinds of time base/WDT selection
- Time base or WDT overflow output
- R/W address auto increment
- Built-in buzzer driver (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provides VLCD pin to adjust LCD operating voltage and max. VLCD voltage up to 7V
- Provides three kinds of bias current programming
- Control of TN-type and STN-type LCDs
- 208-pin QFP package

Applications

- Leisure products
- Games
- Personal digital assistant
- Cellular phone
- Global positioning system
- Consumer electronics

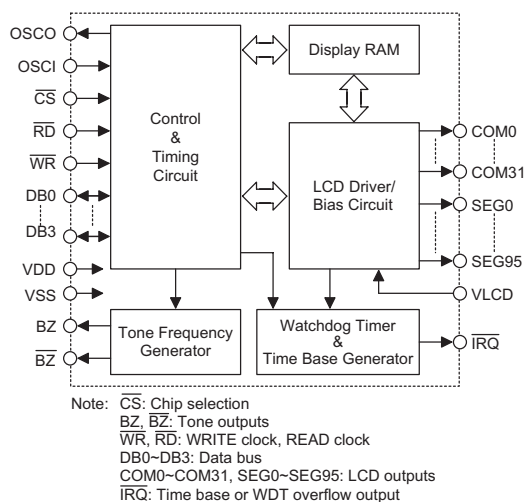
General Description

HT1660 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 3072 patterns (96 segments and 32 commons). It also supports four data bits interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1660 is a memory mapping and multi-function LCD controller. Since the

HT1660 can control TN-type (Twisted Nematic) or STN-type (Super Twisted Nematic) LCDs. The software configuration feature of the HT1660 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only six lines ($\overline{CS}$, $\overline{WR}$, DB0~DB3) are required for the interface between the host controller and the HT1660.



Block Diagram



Pin Assignment

COM23	208	COM22	1	SEG68	156	SEG68
COM21	2	SEG67	155	SEG67		
COM20	3	SEG66	154	SEG66		
COM19	4	SEG65	153	SEG65		
COM18	5	SEG64	152	SEG64		
COM17	6	SEG63	151	SEG63		
COM16	7	SEG62	150	SEG62		
NC	8	SEG61	149	SEG61		
NC	9	SEG60	148	SEG60		
NC	10	SEG59	147	SEG59		
NC	11	SEG58	146	SEG58		
NC	12	SEG57	145	SEG57		
NC	13	SEG56	144	SEG56		
NC	14	SEG55	143	SEG55		
NC	15	SEG54	142	SEG54		
NC	16	SEG53	141	SEG53		
CS	17	SEG52	140	SEG52		
RD	18	SEG51	139	SEG51		
WR	19	SEG50	138	SEG50		
DB0	20	SEG49	137	SEG49		
DB1	21	SEG48	136	SEG48		
DB2	22	NC	135	NC		
DB3	23	NC	134	NC		
VSS	24	NC	133	NC		
OSCI	25	NC	132	NC		
HT1660	26	NC	131	NC		
OSCO	26	NC	131	NC		
VDD	27	NC	130	NC		
VLCD	28	NC	129	NC		
IRQ	29	NC	128	NC		
BZ	30	NC	127	NC		
BZ	31	NC	126	NC		
T1	32	SEG47	125	SEG47		
T2	33	SEG46	124	SEG46		
T3	34	SEG45	123	SEG45		
T4	35	SEG44	122	SEG44		
T000	36	SEG43	121	SEG43		
VLCD	37	SEG42	120	SEG42		
NC	38	SEG41	119	SEG41		
NC	39	SEG40	118	SEG40		
NC	40	SEG39	117	SEG39		
NC	41	SEG38	116	SEG38		
NC	42	SEG37	115	SEG37		
NC	43	SEG36	114	SEG36		
NC	44	SEG35	113	SEG35		
NC	45	SEG34	112	SEG34		
COM0	46	SEG33	111	SEG33		
COM1	47	SEG32	110	SEG32		
COM2	48	SEG31	109	SEG31		
COM3	49	SEG30	108	SEG30		
COM4	50	SEG29	107	SEG29		
COM5	51	SEG28	106	SEG28		
COM6	52	SEG27	105	SEG27		
COM7	53	SEG26	104	SEG26		
COM8	54	SEG25	103	SEG25		
COM9	55	SEG24	102	SEG24		
COM10	56	SEG23	101	SEG23		
COM11	57	SEG22	100	SEG22		
COM12	58	SEG21	99	SEG21		
COM13	59	SEG20	98	SEG20		
COM14	60	SEG19	97	SEG19		
COM15	61	SEG18	96	SEG18		
COM16	62	SEG17	95	SEG17		
COM17	63	SEG16	94	SEG16		
COM18	64	SEG15	93	SEG15		
COM19	65	SEG14	92	SEG14		
COM20	66	SEG13	91	SEG13		
COM21	67	SEG12	90	SEG12		
COM22	68	SEG11	89	SEG11		
COM23	69	SEG10	88	SEG10		
COM24	70	SEG9	87	SEG9		
COM25	71	SEG8	86	SEG8		
COM26	72	SEG7	85	SEG7		
COM27	73	SEG6	84	SEG6		
COM28	74	SEG5	83	SEG5		
COM29	75	SEG4	82	SEG4		
COM30	76	SEG3	81	SEG3		
COM31	77	SEG2	80	SEG2		
COM32	78	SEG1	79	SEG1		
COM33	79	SEG0	78	SEG0		
COM34	80	SEG0	77	SEG0		
COM35	81	SEG0	76	SEG0		
COM36	82	SEG0	75	SEG0		
COM37	83	SEG0	74	SEG0		
COM38	84	SEG0	73	SEG0		
COM39	85	SEG0	72	SEG0		
COM40	86	SEG0	71	SEG0		
COM41	87	SEG0	70	SEG0		
COM42	88	SEG0	69	SEG0		
COM43	89	SEG0	68	SEG0		
COM44	90	SEG0	67	SEG0		
COM45	91	SEG0	66	SEG0		
COM46	92	SEG0	65	SEG0		
COM47	93	SEG0	64	SEG0		
COM48	94	SEG0	63	SEG0		
COM49	95	SEG0	62	SEG0		
COM50	96	SEG0	61	SEG0		
COM51	97	SEG0	60	SEG0		
COM52	98	SEG0	59	SEG0		
COM53	99	SEG0	58	SEG0		
COM54	100	SEG0	57	SEG0		
COM55	101	SEG0	56	SEG0		
COM56	102	SEG0	55	SEG0		
COM57	103	SEG0	54	SEG0		
COM58	104	SEG0	53	SEG0		
COM59	105	SEG0	52	SEG0		
COM60	106	SEG0	51	SEG0		
COM61	107	SEG0	50	SEG0		
COM62	108	SEG0	49	SEG0		
COM63	109	SEG0	48	SEG0		
COM64	110	SEG0	47	SEG0		
COM65	111	SEG0	46	SEG0		
COM66	112	SEG0	45	SEG0		
COM67	113	SEG0	44	SEG0		
COM68	114	SEG0	43	SEG0		
COM69	115	SEG0	42	SEG0		
COM70	116	SEG0	41	SEG0		
COM71	117	SEG0	40	SEG0		
COM72	118	SEG0	39	SEG0		
COM73	119	SEG0	38	SEG0		
COM74	120	SEG0	37	SEG0		
COM75	121	SEG0	36	SEG0		
COM76	122	SEG0	35	SEG0		
COM77	123	SEG0	34	SEG0		
COM78	124	SEG0	33	SEG0		
COM79	125	SEG0	32	SEG0		
COM80	126	SEG0	31	SEG0		
COM81	127	SEG0	30	SEG0		
COM82	128	SEG0	29	SEG0		
COM83	129	SEG0	28	SEG0		
COM84	130	SEG0	27	SEG0		
COM85	131	SEG0	26	SEG0		
COM86	132	SEG0	25	SEG0		
COM87	133	SEG0	24	SEG0		
COM88	134	SEG0	23	SEG0		
COM89	135	SEG0	22	SEG0		
COM90	136	SEG0	21	SEG0		
COM91	137	SEG0	20	SEG0		
COM92	138	SEG0	19	SEG0		
COM93	139	SEG0	18	SEG0		
COM94	140	SEG0	17	SEG0		
COM95	141	SEG0	16	SEG0		
COM96	142	SEG0	15	SEG0		
COM97	143	SEG0	14	SEG0		
COM98	144	SEG0	13	SEG0		
COM99	145	SEG0	12	SEG0		
COM100	146	SEG0	11	SEG0		
COM101	147	SEG0	10	SEG0		
COM102	148	SEG0	9	SEG0		
COM103	149	SEG0	8	SEG0		
COM104	150	SEG0	7	SEG0		
COM105	151	SEG0	6	SEG0		
COM106	152	SEG0	5	SEG0		
COM107	153	SEG0	4	SEG0		
COM108	154	SEG0	3	SEG0		
COM109	155	SEG0	2	SEG0		
COM110	156	SEG0	1	SEG0		

The diagram illustrates the pinout of the PIC16C62 microcontroller. The pins are arranged in a 40-pin package. The top row of pins (1-20) are labeled SEG63 to SEG62. The bottom row of pins (21-40) are labeled COM15 to COM3. The left side of the package has pins 1-20 labeled SEG63 to SEG62. The right side has pins 21-40 labeled COM15 to COM3. A coordinate system (0,0) is shown at the center of the package.

Pin	Label
1	SEG63
2	SEG64
3	SEG65
4	SEG66
5	SEG67
6	SEG68
7	SEG69
8	SEG70
9	SEG71
10	SEG72
11	SEG73
12	SEG74
13	SEG75
14	SEG76
15	SEG77
16	SEG78
17	SEG79
18	SEG80
19	SEG81
20	SEG82
21	SEG83
22	SEG84
23	SEG85
24	SEG86
25	SEG87
26	SEG88
27	SEG89
28	SEG90
29	SEG91
30	SEG92
31	SEG93
32	SEG94
33	SEG95
34	COM31
35	COM30
36	COM29
37	COM28
38	COM27
39	COM26
40	COM25
41	COM24
42	COM23
43	COM22
44	COM21
45	COM20
46	COM19

Chip size: 4340×5030 (μm)²

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	-2028.50	2237.20	51	-1027.85	-2225.20	101	2028.45	654.20
2	-2028.50	2137.20	52	-892.45	-2225.20	102	2028.45	754.20
3	-2028.50	2037.20	53	-745.55	-2225.20	103	2028.45	854.20
4	-2028.50	1937.20	54	-610.15	-2225.20	104	2028.45	954.20
5	-2028.50	1837.20	55	-464.85	-2225.20	105	2028.45	1054.20
6	-2028.50	1637.20	56	-329.25	-2225.20	106	2028.45	1154.20
7	-2028.50	1537.20	57	-187.15	-2225.30	107	2028.45	1254.20
8	-2028.50	1437.20	58	-53.65	-2229.70	108	2028.45	1354.20
9	-2028.50	1337.20	59	84.55	-2229.70	109	2028.45	1454.20
10	-2028.50	1237.20	60	222.85	-2297.35	110	2028.45	1554.20
11	-2028.50	1237.20	61	310.40	-2162.35	111	2028.45	1654.20
12	-2028.50	1137.20	62	492.00	-2183.60	112	2028.45	1754.20
13	-2028.50	1037.20	63	638.50	-2225.30	113	2028.45	1854.20
14	-2028.50	937.20	64	773.90	-2225.30	114	2028.45	1954.20
15	-2028.50	837.20	65	933.50	-2225.30	115	2028.45	2054.20
16	-2028.50	737.20	66	1081.70	-2225.30	116	2028.45	2154.20
17	-2028.50	637.20	67	1228.70	-2225.30	117	2028.45	2254.20
18	-2028.50	537.20	68	1376.90	-2225.30	118	1550.75	2349.60
19	-2028.50	437.20	69	1523.90	-2225.30	119	1450.75	2349.60
20	-2028.50	337.20	70	1662.50	-2225.30	120	1350.75	2349.60
21	-2028.50	237.20	71	1821.19	-2338.90	121	1250.75	2349.60
22	-2028.50	137.20	72	1921.19	-2338.90	122	1150.75	2349.60
23	-2028.50	37.20	73	2021.19	-2338.90	123	1050.75	2349.60
24	-2028.50	-62.80	74	2028.45	-2051.10	124	950.75	2349.60
25	-2028.50	-162.80	75	2028.45	-1951.10	125	850.75	2349.60
26	-2028.50	-262.80	76	2028.45	-1851.10	126	750.75	2349.60
27	-2028.50	-362.80	77	2028.45	-1751.10	127	650.75	2349.60
28	-2028.50	-462.80	78	2028.45	-1651.10	128	550.75	2349.60
29	-2028.50	-562.80	79	2028.45	-1551.10	129	450.75	2349.60
30	-2028.50	-662.80	80	2028.45	-1451.10	130	350.75	2349.60
31	-2028.50	-762.80	81	2028.45	-1351.10	131	250.75	2349.60
32	-2028.50	-862.80	82	2028.45	-1251.10	132	150.75	2349.60
33	-2028.50	-962.80	83	2028.45	-1151.10	133	50.75	2349.60
34	-2028.50	-1062.80	84	2028.45	-1051.10	134	-49.25	2349.60
35	-2028.50	-1162.80	85	2028.45	-951.10	135	-149.25	2349.60
36	-2028.50	-1262.80	86	2028.45	-851.10	136	-249.25	2349.60
37	-2028.50	-1362.80	87	2028.45	-745.80	137	-349.25	2349.60
38	-2028.50V	-1462.80	88	2028.45	-645.80	138	-449.25	2349.60
39	-2028.50	-1562.80	89	2028.45	-545.80	139	-549.25	2349.60
40	-2028.50	-1662.80	90	2028.45	-445.80	140	-649.25	2349.60
41	-2028.50	-1762.80	91	2028.45	-345.80	141	-749.25	2349.60
42	-2028.50	-1862.80	92	2028.45	-245.80	142	-849.25	2349.60
43	-2028.50	-1962.80	93	2028.45	-145.80	143	-949.25	2349.60
44	-2028.50	-2062.80	94	2028.45	-45.80	144	-1049.25	2349.60
45	-2028.50	-2162.80	95	2028.45	54.20	145	-1149.25	2349.60
46	-2028.50	-2262.80	96	2028.45	154.20	146	-1249.25	2349.60
47	-1523.55	-2337.10	97	2028.45	254.20	147	-1349.25	2349.60
48	-1423.55	-2337.10	98	2028.45	354.20	148	-1449.25	2349.60
49	-1323.55	-2337.10	99	2028.45	454.20	149	-1549.25	2349.60
50	-1170.45	-2225.20	100	2028.45	554.20			

Pad Description

Pad No.	Pad Name	I/O	Description
1~33 87~149	SEG63~SEG95 SEG0~SEG62	O	LCD segment outputs
34~49 71~86	COM31~COM16 COM0~COM15	O	LCD common outputs, under 112×16 command mode, COM16~COM31 will share to SEG96~SEG111. COM31/SEG96, COM30/SEG97, COM29/SEG98....., COM18/SEG109, COM17/SEG110, COM16/SEG111
50	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1660 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1660 are all enabled.
51	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1660 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
52	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1660 on the rising edge of the $\overline{WR}$ signal.
53~56	DB0~DB3	I/O	Parallel data input/output with a pull-high resistor
57	VSS	—	Negative power supply for logic circuit, ground
58 59	OSCI OSCO	I O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected, the OSCI and OSCO pads can be left open.
60	VDD	—	Positive power supply for logic circuit
61	VLCD	I	Power supply for LCD driver circuit
62	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
63, 64	BZ, $\overline{BZ}$	O	2kHz or 4kHz frequency output pair (tristate output buffer)
65~69	T1~T4, T000	I	Vary bias current pin It is usually not connected

Absolute Maximum Ratings

Supply Voltage	$V_{SS}-0.3V$ to $V_{SS}+5.5V$	Storage Temperature	-50°C to 125°C
Input Voltage	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	Operating Temperature	-25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I _{DD1}	Operating Current	3V	No load/LCD ON	—	150	250	μA
		5V	On-chip RC oscillator	—	250	370	μA
I _{DD2}	Operating Current	3V	No load/LCD ON	—	135	200	μA
		5V	Crystal oscillator	—	200	300	μA
I _{DD11}	Operating Current	3V	No load/LCD OFF	—	15	30	μA
		5V	On-chip RC oscillator	—	50	70	μA
I _{DD22}	Operating Current	3V	No load/LCD OFF	—	2	10	μA
		5V	Crystal oscillator	—	3	10	μA
I _{STB}	Standby Current	3V	No load, Power down mode	—	—	1	μA
		5V		—	—	2	μA
V _{IL}	Input Low Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V _{IH}	Input High Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I _{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$ Sink Current	3V	V _{OL} =0.3V	1.2	2.5	—	mA
		5V	V _{OL} =0.5V	3	6	—	mA
I _{OH1}	BZ, $\overline{BZ}$ Source Current	3V	V _{OH} =2.7V	-0.9	-1.8	—	mA
		5V	V _{OH} =4.5V	-2	-4	—	mA
I _{OL2}	DB0~DB3 Sink Current	3V	V _{OL} =0.3V	1.2	2.5	—	mA
		5V	V _{OL} =0.5V	3	6	—	mA
I _{OH2}	DB0~DB3 Source Current	3V	V _{OH} =2.7V	-0.9	-1.8	—	mA
		5V	V _{OH} =4.5V	-2	-4	—	mA
I _{OL3}	LCD Common Sink Current	3V	V _{OL} =0.3V	80	160	—	μA
		5V	V _{OL} =0.5V	180	360	—	μA
I _{OH3}	LCD Common Source Current	3V	V _{OH} =2.7V	-40	-80	—	μA
		5V	V _{OH} =4.5V	-90	-180	—	μA
I _{OL4}	LCD Segment Sink Current	3V	V _{OL} =0.3V	50	100	—	μA
		5V	V _{OL} =0.5V	120	240	—	μA
I _{OH4}	LCD Segment Source Current	3V	V _{OH} =2.7V	-30	-60	—	μA
		5V	V _{OH} =4.5V	-70	-140	—	μA
R _{PH}	Pull-high Resistor	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	150	250	410	kΩ
		5V		60	125	210	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
f _{SYS1}	System Clock	3V	On-chip RC oscillator	22	32	40	kHz
		5V		24	32	40	kHz
f _{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f _{SYS3}	System Clock	3V	External clock source	—	32	—	kHz
		5V		—	32	—	kHz
f _{LCD1}	LCD Frame Frequency	3V	On-chip RC oscillator	61/117	89/170	111/213	Hz
		5V		61/117	89/170	111/213	Hz
f _{LCD2}	LCD Frame Frequency	3V	Crystal oscillator	—	64	—	Hz
		5V		—	64	—	Hz
f _{LCD3}	LCD Frame Frequency	3V	External clock source	—	64	—	Hz
		5V		—	64	—	Hz
t _{COM}	LCD Common Period	—	n: Number of COM	—	n/f _{LCD}	—	sec
f _{CLK1}	4-Bit Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f _{CLK2}	4-Bit Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t _{CS}	4-Bit Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t _{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34			
t _r , t _f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t _{su}	Setup Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t _h	Hold Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t _{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t _{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

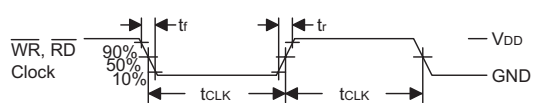


Figure 1

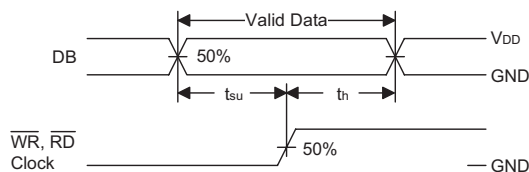


Figure 2

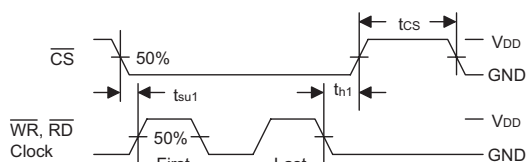


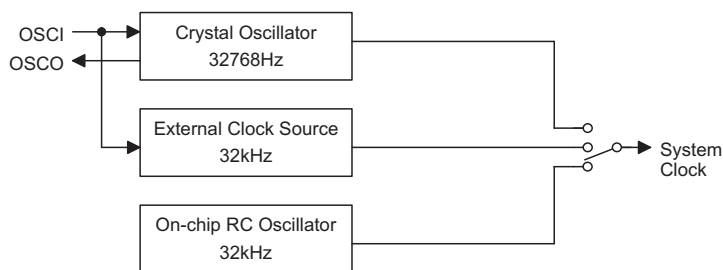
Figure 3

Functional Description

System Oscillator

The HT1660 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The clock source may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 32kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT loses its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, thus serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSC1 pin. In this case, the system fails to enter the power down mode, similar to the case in the external 32kHz clock source operation. At the initial system power on, the HT1660 is at the SYS DIS state.



System Oscillator Configuration

Display Memory – RAM Structure

The static display RAM is organized into 768×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	00H	08H	10H	18H	20H - - - - - 2D8H	2E0H	2E8H	2F0H	2F8H
COM0	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM1	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM2	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM3	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	01H	09H	11H	19H	21H - - - - - 2D9H	2E1H	2E9H	2F1H	2F9H
COM4	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM5	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM6	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM7	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	02H	0AH	12H	1AH	22H - - - - - 2DAH	2E2H	2EAH	2F2H	2FAH
COM8	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM9	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM10	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM11	Bit3	Bit3	Bit03				Bit3	Bit3	Bit3
	03H	0BH	13H	1BH	23H - - - - - 2DBH	2E3H	2EBH	2F3H	2FBH
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	04H	0CH	14H	1CH	24H - - - - - 2DCH	2E4H	2ECH	2F4H	2FCH
COM16	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM17	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM18	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM19	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	05H	0DH	15H	1DH	25H - - - - - 2DDH	2E5H	2EDH	2F5H	2FDH
COM20	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM21	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM22	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM23	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	06H	0EH	16H	1EH	26H - - - - - 2DEH	2E6H	2EEH	2F6H	2FEH
COM24	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM25	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM26	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM27	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	07H	0FH	17H	1FH	27H - - - - - 2DFH	2E7H	2EFH	2F7H	2FFH
COM28	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM29	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM30	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM31	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	SEG1	SEG2	SEG3		SEG92	SEG93	SEG94	SEG95

96×32 Selection Mode RAM Mapping Table

	00H	04H	08H	0CH	10H-----1ACH	1B0H	1B4H	1B8H	1BCH
COM0	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM1	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM2	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM3	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	01H	05H	09H	0DH	11H-----1ADH	1B1H	1B5H	1B9H	1BDH
COM4	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM5	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM6	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM7	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	02H	06H	0AH	0EH	12H-----1AEH	1B2H	1B6H	1BAH	1BEH
COM8	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM9	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM10	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM11	Bit3	Bit3	Bit3s				Bit3	Bit3	Bit3
	03H	07H	0BH	0FH	13H-----1AFH	1B3H	1B7H	1BBH	1BFH
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	SEG1	SEG2	SEG3		SEG108	SEG109	SEG110	SEG111

112×16 Selection Mode RAM Mapping Table

Name	Command Code	Function
112×16 Mode	X100-0001-1111-XXXX	Change segment from 96 to 112 and common from 32 to 16
The default value after power ON reset is 96×32 mode, set "Normal" command will change 112×16 mode to 96×32 mode.		

Frame Frequency

HT1660 provides three kinds of frame frequency option by command code; 64Hz, 89Hz and 170Hz respectively. FRAME 64Hz provides 64Hz frame frequency. FRAME 89Hz provides 89Hz frame frequency. FRAME 170Hz provides 170Hz frame frequency.

Name	Command Code	Function
FRAME 170Hz	X100-0001-1000-XXXX	Select 170Hz frame frequency
FRAME 89Hz	X100-0001-1101-XXXX	Select 89Hz frame frequency
FRAME 64Hz	X100-0001-1110-XXXX	Select 64Hz frame frequency

Frame Frequency Selection Command Code

Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same counter which is divided by 256. The $\overline{\text{IRQ}}$ clock can be programmed as 1Hz, 2Hz, ..., 128Hz output. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{\text{IRQ}}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{\text{IRQ}}$ pin will remain at a logic low level until the CLR WDT or the $\overline{\text{IRQ}}$ DIS command is issued.

If an external clock is selected as the system frequency source, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

A simple tone generator is implemented in the HT1660. The tone generator can output a pair of differential driving signals on the BZ and $\overline{\text{BZ}}$ which are used to generate a single tone.

By executing the TONE 4K and TONE 2K commands there are two tone frequency outputs selectable that can turn on the tone output. The TONE 4K and TONE 2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned off by invoking the TONE OFF command. The tone outputs, namely BZ and $\overline{\text{BZ}}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{\text{BZ}}$ outputs will remain at low level.

Command Format

The HT1660 can be configured by software setting. There are two mode commands to configure the HT1660 resource and to transfer the LCD display data.

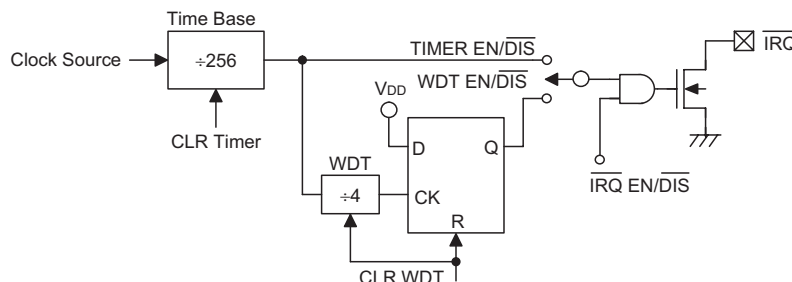
The configuration mode of the HT1660 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration

command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a bias current selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{\text{CS}}$ pin should be set to "1" and the previous operation mode will also be reset. The $\overline{\text{CS}}$ pin returns to "0", so a new operation mode ID should be issued first.



Time Base and WDT Configurations

Name	Command Code	Function
TONE OFF	X100 -0000-1000-XXXX	Turn-off tone output
TONE 4K	X100 -0001-0000-XXXX	Turn-on tone output, tone frequency is 4kHz
TONE 2K	X100 -0001-0001-XXXX	Turn-on tone output, tone frequency is 2kHz

Buzzer Tone Output Command Code

The following are the data mode ID and the command ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive address data mode, the $\overline{\text{CS}}$ pin should be set 1 and the previous operation mode will also be reset. The $\overline{\text{CS}}$ pin returns to 0, so a new operation mode ID should be issued first.

Bias Generator

The HT1660 bias voltage belongs to internal resistor type. It provides two kinds of bias option named 1/6 bias and 1/5 bias respectively. It also provides three kinds of bias current option by programming to suitably drive an LCD panel. The three kinds of bias current are large, middle, and small, respectively. Usually, large panel LCD can be excellently displayed by large bias current. Relatively, it consumes large current when LCD ON command is used. Small bias current provides low power consumption during on condition when the LCD is normally displayed. The following are the reference value table.

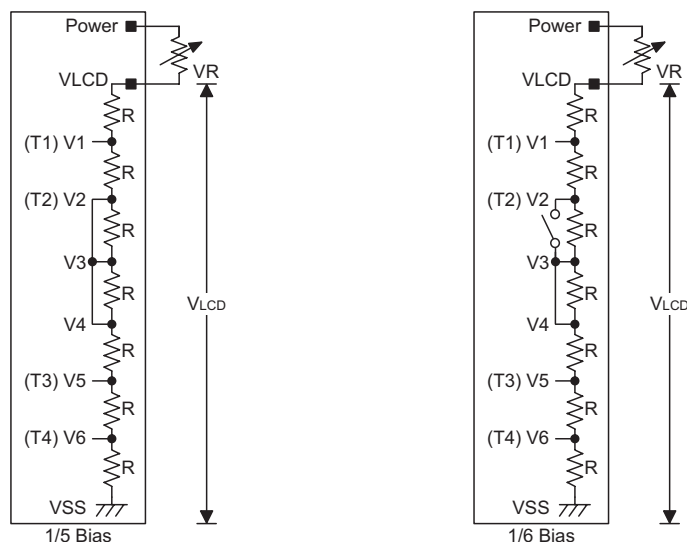
When the bias current for LCD is more than Large Bias Current setting. It is recommended to add external circuit to increase driving current.

Interfacing

Only six lines are required to interface with the HT1660. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1660. If the $\overline{CS}$ pin is set to 1, the

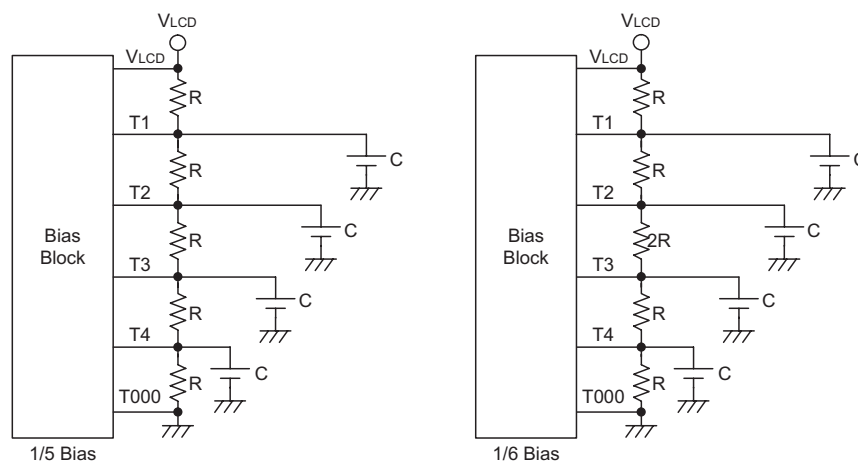
data and command issued between the host controller and the HT1660 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1660. The DB0~DB3 are the 4-bit parallel data input/output lines. Data to be read or written or commands to be written have to pass through the DB0~DB3 lines. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DB0~DB3 lines. It is recommended that the host controller read correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DB0~DB3 lines are all clocked into the HT1660 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1660. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the $\overline{IRQ}$ pin of the HT1660.

Bias	VLCD	Large Bias Current	Middle Bias Current	Small Bias Current
1/5	3V	165 μ A	70 μ A	30 μ A
	5V	270 μ A	110 μ A	50 μ A
1/6	3V	140 μ A	55 μ A	25 μ A
	5V	225 μ A	90 μ A	40 μ A



Internal Resistor Type Bias Generator Configurations

Note: The voltage applied to VLCD pin must be lower than 7V
Adjust VR to fit LCD display

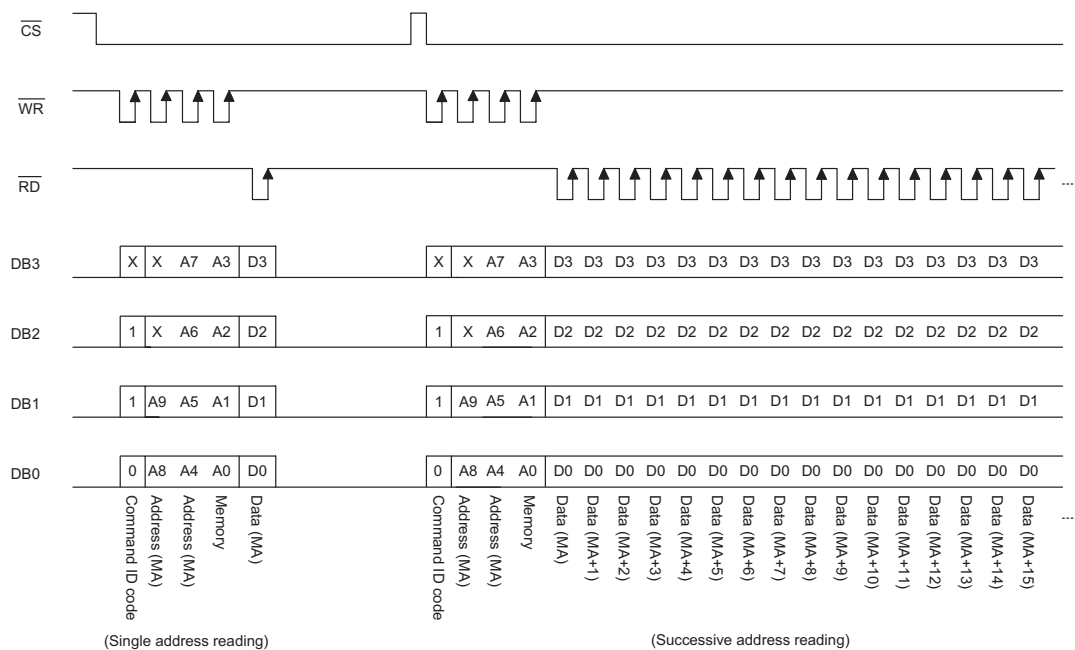


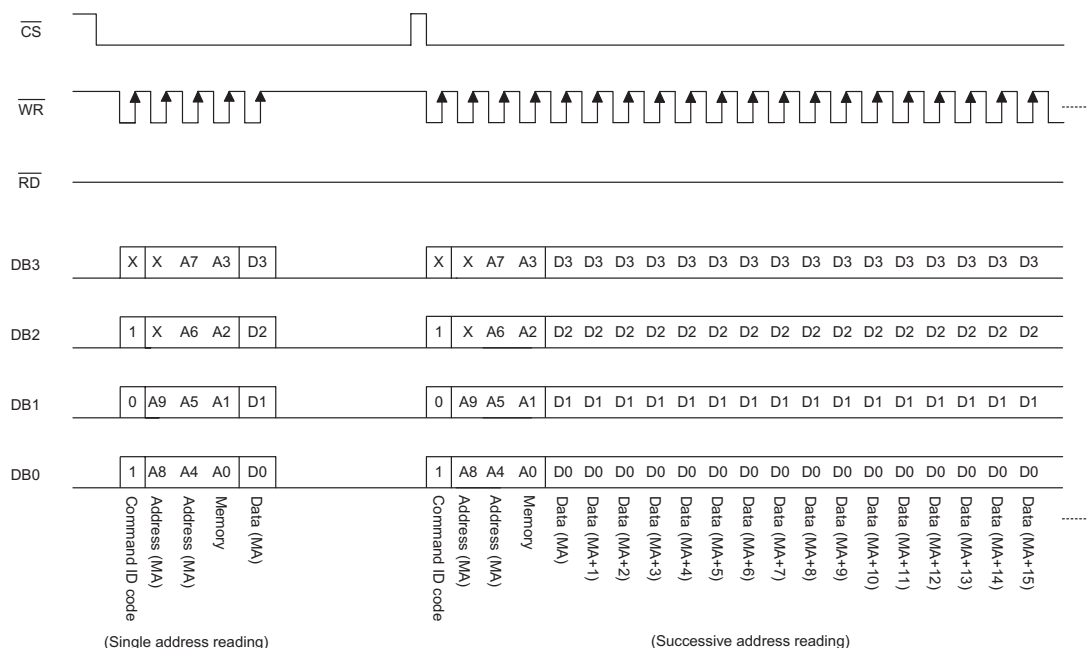
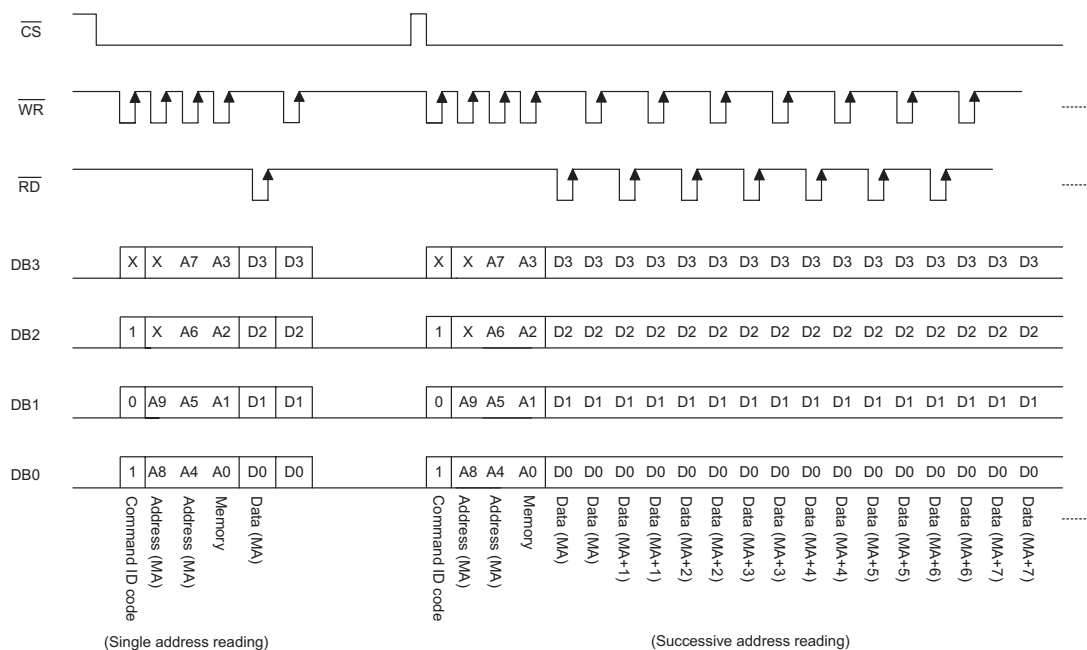
Increase Driver Current Configurations

Note: The external resistors are used to increment the driving current.
And the external capacitors are used to keep the bias voltage stable.

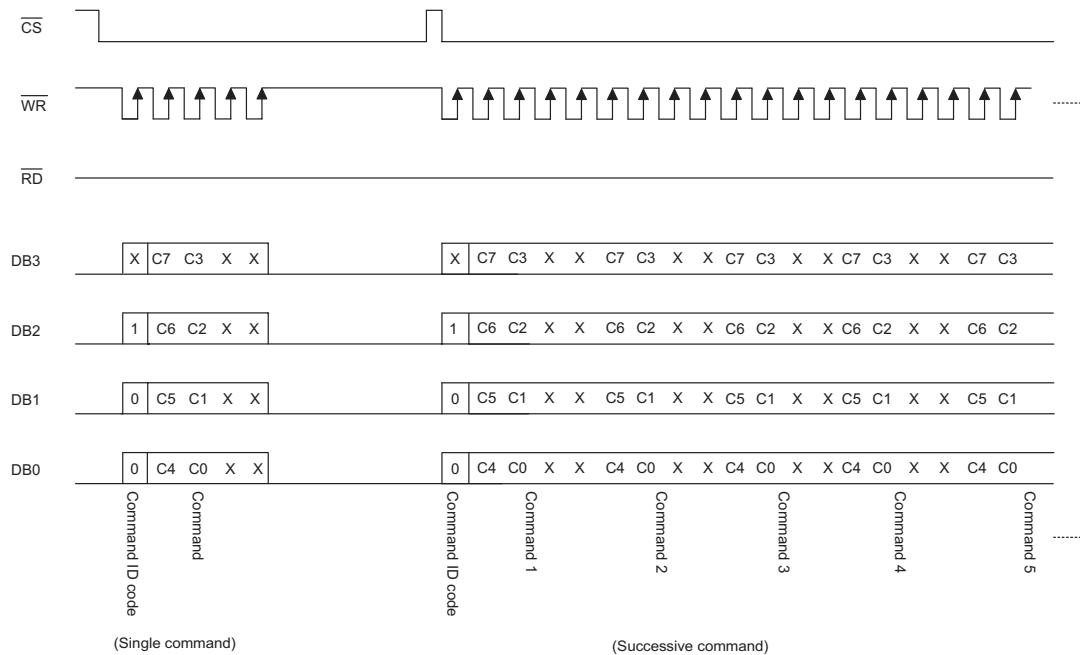
Timing Diagrams

READ Mode (Command ID Code: 1 1 0)



WRITE Mode (Command ID Code: 1 0 1)

READ-MODIFY-WRITE Mode (Command ID Code: 1 0 1)


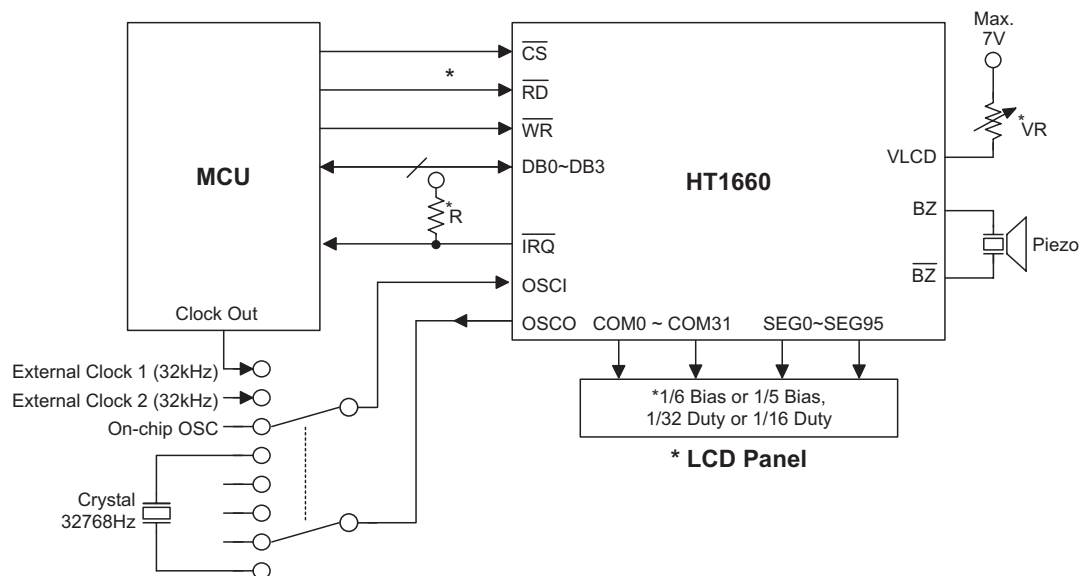
Command Mode (Command ID Code: 1 0 0)



Note: "X" stands for don't care

Application Circuits

Host Controller With an HT1660 Display System



*Note: The connection of $\overline{\text{IRQ}}$ and $\overline{\text{RD}}$ pin can be selected depending on the MCU.

Adjust VR to fit LCD display

Adjust R (external pull-high resistance) to fit user's time base clock.

It is recommended that the internal equivalent capacitance between SEG and COM of LCD panel should be lower than 10pF. (LCR meter test condition: frequency in 1KHz)

Instruction Set Summary

Name	Command Code	D/C	Function	Def.
READ	X110-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Read data from the RAM	
WRITE	X101-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Write data to the RAM	
READ-MODIFY-WRITE	X101-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Read and Write data to the RAM	
SYS DIS	X100-0000-0000-XXXX-XXXX	C	Turn Off both system oscillator and LCD bias generator	Yes
SYS EN	X100-0000-0001-XXXX-XXXX	C	Turn On system oscillator	
LCD OFF	X100-0000-0010-XXXX-XXXX	C	Turn Off LCD display	Yes
LCD ON	X100-0000-0011-XXXX-XXXX	C	Turn On LCD display	
TIMER DIS	X100-0000-0100-XXXX-XXXX	C	Disable time base output	Yes
WDT DIS	X100-0000-0101-XXXX-XXXX	C	Disable WDT time-out flag output	Yes
TIMER EN	X100-0000-0110-XXXX-XXXX	C	Enable time base output	
WDT EN	X100-0000-0111-XXXX-XXXX	C	Enable WDT time-out flag output	
TONE OFF	X100-0000-1000-XXXX-XXXX	C	Turn Off tone outputs	Yes
CLR TIMER	X100-0000-1101-XXXX-XXXX	C	Clear the contents of the time base generator	
CLR WDT	X100-0000-1111-XXXX-XXXX	C	Clear the contents of the WDT stage	
TONE 4K	X100-0001-0000-XXXX-XXXX	C	Turn on tone output, tone frequency output: 4kHz	
TONE 2K	X100-0001-0001-XXXX-XXXX	C	Turn on tone output, tone frequency output: 2kHz	
IRQ DIS	X100-0001-0010-XXXX-XXXX	C	Disable $\overline{\text{IRQ}}$ output	Yes
IRQ EN	X100-0001-0011-XXXX-XXXX	C	Enable $\overline{\text{IRQ}}$ output	
RC 32K	X100-0001-0100-XXXX-XXXX	C	System clock source, on-chip RC oscillator	Yes
EXT (X'TAL)	X100-0001-0101-XXXX-XXXX	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
LARGE BIAS	X100-0001-0110-XXXX-XXXX	C	Large bias current option	Yes
MIDDLE BIAS	X100-0001-0111-XXXX-XXXX	C	Middle bias current option	
SMALL BIAS	X100-0001-1000-XXXX-XXXX	C	Small bias current option	
BIAS 1/6	X100-0001-1010-XXXX-XXXX	C	LCD 1/6 bias option	Yes
BIAS 1/5	X100-0001-1001-XXXX-XXXX	C	LCD 1/5 bias option	
FRAME 170Hz	X100-0001-1100-XXXX-XXXX	C	Selects 170Hz frame frequency	
FRAME 89Hz	X100-0001-1101-XXXX-XXXX	C	Selects 89Hz frame frequency	
FRAME 64Hz	X100-0001-1110-XXXX-XXXX	C	Selects 64Hz frame frequency	Yes
Select 112×16	X100-0001-1111-XXXX-XXXX	C	This command will change segment from 96 to 112 and command from 32 to 16	
F1	X100-1010-0000-XXXX-XXXX	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	X100-1010-0001-XXXX-XXXX	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	X100-1010-0010-XXXX-XXXX	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	

Name	Command Code	D/C	Function	Def.
F8	X100-1010-0011-XXXX-XXXX	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	X100-1010-0100-XXXX-XXXX	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	X100-1010-0101-XXXX-XXXX	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	X100-1010-0110-XXXX-XXXX	C	Time base clock output: 96Hz The time-out flag after: 1/16s	
F128	X100-1010-0111-XXXX-XXXX	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	X100-1111-1111-XXXX-XXXX	C	Test mode, user don't use.	
NORMAL	X100-1111-1110-XXXX-XXXX	C	Normal mode, 96×32 mode will be set	Yes

Note: "X" stands for don't care

A9~A0: RAM address

D3~D0: RAM data

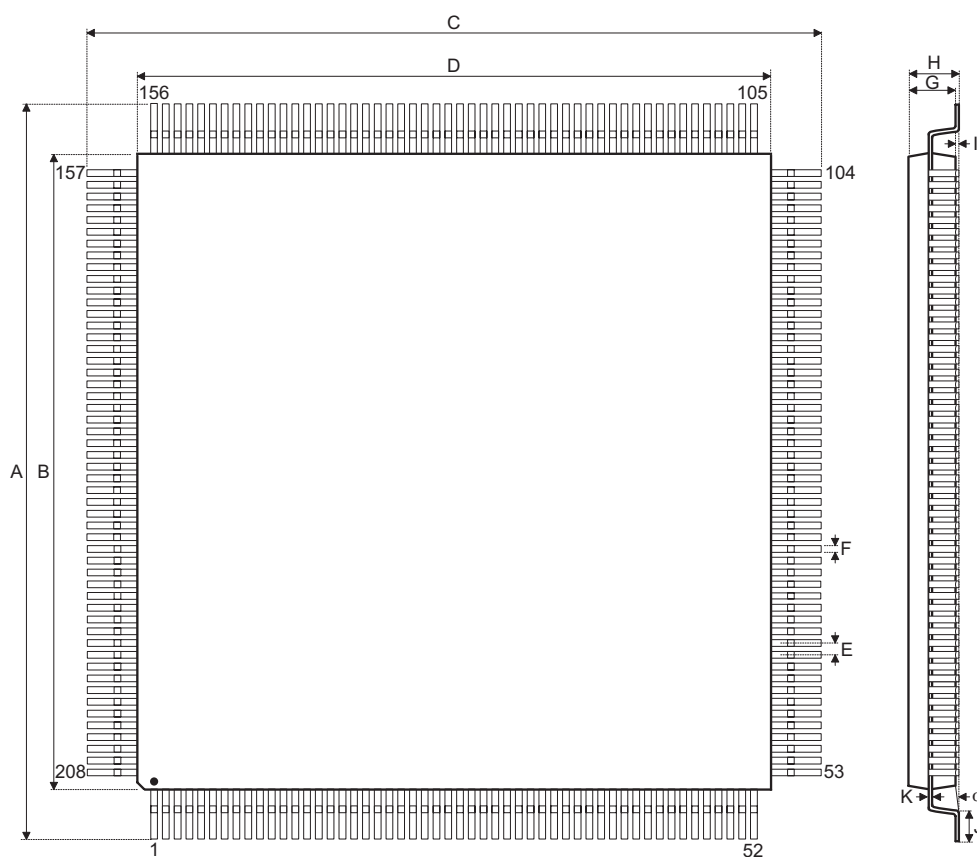
D/C: Data/Command mode

Def.: Power-on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The tone frequency source and the time base/WDT clock frequency source can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1660 after power-on reset, otherwise, power on reset may fail, which in turn leads to the malfunctioning of the HT1660.

Package Information

208-pin QFP (28×28) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	31	—	31.4
B	27.9	—	28.1
C	31	—	31.4
D	27.9	—	28.1
E	—	0.5	—
F	—	0.2	—
G	3.1	—	3.4
H	—	—	3.7
I	—	0.1	—
J	0.35	—	0.65
K	0.1	—	0.2
α	0°	—	7°

Holtek Semiconductor Inc. (Headquarters)

No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
<http://www.holtek.com.tw>

Holtek Semiconductor Inc. (Taipei Sales Office)

4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shanghai Sales Office)

7th Floor, Building 2, No.889, Yi Shan Rd., Shanghai, China 200233
Tel: 021-6485-5560
Fax: 021-6485-0313
<http://www.holtek.com.cn>

Holtek Semiconductor Inc. (Shenzhen Sales Office)

5/F, Unit A, Productivity Building, Cross of Science M 3rd Road and Gaoxin M 2nd Road, Science Park, Nanshan District, Shenzhen, China 518057
Tel: 0755-8616-9908, 8616-9308
Fax: 0755-8616-9533

Holtek Semiconductor Inc. (Beijing Sales Office)

Suite 1721, Jinyu Tower, A129 West Xuan Wu Men Street, Xicheng District, Beijing, China 100031
Tel: 010-6641-0030, 6641-7751, 6641-7752
Fax: 010-6641-0125

Holtek Semiconductor Inc. (Chengdu Sales Office)

709, Building 3, Champagne Plaza, No.97 Dongda Street, Chengdu, Sichuan, China 610016
Tel: 028-6653-6590
Fax: 028-6653-6591

Holmate Semiconductor, Inc. (North America Sales Office)

46729 Fremont Blvd., Fremont, CA 94538
Tel: 510-252-9880
Fax: 510-252-9885
<http://www.holmate.com>

Copyright © 2006 by HOLTEK SEMICONDUCTOR INC.

The information appearing in this Data Sheet is believed to be accurate at the time of publication. However, Holtek assumes no responsibility arising from the use of the specifications described. The applications mentioned herein are used solely for the purpose of illustration and Holtek makes no warranty or representation that such applications will be suitable without further modification, nor recommends the use of its products for application that may present a risk to human life due to malfunction or otherwise. Holtek's products are not authorized for use as critical components in life support devices or systems. Holtek reserves the right to alter its products without prior notification. For the most up-to-date information, please visit our web site at <http://www.holtek.com.tw>.