RENESAS

HVD396C

Variable Capacitance Diode for VCO

REJ03G0213-0200
Rev.2.00
Mar 30, 2006

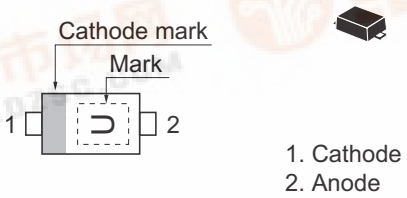
Features

- High capacitance ratio. (n = 2.62 min)
- Low series resistance. (rs = 0.40 Ω max)
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVD396C	U	SFP	PUSF0002ZB-A

Pin Arrangement



1. Cathode
2. Anode

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	10	V
Junction temperature	Tj	125	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I_{R1}	—	—	10	nA	V_R = 10 V
	I_{R2}	—	—	50		V_R = 10 V, Ta = 60°C
Capacitance	C_1	14.6	—	15.8	pF	V_R = 1 V, f = 1 MHz
	C_4	5.20	—	5.80		V_R = 4 V, f = 1 MHz
Capacitance ratio	n	2.62	—	—	—	C_1 / C_4
Series resistance	r_S	—	—	0.40	Ω	V_R = 1 V, f = 470 MHz

Note: For SFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

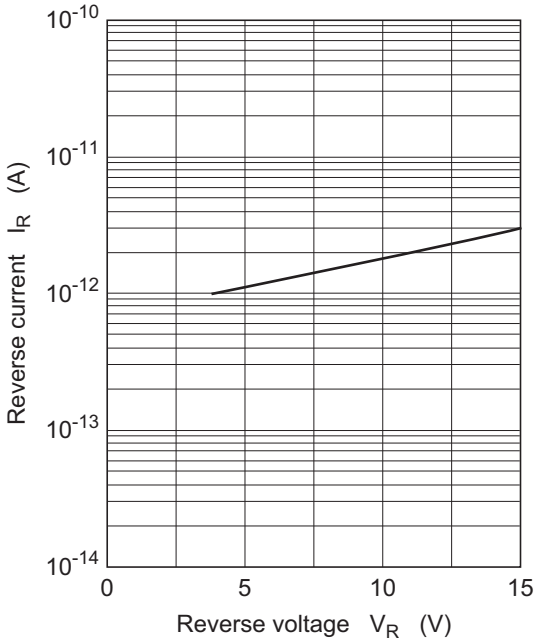


Fig.1 Reverse current vs. Reverse voltage

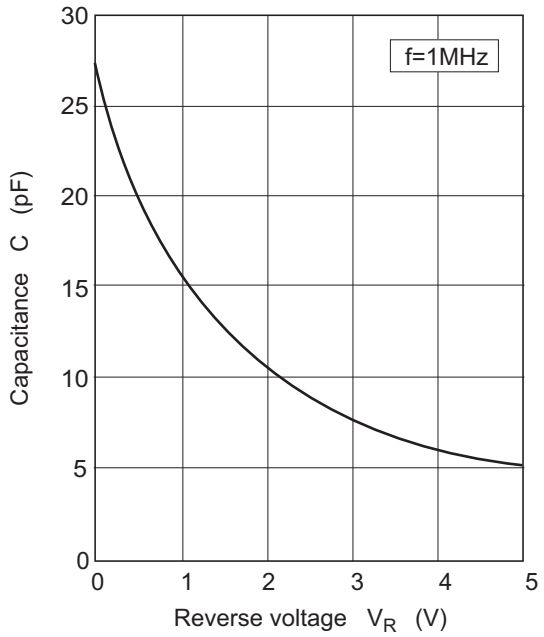


Fig.2 Capacitance vs. Reverse voltage

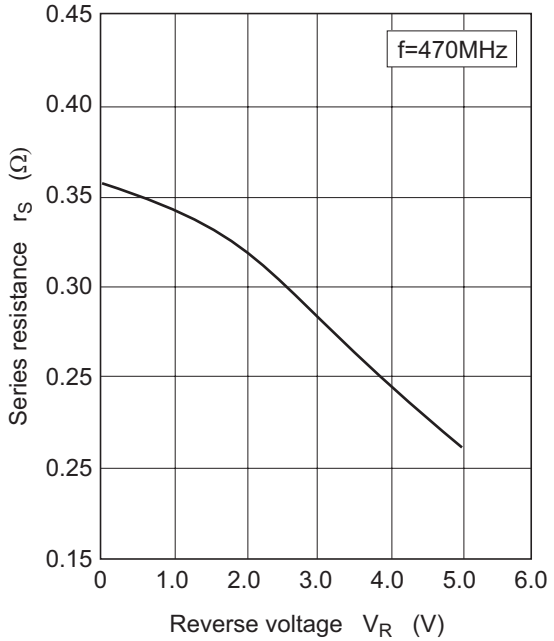


Fig.3 Series resistance vs. Reverse voltage

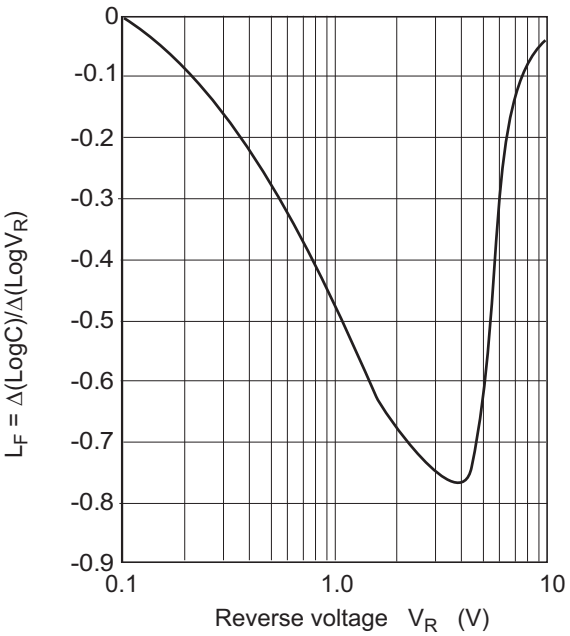
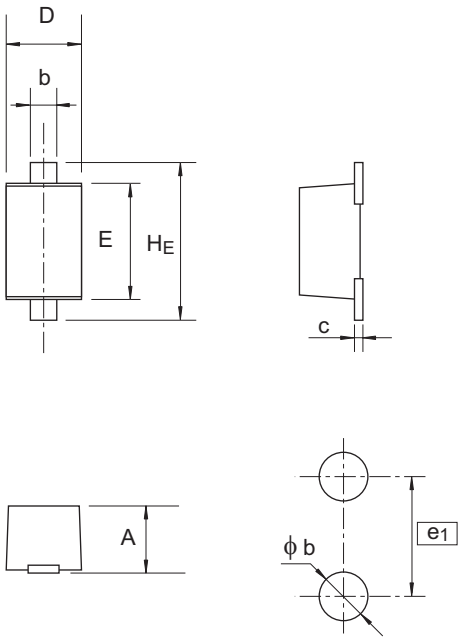


Fig.4 Linearity factor vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SFP	—	PUSF0002ZB-A	SFP / SFPV	0.0010g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕ b	—	0.50	—
e1	—	1.40	—

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Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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