



H7N1004DL, H7N1004DS

Silicon N-Channel MOSFET
High-Speed Power Switching

REJ03G1482-0100

Rev.1.00

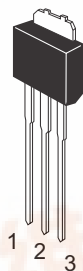
Nov 07, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 25 \text{ m}\Omega$ typ.
- Low drive current
- Available for 4.5 V gate drive

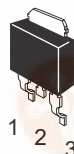
Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK(L)-2)

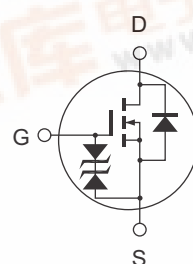


H7N0607DL

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK-(S))



H7N0607DS



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	25	A
Drain peak current	I_D (pulse) ^{Note 1}	75	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} ^{Note 3}	15	A
Avalanche energy	E_{AR} ^{Note 3}	22.5	mJ
Channel dissipation	P_{ch} ^{Note 2}	30	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. Value at $T_c = 25^\circ C$ 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

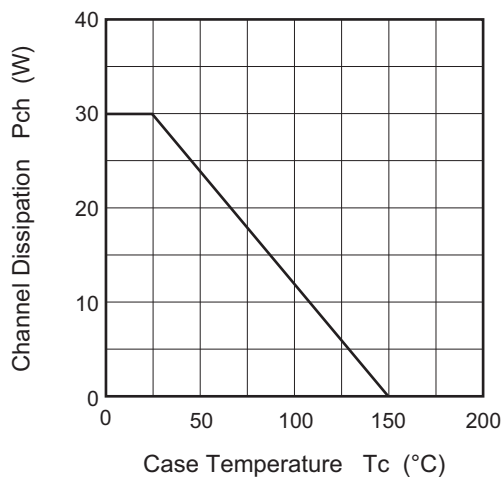
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Static drain to source on state resistance	$R_{DS(on)}$	—	25	35	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
		—	30	45	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	20	35	—	S	$I_D = 12.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	2800	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	240	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	140	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	50	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	Q_{gs}	—	9	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	11	—	nC	$I_D = 25 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 12.5 \text{ A}$
Rise time	t_r	—	110	—	ns	$R_L = 2.4 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	t_f	—	9.5	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.89	—	V	$I_F = 25 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = 25 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

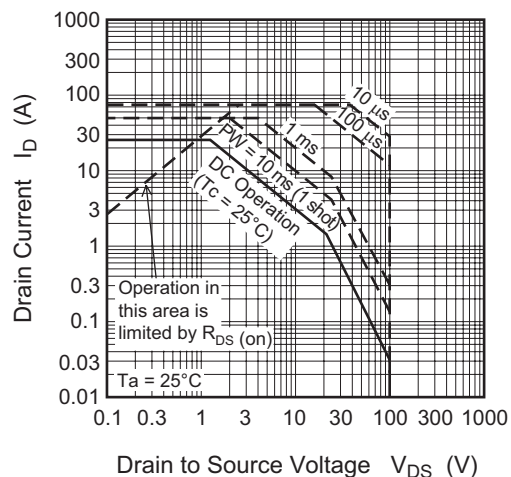
Notes: 4. Pulse test

Main Characteristics

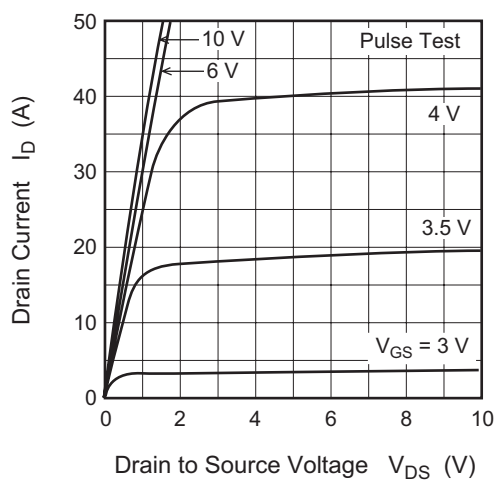
Power vs. Temperature Derating



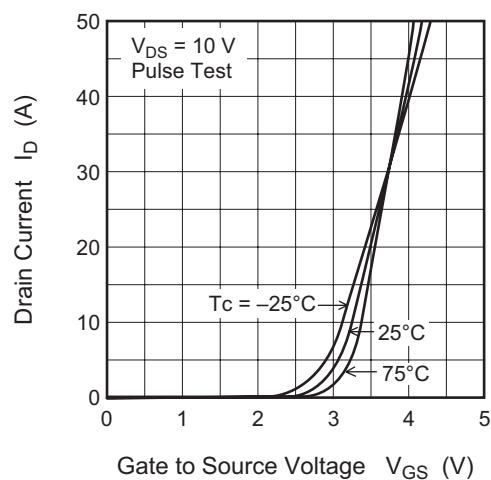
Maximum Safe Operation Area



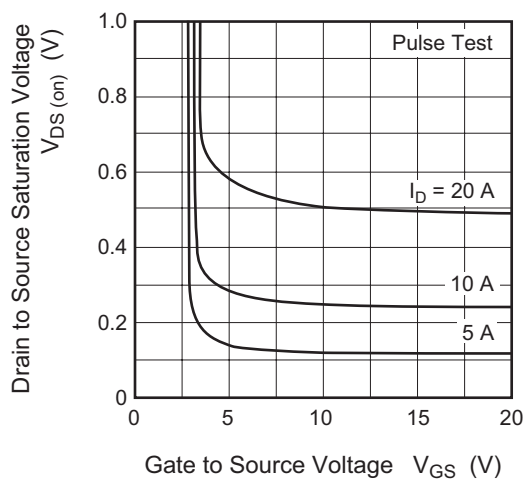
Typical Output Characteristics



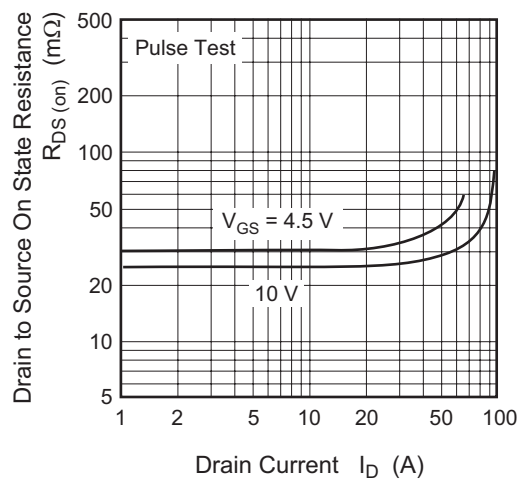
Typical Transfer Characteristics

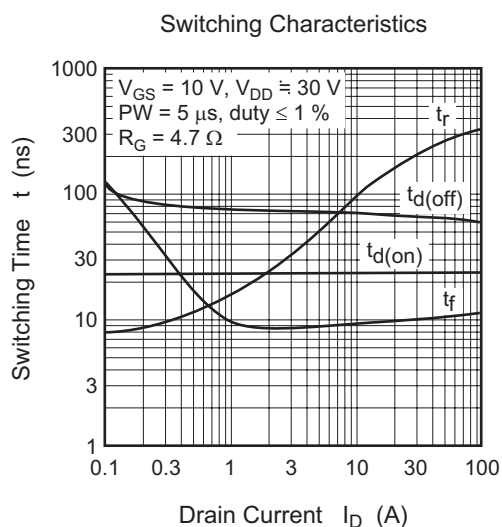
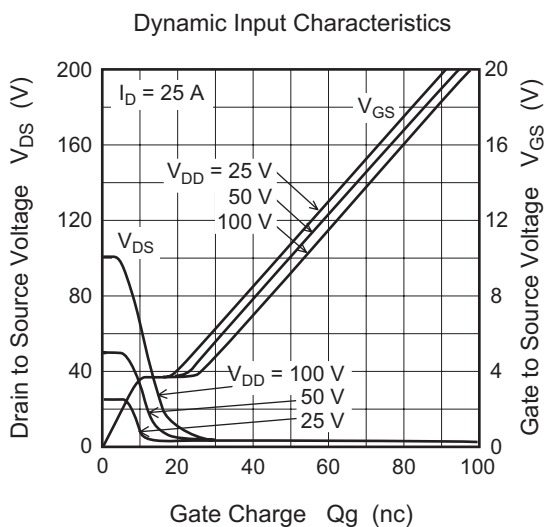
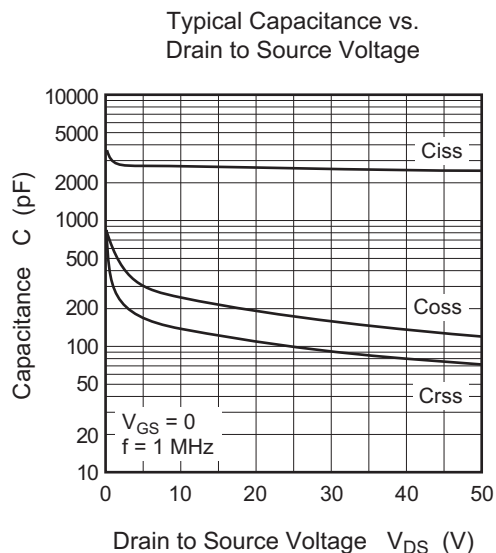
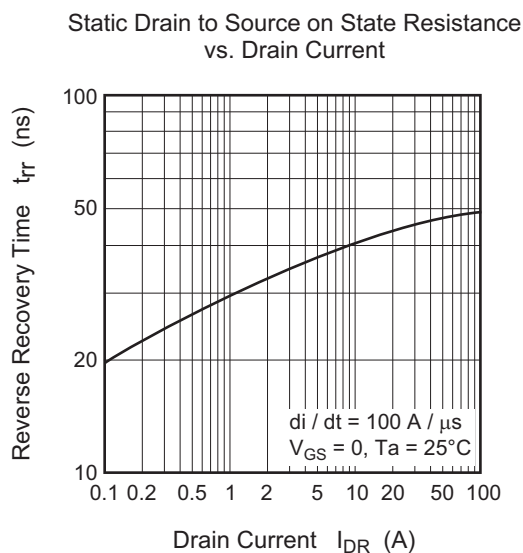
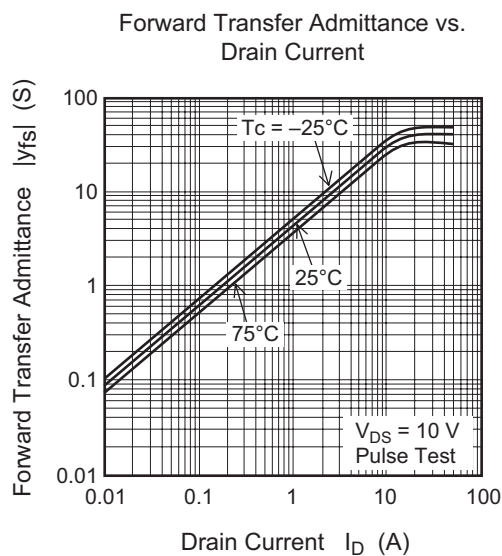
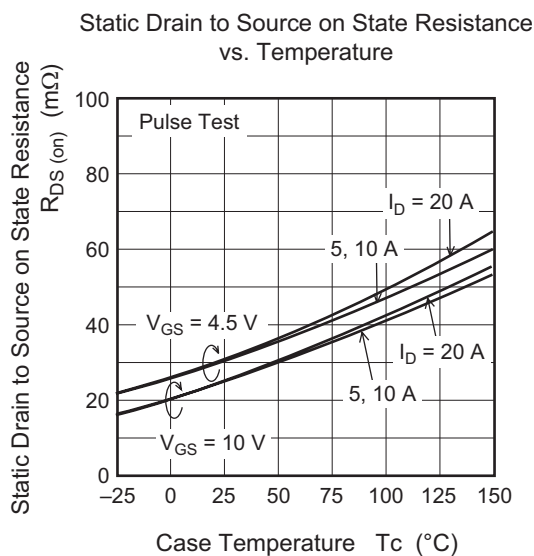


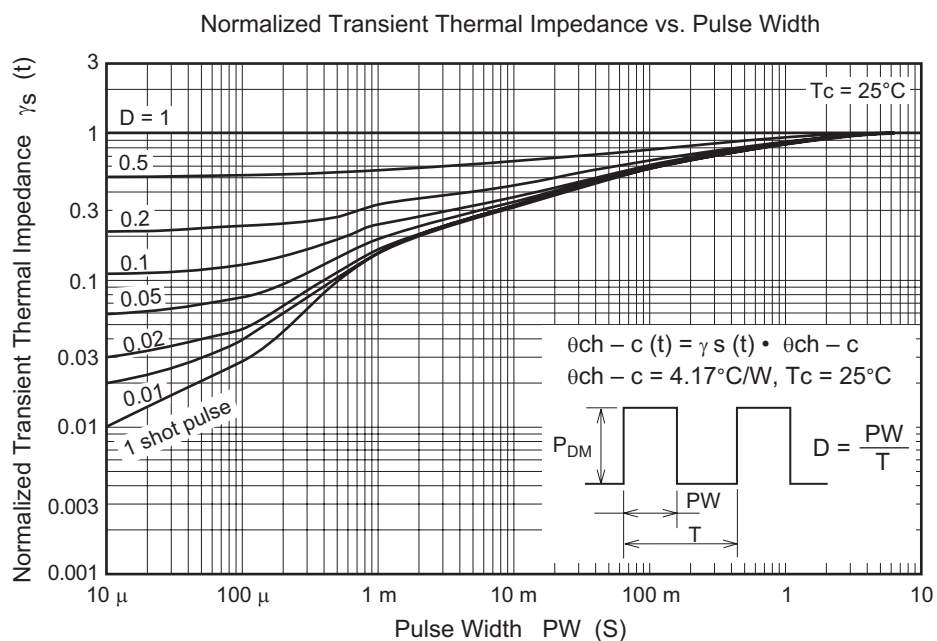
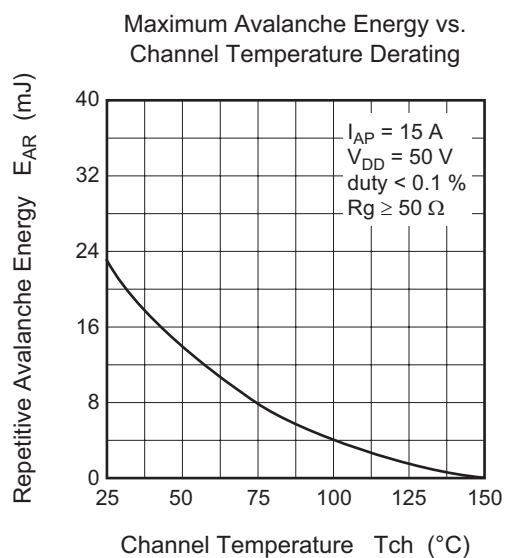
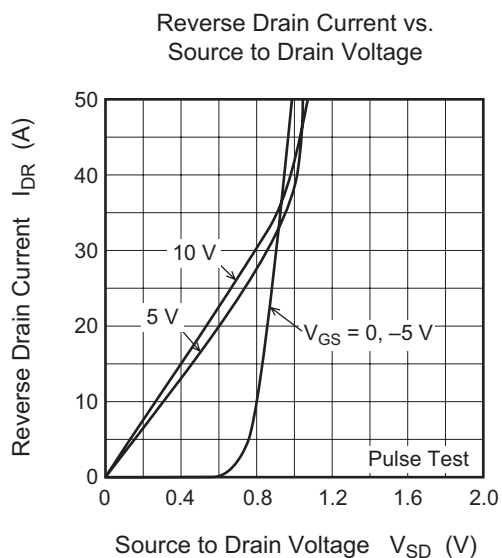
Drain to Source Saturation Voltage vs. Gate to Source Voltage



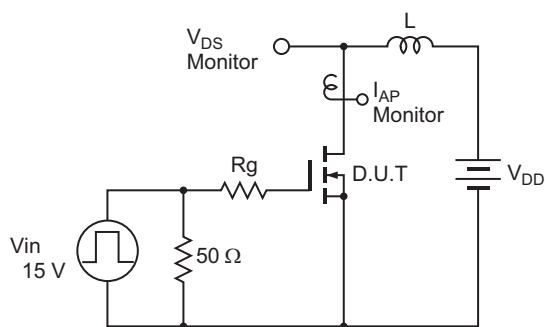
Static Drain to Source on State Resistance vs. Drain Current





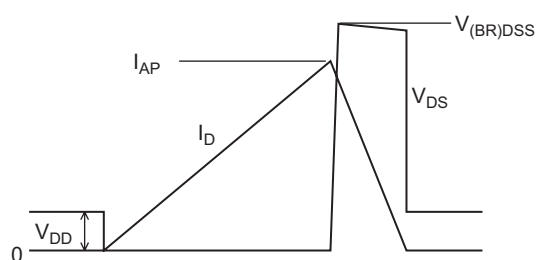


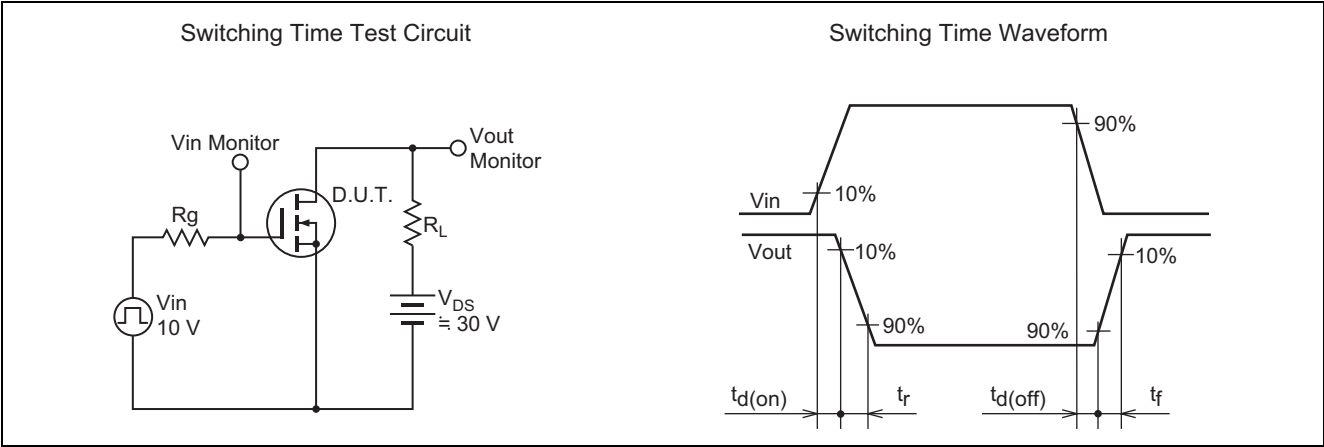
Avalanche Test Circuit



Avalanche Waveform

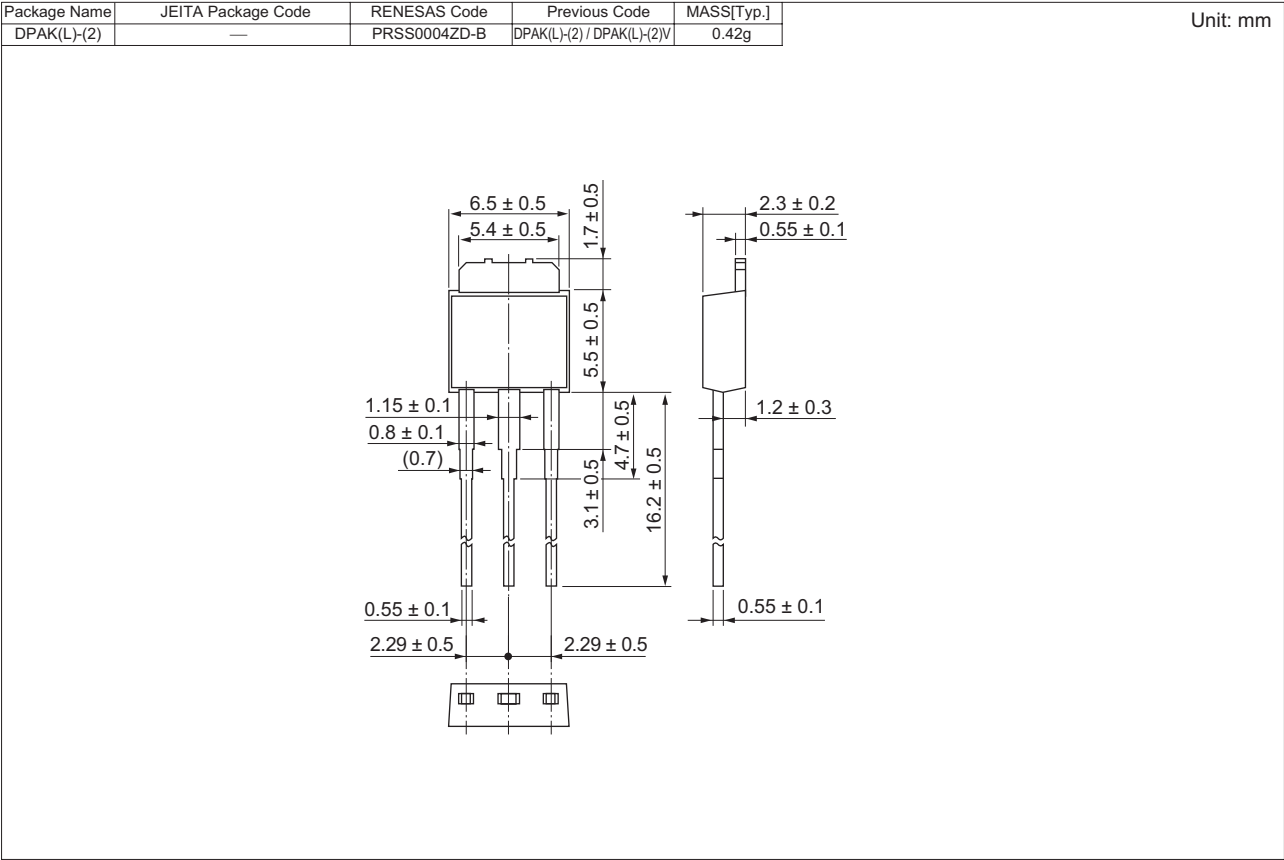
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



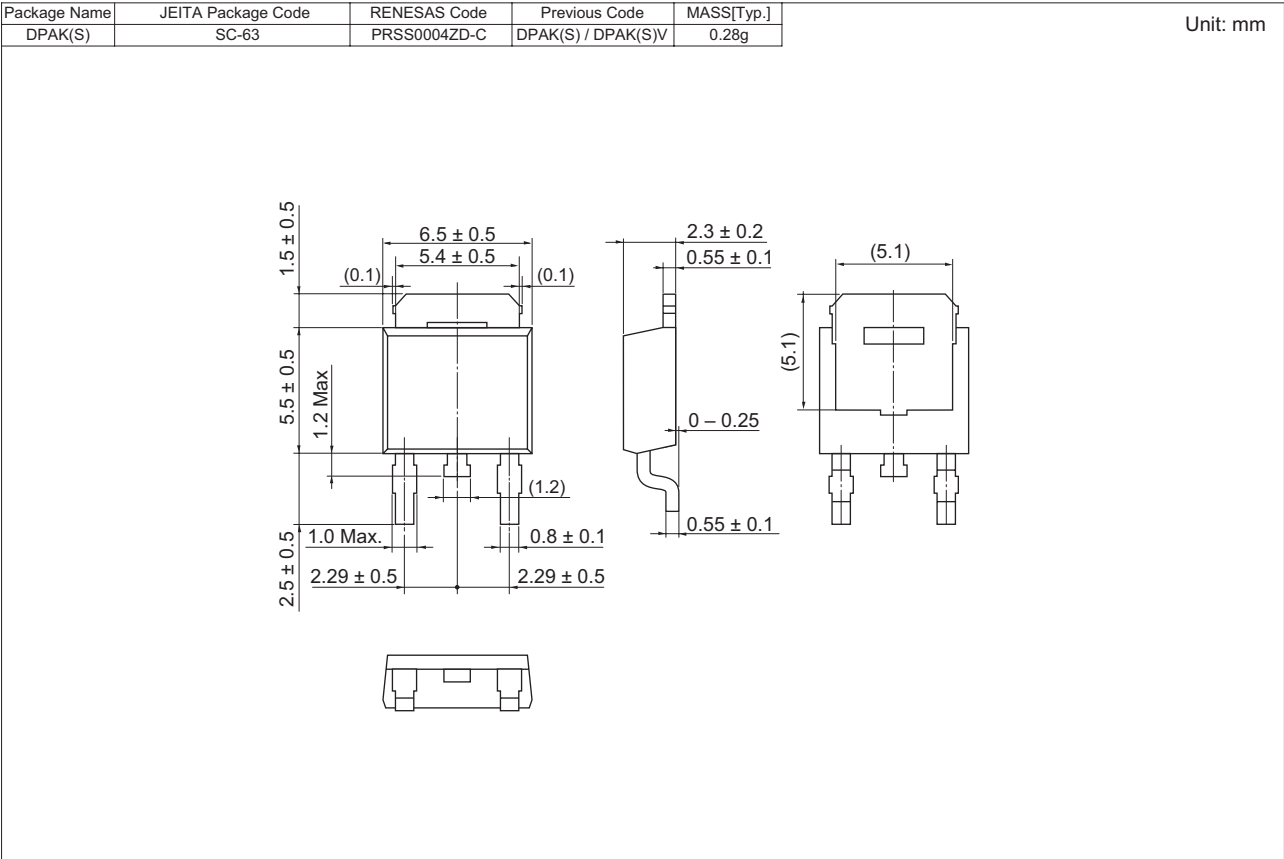


Package Dimensions

• H7N1004DL



• H7N1004DS



Ordering Information

Part Name	Quantity	Shipping Container
H7N1004DL	100 pcs	Sack
H7N1004DSTL	3000 pcs	Taping
H7N1004DL-E	100 pcs	Sack
H7N1004DSTL-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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