



Integrated
Circuit
Systems, Inc.

ICS8304

LOW SKEW, 1-TO-4 LVCMOS / LVTTTL FANOUT BUFFER

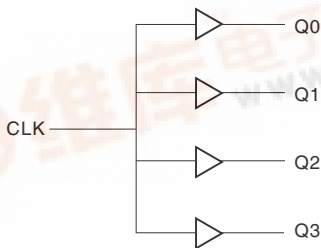
GENERAL DESCRIPTION

The ICS8304 is a low skew, 1-to-4 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8304 is characterized at full 3.3V for input V_{DD} , and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8304 ideal for those clock distribution applications demanding well defined performance and repeatability.

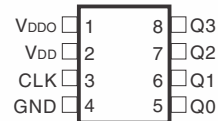
FEATURES

- 4 LVCMOS / LVTTTL outputs
- LVCMOS / LVTTTL clock input
- Maximum output frequency: 200MHz
- Output skew: 45ps (maximum at 3.3V supply)
- Part-to-part skew: 500ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- Lead-Free package available
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8304
8-Lead SOIC, 150mil
3.9mm x 4.9mm, x 1.63mm package body
M Package
Top View



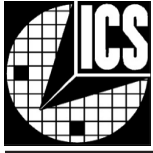


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{DDO}	Power		Output supply pin.
2	V _{DD}	Power		Core supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTTL clock input.
4	GND	Power		Power supply ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD} , V _{DDO} = 3.465V			15	pF
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ
R _{OUT}	Output Impedance		5	7	12	Ω



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.6			V
		$I_{OH} = -16mA$	2.9			V
		$I_{OH} = -100\mu A$	3			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V
		$I_{OL} = 16mA$			0.25	V
		$I_{OL} = 100\mu A$			0.15	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Section, "3.3V Output Load Test Circuit".

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA



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TABLE 3D. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		2.1			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Section, "3.3V/2.5V Output Load Test Circuit".

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq 166MHz$	2.0		3.3	ns
		$166MHz < f \leq 189.5MHz$	2.0		3.4	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	$f = 133MHz$			45	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	$f \leq 189.5MHz$	40		60	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				189.5	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq 166MHz$	2.3		3.7	ns
		$166MHz < f \leq 189.5MHz$	2.15		3.55	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	$f = 133MHz$			60	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	$f \leq 189.5MHz$	40		60	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

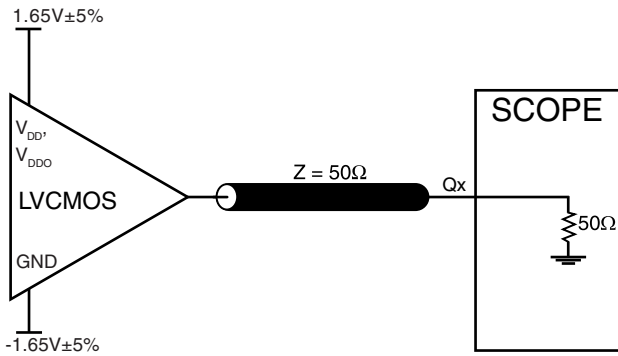
Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

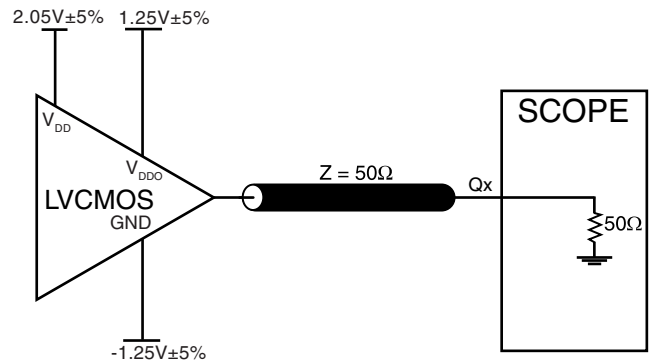
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



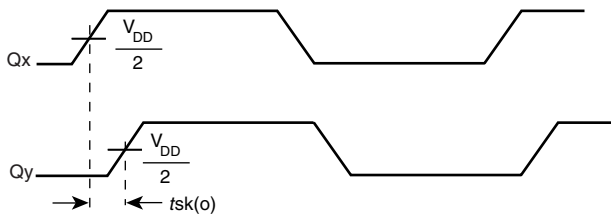
PARAMETER MEASUREMENT INFORMATION



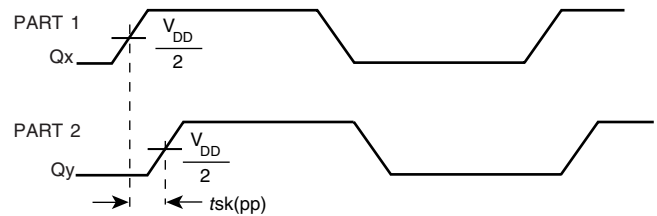
3.3V OUTPUT LOAD AC TEST CIRCUIT



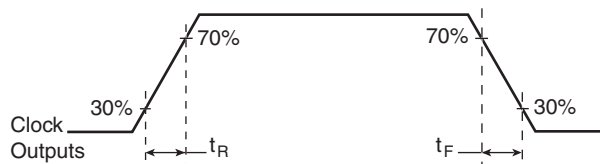
2.5V OUTPUT LOAD AC TEST CIRCUIT



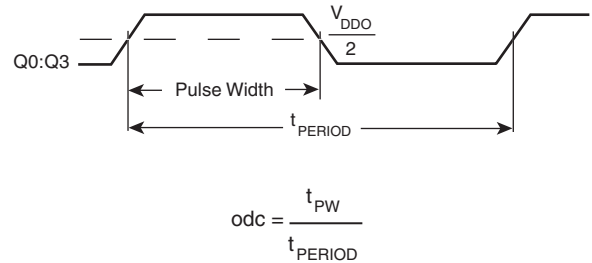
OUTPUT SKEW



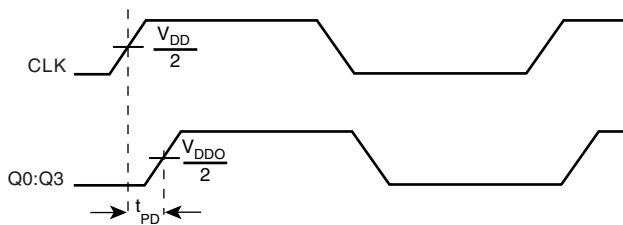
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY



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RELIABILITY INFORMATION

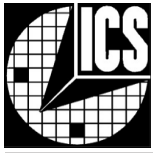
TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8304 is: 416



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PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

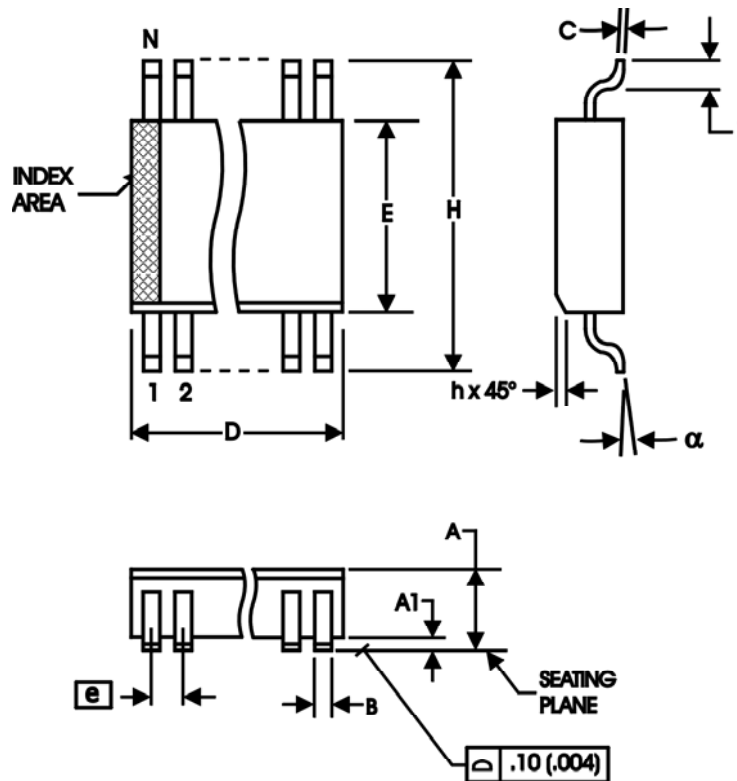
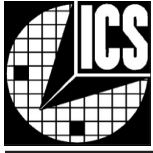


TABLE 6. PACKAGE DIMENSIONS - SUFFIX M

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012



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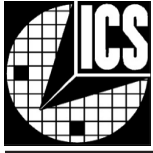
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TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8304AM	8304AM	8 lead SOIC	96 per tube	0°C to 70°C
ICS8304AMT	8304AM	8 lead SOIC on Tape and Reel	2500	0°C to 70°C
ICS8304AMLN	8304AMLN	8 lead SOIC, "Lead Free/Annealed"	96 per tube	0°C to 70°C
ICS8304AMLNT	8304AMLN	8 lead SOIC, "Lead Free/Annealed" on Tape and Reel	2500	0°C to 70°C
ICS8304AMLF	8304AMLF	8 lead SOIC, "Lead Free"	96 per tube	0°C to 70°C
ICS8304AMLFT	8304AMLF	8 lead SOIC, "Lead Free" on Tape and Reel	2500	0°C to 70°C

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T4A	3	<ul style="list-style-type: none"> Revised $t_{p_{LH}}$ (Propagation Delay) row from 2.3 Min. to 2 Min. Deleted $t_{p_{HL}}$ row. Revised $tsk(o)$ (Output Skew) row from 35 Max. to 80 Max. Revised $tsk(pp)$ (Part-to-Part Skew) row from 200 Max. to 500 Max. General note changed from "...measured at 166MHz..." to "...measured at 150MHz..." 	12/4/01
	T4B	4	<ul style="list-style-type: none"> Revised $t_{p_{LH}}$ (Propagation Delay) row from 2.6 Min. to 2.3 Min. Deleted $t_{p_{HL}}$ row. Revised $tsk(o)$ (Output Skew) row from 35 Max. to 85 Max. Revised $tsk(pp)$ (Part-to-Part Skew) row from 200 Max. to 500 Max. General note changed from "...measured at 166MHz..." to "...measured at 150MHz..." 	
C	T4A	3	<ul style="list-style-type: none"> In AC table, revised $tsk(o)$ row from 80ps Max. to 45ps Max. Added $f = 133\text{MHz}$ in Test Conditions column. In odc row, deleted test conditions. In notes, changed 150MHz to f_{MAX}. 	12/11/01
	T4B	4	<ul style="list-style-type: none"> In AC table, revised $tsk(o)$ row from 80ps Max. to 60ps Max. Added $f = 133\text{MHz}$ in Test Conditions column. In odc row, deleted test conditions In notes, changed 150MHz to f_{MAX}. 	
C	T7	10	In the Ordering Information table, Marking column, revised marking to read 8304AM from ICS8304AM.	3/11/02
D	T3B	3	LVCMOS/LVTTTL DC Characteristics Table, added I_{OH} and I_{OL} Test Conditions to V_{OH} and V_{OL} rows.	4/4/02
E	T1	1	Pin Assignment - adjusted dimensions.	4/13/04
	T2	2	Pin Descriptions - changed V_{DD} description to Core supply pin.	
	T3A & T3C	2	Pin Characteristics - changed C_{IN} max 4pF to typical 4pF. Deleted R_{PULLUP} row.	
		3 & 4	Added 5Ω min. and 12Ω max. to R_{OUT} .	
T7	8	Power Supply tables - changed V_{DD} parameter from Power to Core. Ordering Information table - added "Lead Free/Annealed" marking. Updated format throughout the data sheet.		
F	T4A	1	Features section, changed Maximum output frequency bullet from 166MHz to 200MHz.	6/1/04
	T4B	4	3.3V AC Table - changed 166MHz max. to 200MHz max. Added another line for Propagation Delay. Changed test conditions in Output Duty Cycle from 166MHz to 189.5MHz.	
		4	3.3V AC Table - changed 166MHz max. to 189.5MHz max. Added another line for Propagation Delay. Changed test conditions in Output Duty Cycle from 166MHz to 189.5MH	
F	T7	8	Ordering Information table - added "Lead Free" marking.	9/13/04