SONY

ICX405AL

Diagonal 6mm (Type 1/3) CCD Image Sensor for CCIR B/W Video Cameras

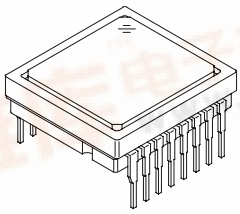
Description

The ICX405AL is an interline CCD solid-state image sensor suitable for CCIR B/W video cameras with a diagonal 6mm (Type 1/3) system. Compared with the conventional product ICX055BL, basic characteristics such as sensitivity, smear, dynamic range and S/N are improved drastically.

This chip features a field period readout system and an electronic shutter with variable charge-storage time.

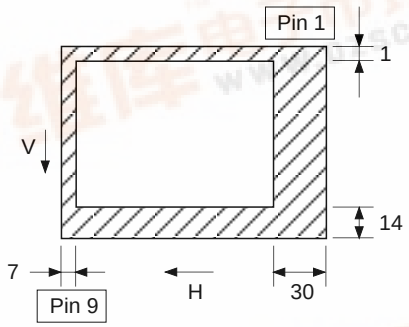
This chip is suitable for applications such as surveillance cameras, automotive cameras, etc.

16 pin DIP (Plastic)



Features

- High sensitivity (+4dB compared with the ICX055BL)
- Low smear (–20dB compared with the ICX055BL)
- High D range (+3dB compared with the ICX055BL)
- High S/N
- Low dark current
- Excellent antiblooming characteristics
- Continuous variable-speed shutter
- No voltage adjustment
  (Reset gate and substrate bias are not adjusted.)
- Reset gate: 5V drive
- Horizontal register: 5V drive



Optical black position
(Top View)

Device Structure

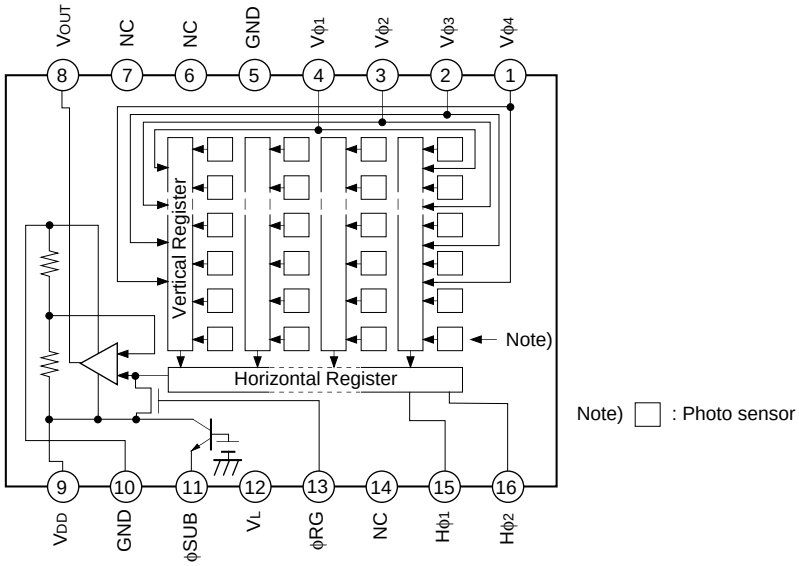
- Interline CCD image sensor
- Image size: Diagonal 6mm (Type 1/3)
- Number of effective pixels: 500 (H) × 582 (V) approx. 290K pixels
- Total number of pixels: 537 (H) × 597 (V) approx. 320K pixels
- Chip size: 5.59mm (H) × 4.68mm (V)
- Unit cell size: 9.8µm (H) × 6.3µm (V)
- Optical black: Horizontal (H) direction : Front 7 pixels, rear 30 pixels
  Vertical (V) direction : Front 14 pixels, rear 1 pixel
- Number of dummy bits: Horizontal 16
  Vertical 1 (even fields only)
- Substrate material: Silicon

Super HAD CCD™

*Super HAD CCD is a trademark of Sony Corporation. The Super HAD CCD is a version of Sony's high performance CCD HAD (Hole-Accumulation Diode) sensor with sharply improved sensitivity by the incorporation of a new semiconductor technology developed by Sony Corporation.

E00608A14-PS

Block Diagram and Pin Configuration
(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	9	V_{DD}	Supply voltage
2	$V\phi_3$	Vertical register transfer clock	10	GND	GND
3	$V\phi_2$	Vertical register transfer clock	11	φSUB	Substrate clock
4	$V\phi_1$	Vertical register transfer clock	12	V_L	Protective transistor bias
5	GND	GND	13	φRG	Reset gate clock
6	NC		14	NC	
7	NC		15	$H\phi_1$	Horizontal register transfer clock
8	V_{OUT}	Signal output	16	$H\phi_2$	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +8	V	
	$V\phi_1$, $V\phi_3$ – φSUB	–50 to +15	V	
	$V\phi_2$, $V\phi_4$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – φSUB	–40 to +0.3	V	
Against GND	V_{DD}, V_{OUT}, φRG – GND	–0.3 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +6	V	
Against V_L	$V\phi_1$, $V\phi_3$ – V_L	–0.3 to +28	V	
	$V\phi_2$, $V\phi_4$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–6 to +6	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_4$	–14 to +14	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock pin, because a DC bias is generated within the CCD.

DC Characteristics

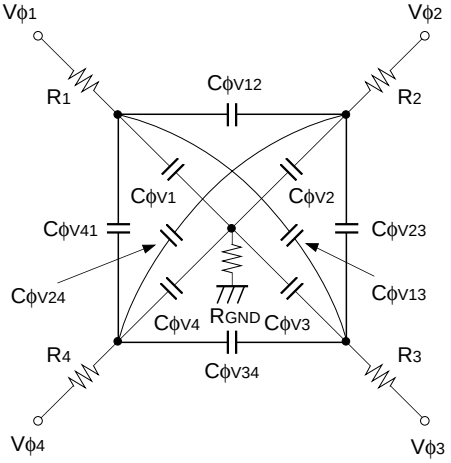
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		3	5	mA	

Clock Voltage Conditions

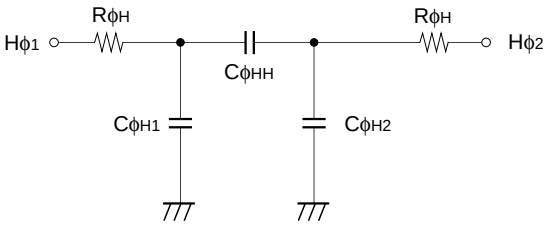
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.0	–7.0	–6.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi_V$	6.3	7.0	8.05	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.3	V	2	High-level coupling
	V_{VHL}			0.3	V	2	High-level coupling
	V_{VLH}			0.3	V	2	Low-level coupling
	V_{VLL}			0.3	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	Input through 0.1µF capacitance
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
	V_{RGH}	V_{DD} +0.3	V_{DD} +0.6	V_{DD} +0.9	V	4	
Substrate clock voltage	$V\phi_{SUB}$	21.0	22.0	23.5	V	5	

Clock Equivalent Circuit Constant

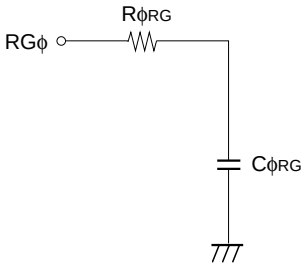
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$, $C\phi V3$		1500		pF	
	$C\phi V2$, $C\phi V4$		1000		pF	
Capacitance between vertical transfer clocks	$C\phi V12$, $C\phi V34$		820		pF	
	$C\phi V23$, $C\phi V41$		330		pF	
	$C\phi V13$		100		pF	
	$C\phi V24$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$, $C\phi H2$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		22		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		5		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		270		pF	
Vertical transfer clock series resistor	$R1$, $R3$		100		Ω	
	$R2$, $R4$		150		Ω	
Vertical transfer clock ground resistor	R_{GND}		68		Ω	
Horizontal transfer clock series resistor	$R\phi H$		10		Ω	
Reset gate clock series resistor	$R\phi RG$		50		Ω	



Vertical transfer clock equivalent circuit



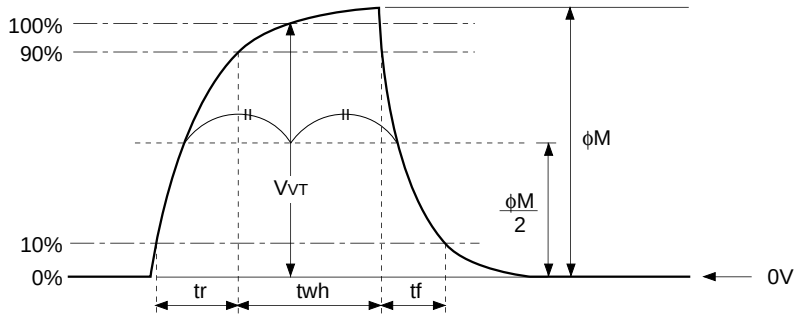
Horizontal transfer clock equivalent circuit



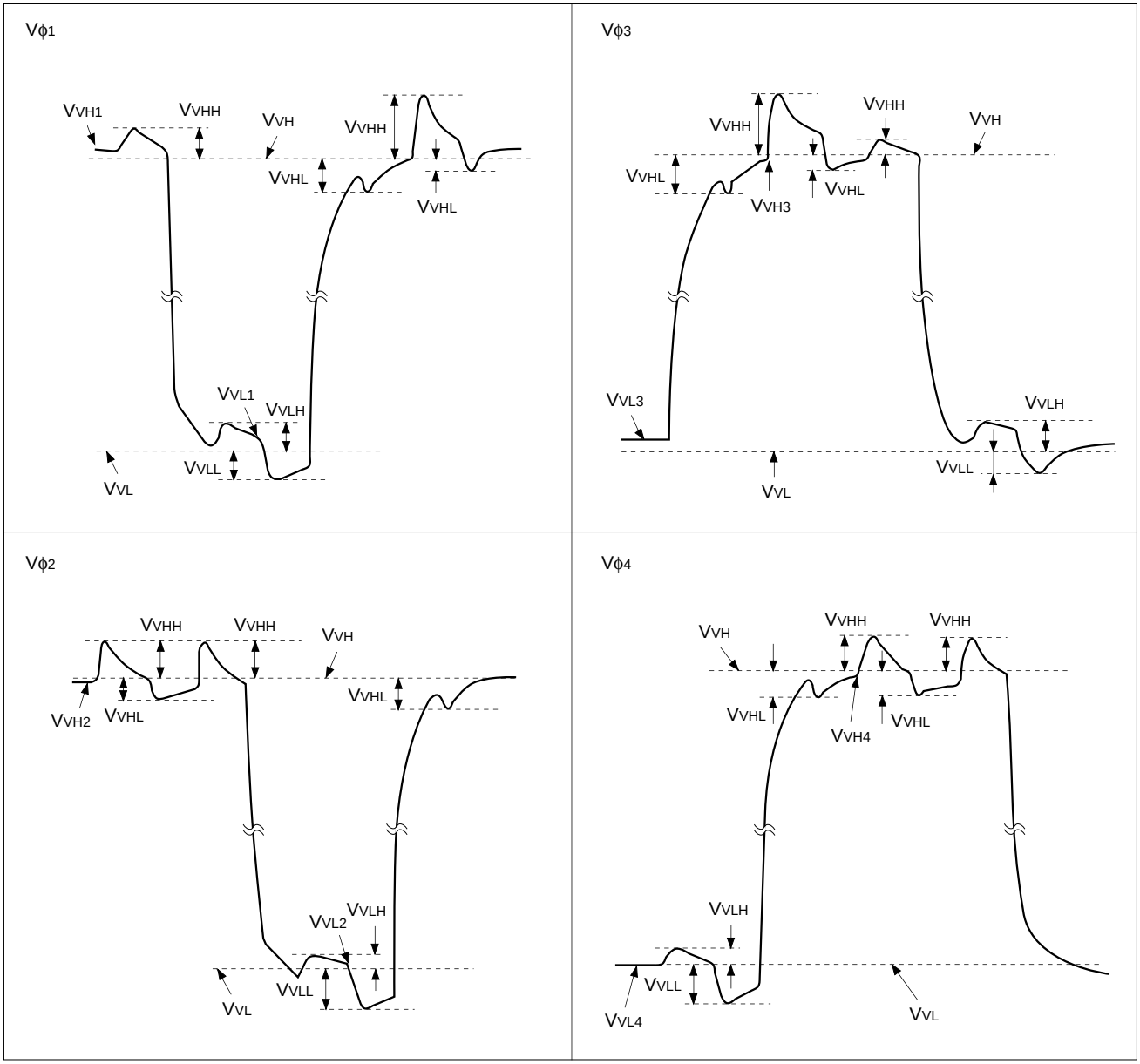
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

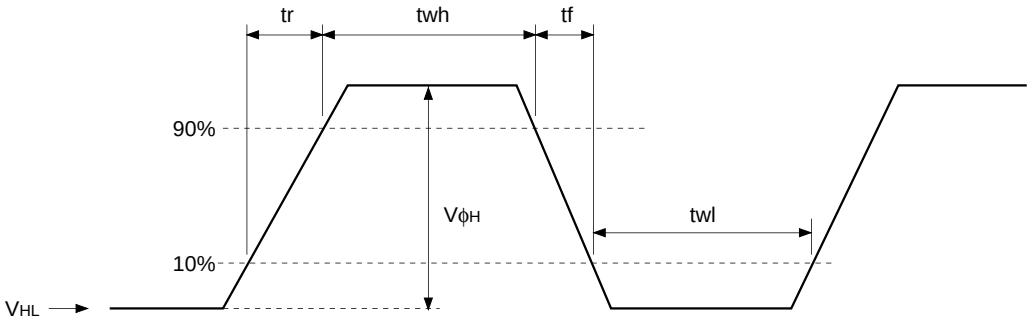


$V_{VH} = (V_{VH1} + V_{VH2})/2$

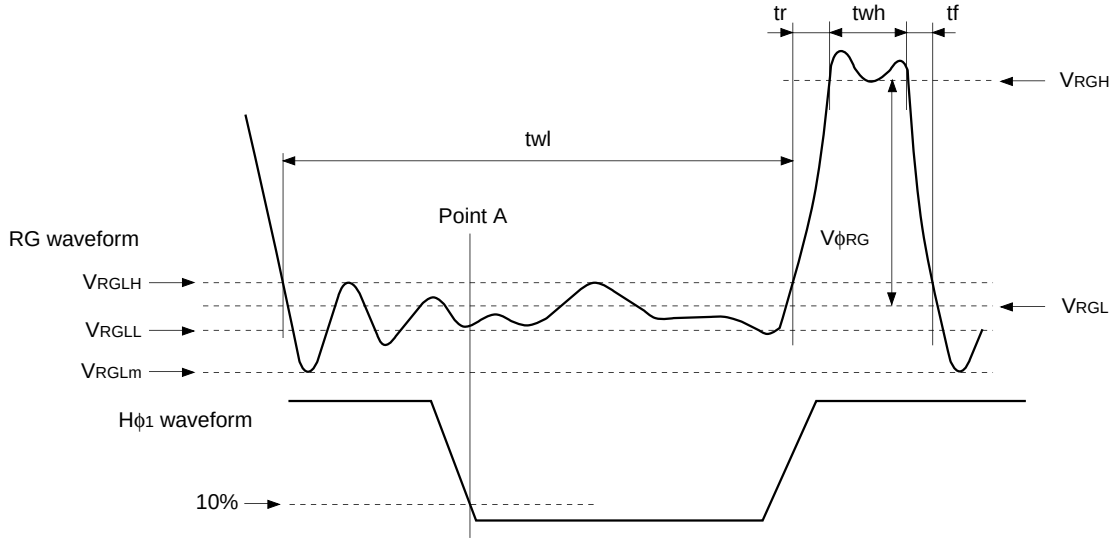
$V_{VL} = (V_{VL3} + V_{VL4})/2$

$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, VRGL is the average value of VRGLH and VRGLL.

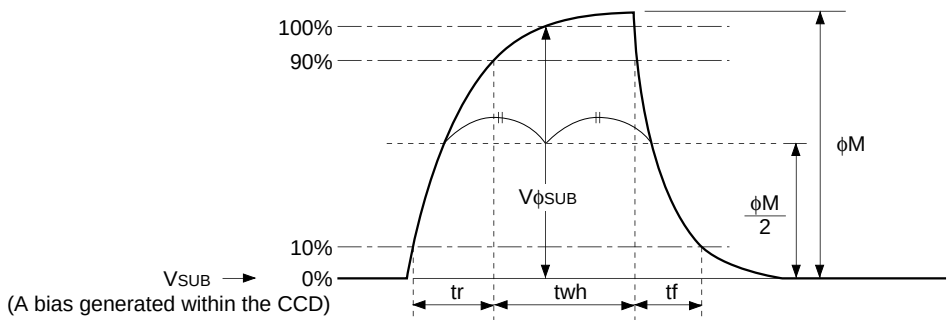
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	*1
Horizontal transfer clock	During imaging	$H\phi$	37	41		38	42			12	15		10	15	ns	*2
Horizontal transfer clock	During parallel-serial conversion	$H\phi_1$		5.6						0.012			0.012		µs	
Horizontal transfer clock	During parallel-serial conversion	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock		ϕRG	11	15		75	79			6.5			4.5		ns	
Substrate clock		ϕSUB	1.5	2.0							0.5			0.5	µs	During drain charge

*1 When vertical transfer clock driver CXD1267AN is used.

*2 $tf \geq tr - 2ns$.

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	1080	1350		mV	1	
Saturation signal	Vsat	1000			mV	2	Ta = 60°C
Smear	Sm		–115	–98	dB	3	
Video signal shading	SH			20	%	4	Zone 0 and I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Definition of Video Signal Shading

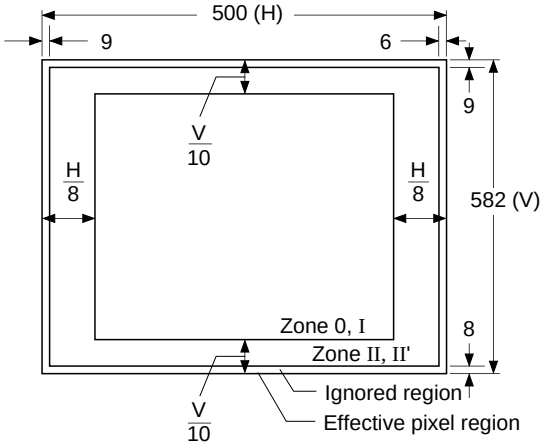


Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*A] in the drive circuit example is used.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute the value into the following formula.

$$S = Vs \times \frac{250}{50} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 200mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = 20 \times \log\left(\frac{YSm}{200} \times \frac{1}{500} \times \frac{1}{10}\right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

   $SH = (Vmax - Vmin)/200 \times 100$ [%]

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

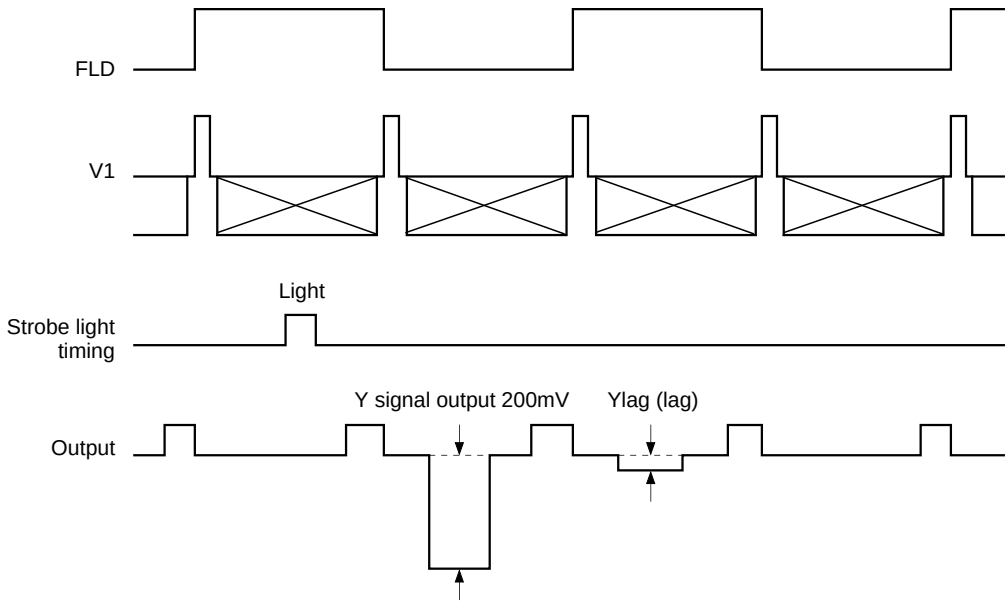
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Flicker
   Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the signal output is 200mV, and then measure the difference in the signal level between fields (ΔVf [mV]). Then substitute the value into the following formula.

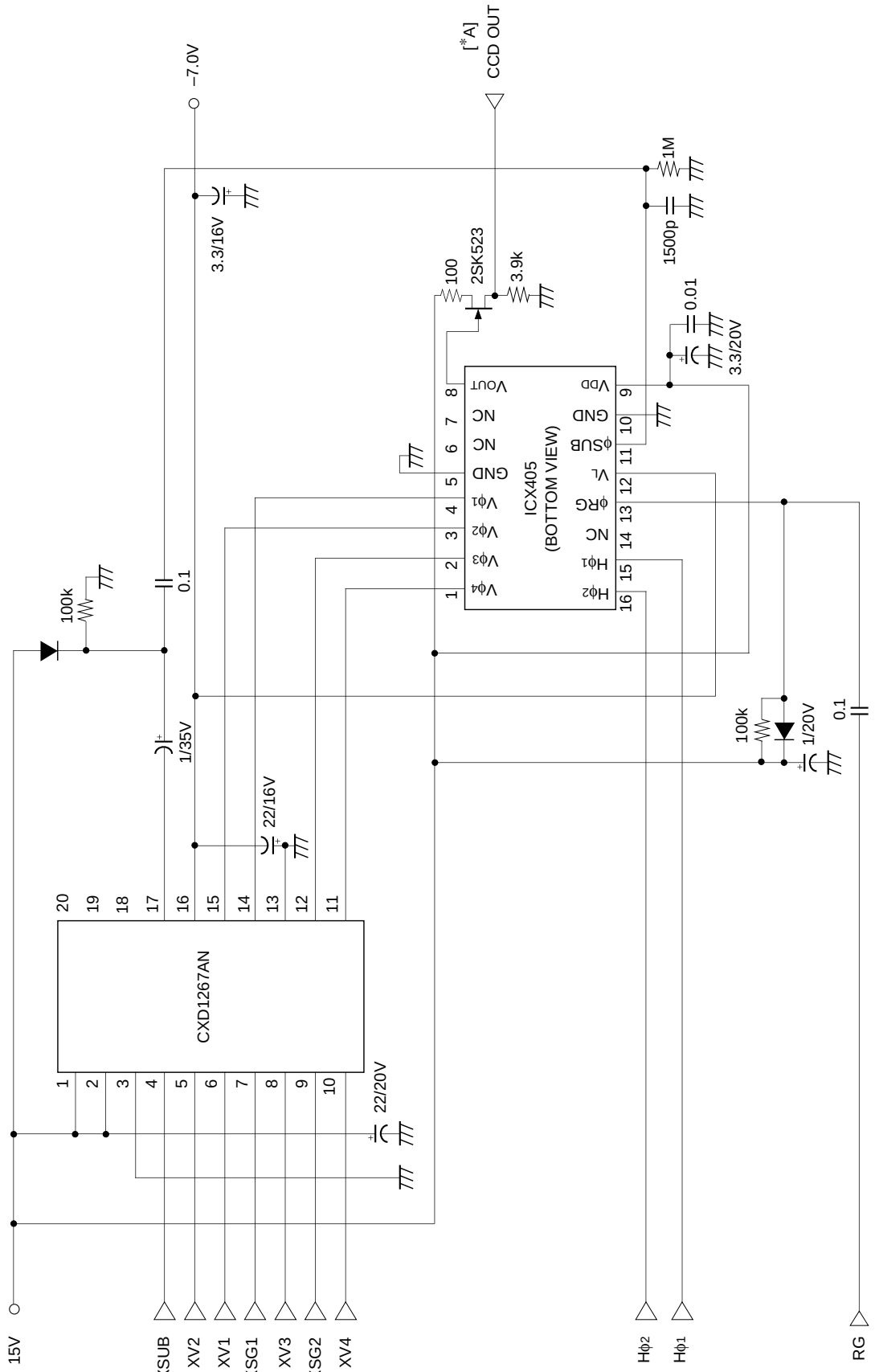
   $F = (\Delta Vf/200) \times 100$ [%]

8. Lag
   Adjust the signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/200) \times 100$ [%]

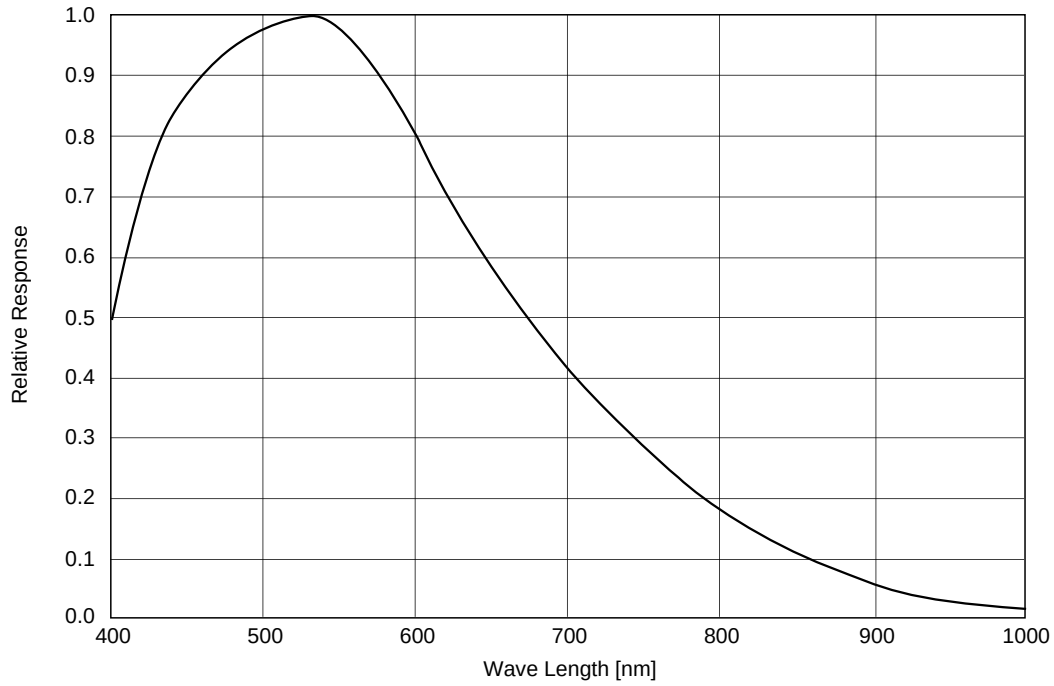


Drive Circuit

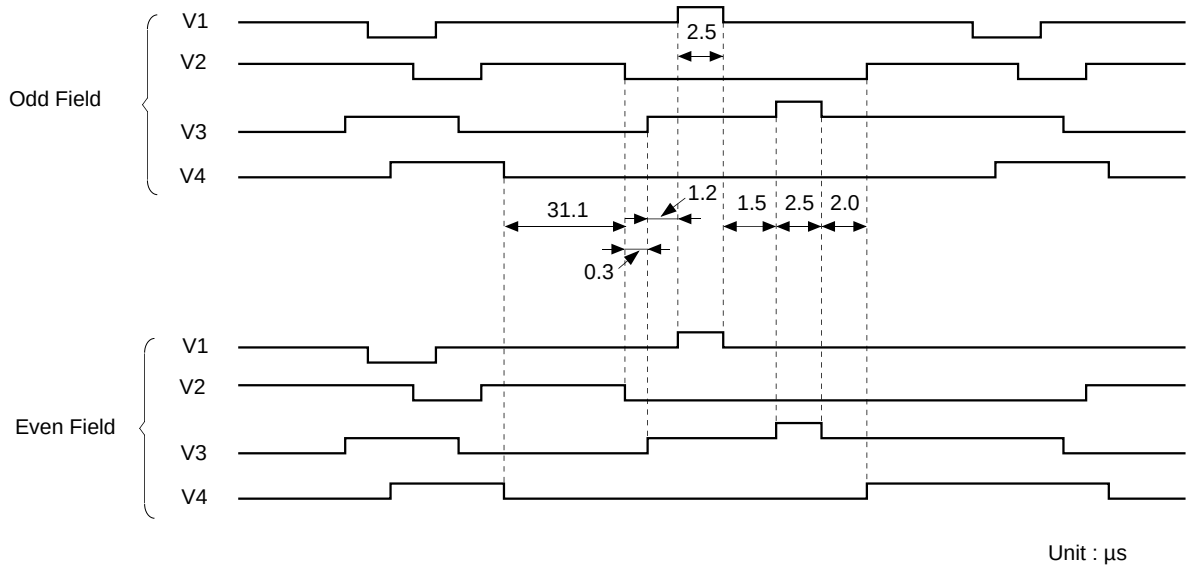


Spectral Sensitivity Characteristics

(excludes both lens characteristics and light source characteristics)

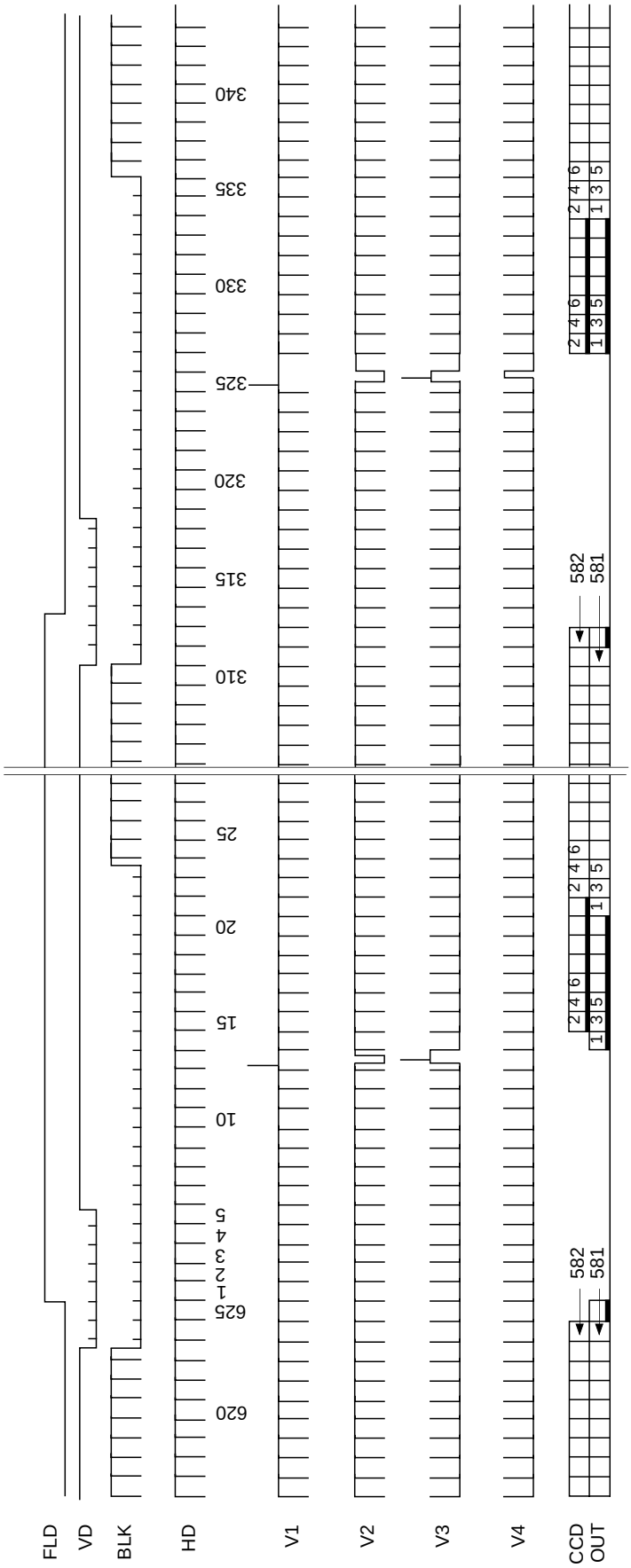


Sensor Readout Clock Timing Chart

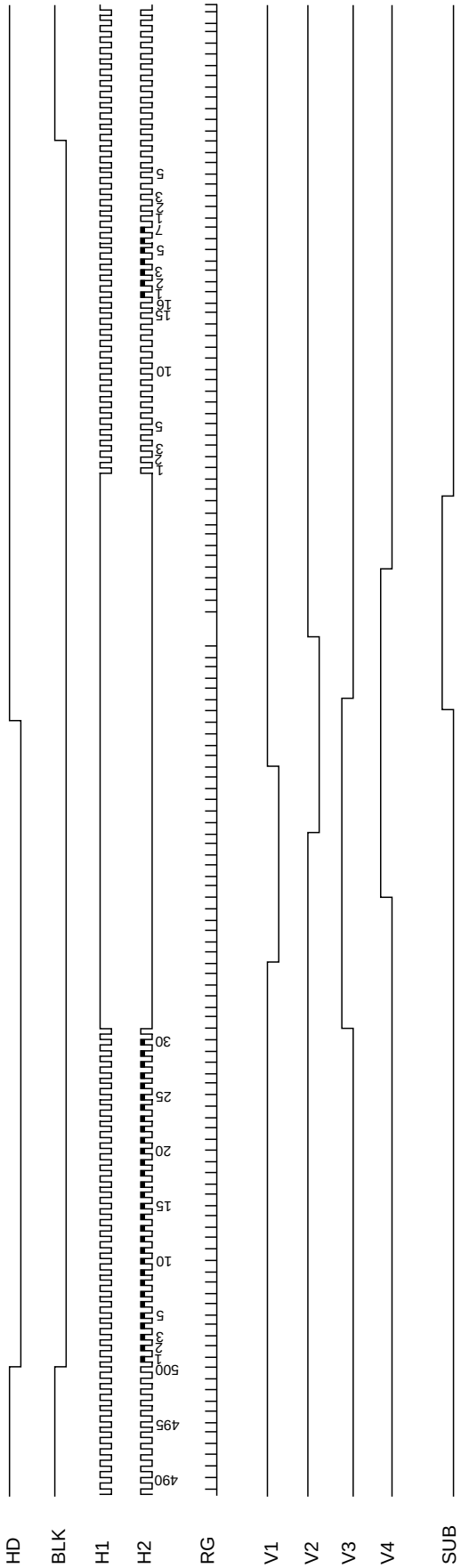


Unit : µs

Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

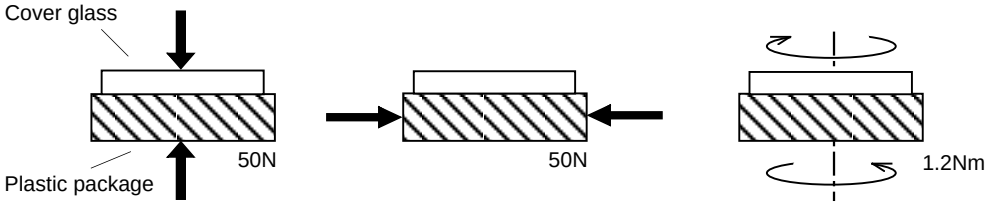
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



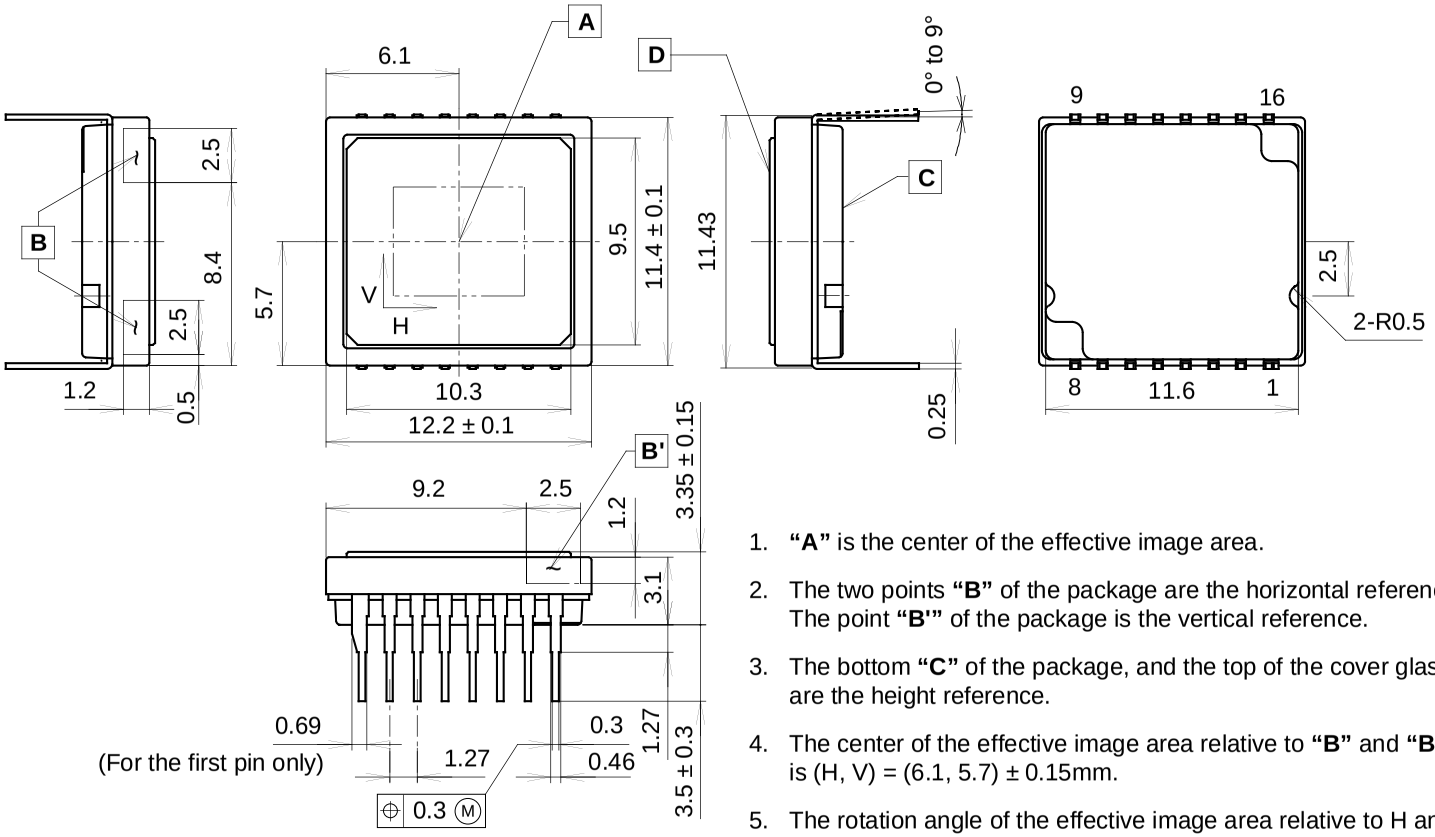
Compressive strength **Torsional strength**

b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

16pin DIP (450mil)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.90g
DRAWING NUMBER	AS-C2.2-01(E)

1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.