



QUICKSWITCH® PRODUCTS
2.5V / 3.3V 32-BIT HIGH
BANDWIDTH BUS SWITCH

IDTQS34XVH2245

FEATURES:

- N channel FET switches with no parasitic diode to Vcc
 - Isolation under power-off conditions
 - No DC path to Vcc or GND
 - 5V tolerant in OFF and ON state
- 5V tolerant I/Os
- Flat Ron characteristics over operating range
- Rail-to-rail switching 0 - 5V
- Bidirectional dataflow with near-zero delay: no added ground bounce
- Excellent Ron matching between channels
- Vcc operation: 2.3V to 3.6V
- High bandwidth
- LVTTTL-compatible control Inputs
- Undershoot Clamp Diodes on all switch and control Inputs
- Low I/O capacitance, 4pF typical
- 25Ω resistors for low noise and line matching
- Available in 80-pin QVSOP package

APPLICATIONS:

- Hot-swapping
- Low distortion analog switch
- Replaces mechanical relay
- ATM 25/155 switching

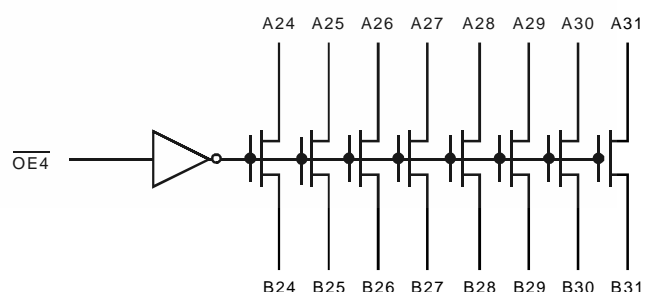
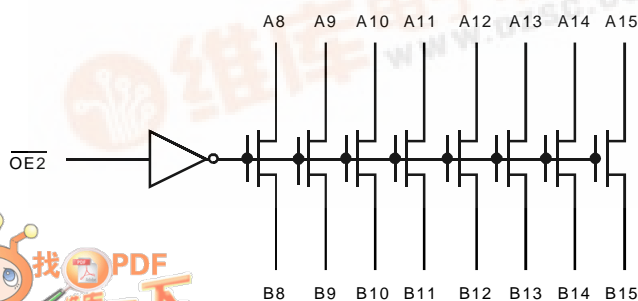
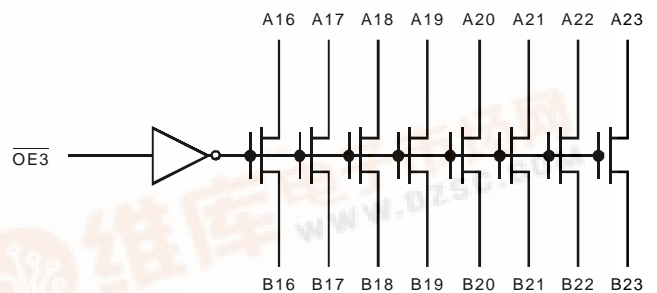
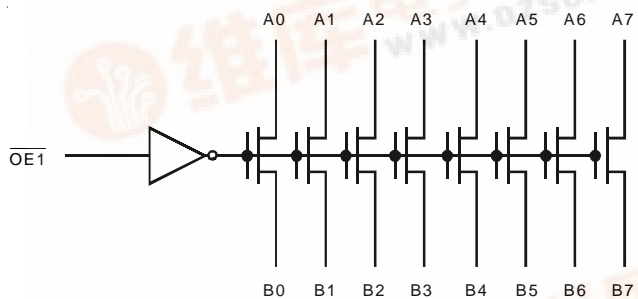
DESCRIPTION:

The QS34XVH2245 is a high bandwidth, 32-bit bus switch. The QS34XVH2245 with 25Ω resistance and 1.35ns propagation delay is ideal for line matching and low noise environments. The switches can be turned ON under the control of individual LVTTTL-compatible Output Enable (\overline{OE}) signals for bidirectional data flow with no added delay or ground bounce. In the ON state, the switches can pass signals up to 5V. In the OFF state, the switches offer very high impedance at the terminals.

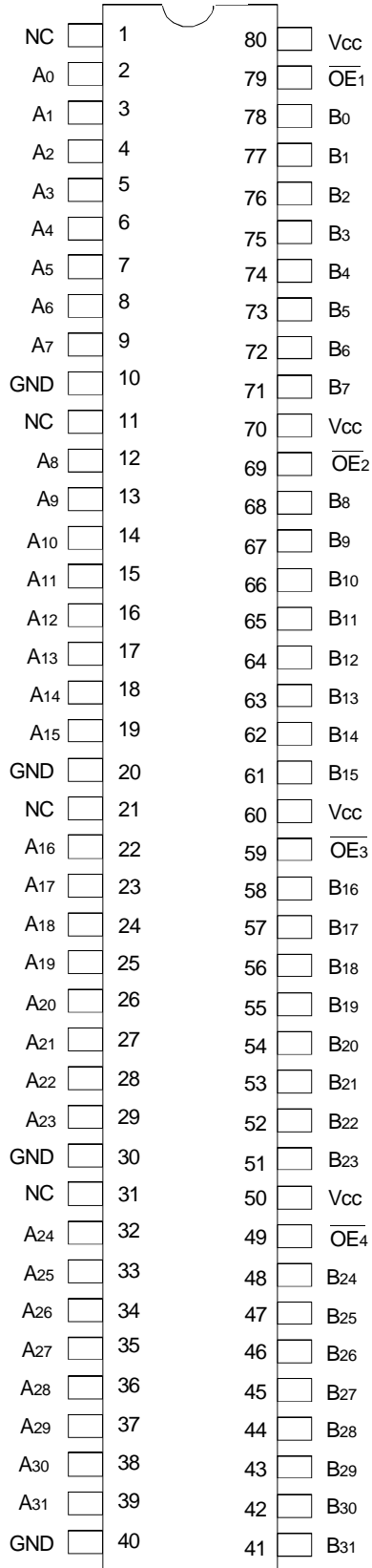
The combination of small propagation delay, high OFF impedance, and over-voltage tolerance makes the QS34XVH2245 ideal for high performance communications applications.

The QS34XVH2245 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|---|--------------|------|
| VTERM ⁽²⁾ | Supply Voltage to Ground | -0.5 to +4.6 | V |
| VTERM ⁽³⁾ | DC Switch Voltage V _s | -0.5 to +5.5 | V |
| VTERM ⁽³⁾ | DC Input Voltage V _{IN} | -0.5 to +5.5 | V |
| V _{AC} | AC Input Voltage (pulse width ≤20ns) | -3 | V |
| I _{OUT} | DC Output Current (max. sink current/pin) | 120 | mA |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

| Symbol | Parameter ⁽¹⁾ | Typ. | Max. | Unit |
|------------------|-----------------------------------|------|------|------|
| C _{IN} | Control Inputs | 3 | 5 | pF |
| C _{I/O} | Quickswitch Channels (Switch OFF) | 4 | 6 | pF |
| C _{I/O} | Quickswitch Channels (Switch ON) | 8 | 12 | pF |

NOTE:

- This parameter is guaranteed but not production tested.

PIN DESCRIPTION

| Pin Names | I/O | Description |
|------------------|-----|---------------|
| $\overline{OE}x$ | I | Output Enable |
| A _x | I/O | Bus A |
| B _x | I/O | Bus B |

FUNCTION TABLE⁽¹⁾

| $\overline{OE}x$ | Function |
|------------------|--|
| H | Disconnected |
| L | Connect (A _x = B _x) |

NOTE:

- H = HIGH Voltage Level
 L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

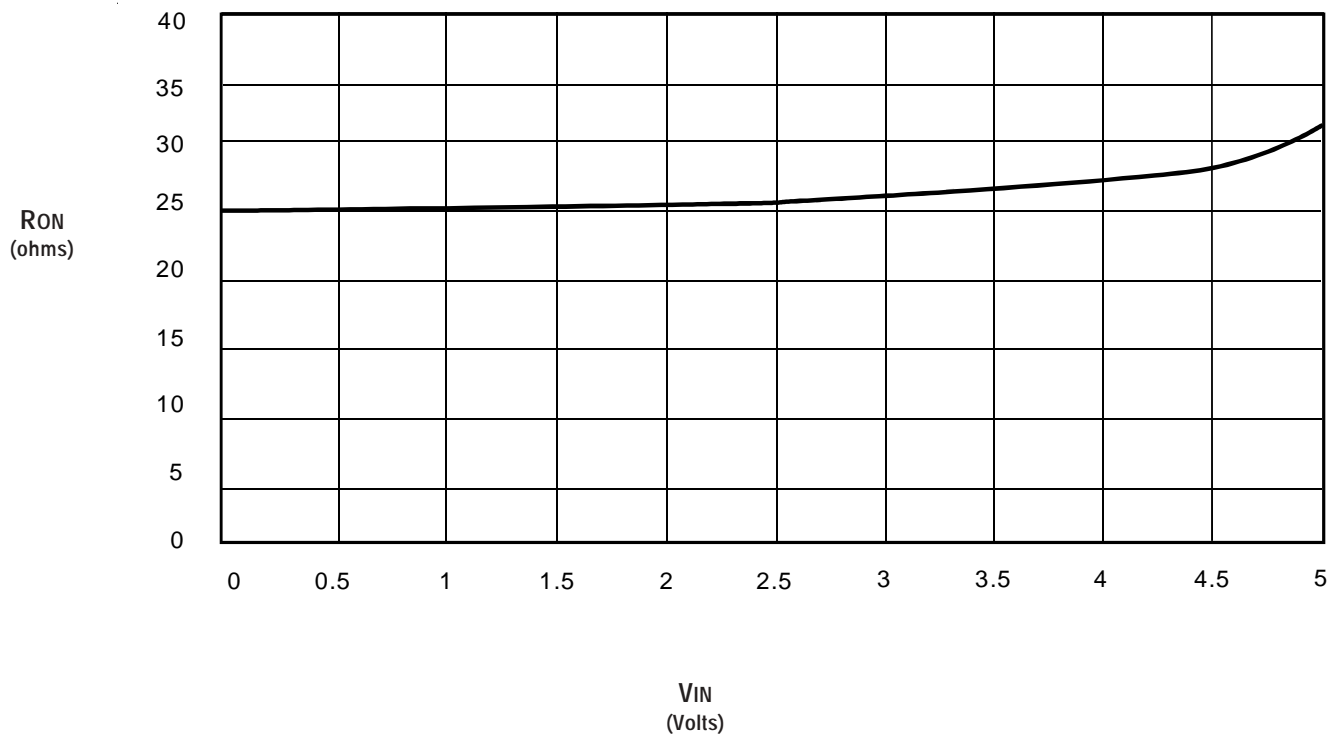
Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

| Symbol | Parameter | Test Conditions | | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|-----------|--|---|---|------------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Voltage | Guaranteed Logic HIGH for Control Inputs | $V_{CC} = 2.3\text{V}$ to 2.7V | | 1.7 | — | — | V |
| | | | $V_{CC} = 2.7\text{V}$ to 3.6V | | 2 | — | — | |
| V_{IL} | Input LOW Voltage | Guaranteed Logic LOW for Control Inputs | $V_{CC} = 2.3\text{V}$ to 2.7V | | — | — | 0.7 | V |
| | | | $V_{CC} = 2.7\text{V}$ to 3.6V | | — | — | 0.8 | |
| I_{IN} | Input Leakage Current (Control Inputs) | $0\text{V} \leq V_{IN} \leq V_{CC}$ | | | — | — | ± 1 | μA |
| I_{OZ} | Off-State Current (Hi-Z) | $0\text{V} \leq V_{OUT} \leq 5\text{V}$, Switches OFF | | | — | — | ± 1 | μA |
| I_{OFF} | Data Input/Output Power Off Leakage | V_{IN} or V_{OUT} 0V to 5V , $V_{CC} = 0\text{V}$ | | | — | — | ± 1 | μA |
| R_{ON} | Switch ON Resistance | $V_{CC} = 2.3\text{V}$ Typical at $V_{CC} = 2.5\text{V}$ | $V_{IN} = 0\text{V}$ | $I_{ON} = 30\text{mA}$ | 18 | 27 | 39 | Ω |
| | | | $V_{IN} = 1.7\text{V}$ | $I_{ON} = 15\text{mA}$ | 18 | 28 | 41 | |
| | | $V_{CC} = 3\text{V}$ | $V_{IN} = 0\text{V}$ | $I_{ON} = 30\text{mA}$ | 18 | 25 | 38 | |
| | | | $V_{IN} = 2.4\text{V}$ | $I_{ON} = 15\text{mA}$ | 18 | 26 | 40 | |

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^{\circ}\text{C}$.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 3.3\text{V}$



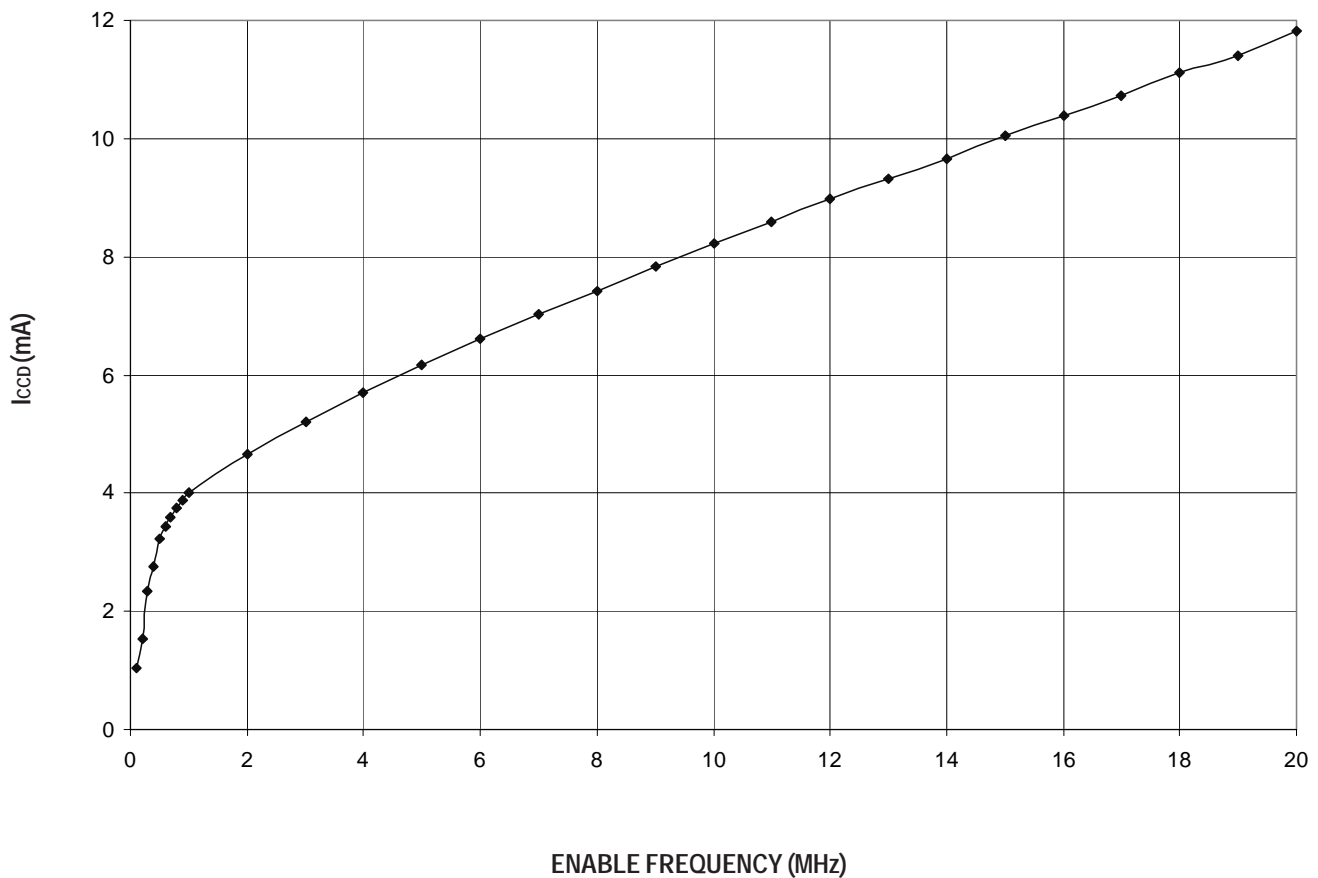
POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|------------------|---|---|--|------|------|------|
| I _{CCQ} | Quiescent Power Supply Current | V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0 | — | 4 | 12 | mA |
| ΔI _{CC} | Power Supply Current ^(2,3) per Input HIGH | V _{CC} = Max., V _{IN} = 3V, f = 0 per Control Input | — | — | 30 | μA |
| I _{CCD} | Dynamic Power Supply Current per Output Enable Control Input ⁽⁴⁾ | V _{CC} = 3.3V, A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle | See Typical I _{CCD} vs Enable Frequency graph below | | | |

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per input driven at the specified level. A and B pins do not contribute to ΔI_{CC}.
3. This parameter is guaranteed but not tested.
4. This parameter represents the current required to switch internal capacitance at the specified frequency. The A and B inputs do not contribute to the Dynamic Power Supply Current. This parameter is guaranteed but not production tested.

TYPICAL I_{CCD} vs ENABLE FREQUENCY CURVE AT V_{CC} = 3.3V



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

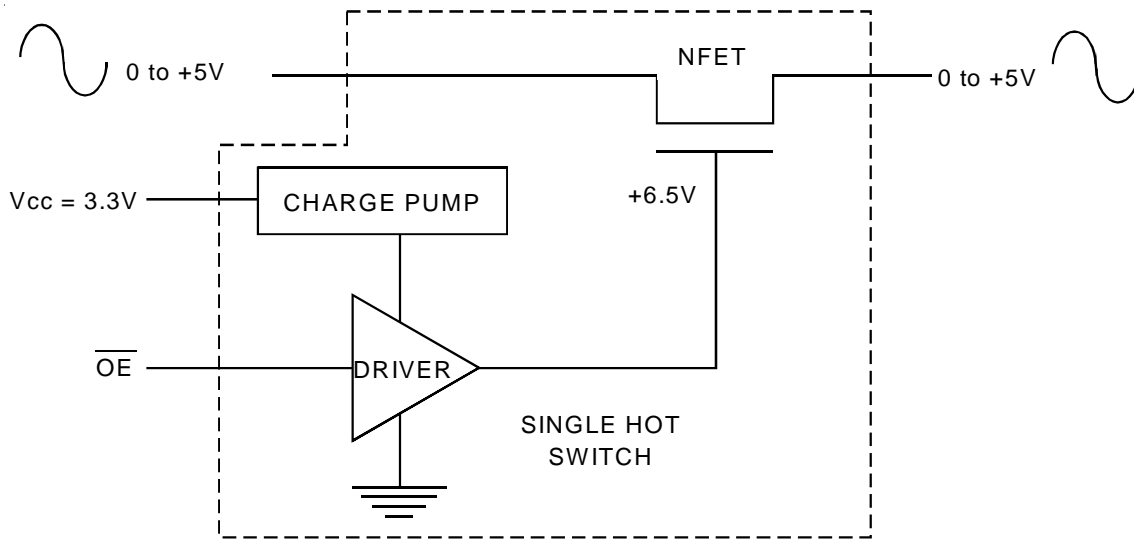
T_A = -40°C to +85°C

| Symbol | Parameter | V _{CC} = 2.5 ± 0.2V ⁽¹⁾ | | V _{CC} = 3.3 ± 0.3V ⁽¹⁾ | | Unit |
|--------------------------------------|---|---|------|---|------|------|
| | | Min. ⁽⁴⁾ | Max. | Min. ⁽⁴⁾ | Max. | |
| t _{PLH} t _{PHL} | Data Propagation Delay ^(2,3) Ax to/from Bx | — | 0.9 | — | 1.35 | ns |
| t _{PZL} t _{PZH} | Switch Turn-On Delay $\overline{\text{OEx}}$ to Ax/Bx | 1.5 | 9 | 1.5 | 8 | ns |
| t _{PLZ} t _{PHZ} | Switch Turn-Off Delay $\overline{\text{OEx}}$ to Ax/Bx | 1.5 | 7.5 | 1.5 | 7.5 | ns |
| f _{OEx} | Operating Frequency - Enable ^(2,5) | — | 10 | — | 20 | MHz |

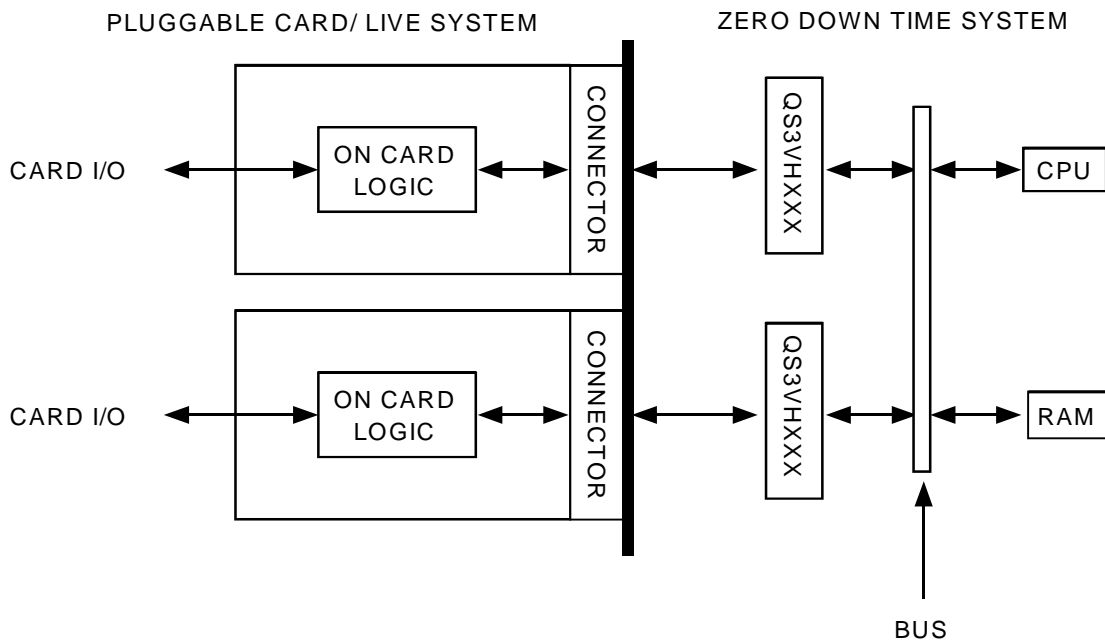
NOTES:

1. See Test Conditions under TEST CIRCUITS AND WAVEFORMS.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 1.35ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums are guaranteed but not production tested.
5. Maximum toggle frequency for $\overline{\text{OEx}}$ control input (pass voltage > V_{CC}, V_{IN} = 5V, R_{LOAD} ≥ 1MΩ, no C_{LOAD}).

SOME APPLICATIONS FOR HOTSWITCH PRODUCTS



Rail-to-Rail Switching

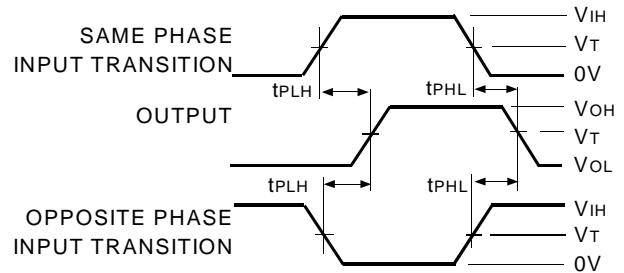


Hot-Swapping

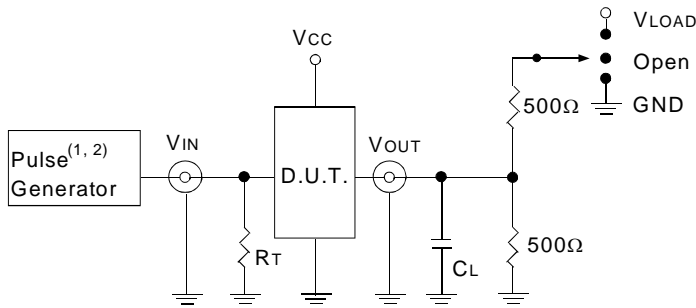
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

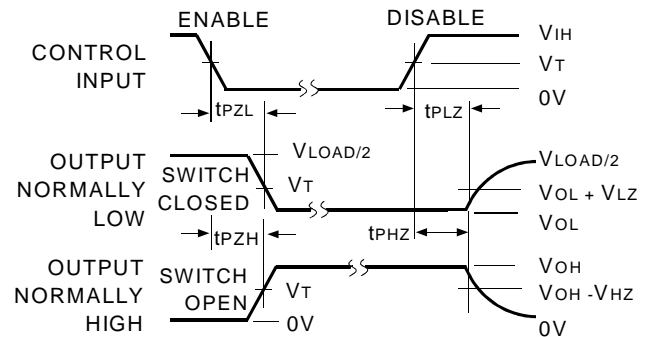
| Symbol | V _{CC} ⁽¹⁾ = 3.3V ± 0.3V | V _{CC} ⁽²⁾ = 2.5V ± 0.2V | Unit |
|-------------------|--|--|------|
| V _{LOAD} | 6 | 2 x V _{CC} | V |
| V _{IH} | 3 | V _{CC} | V |
| V _T | 1.5 | V _{CC} /2 | V |
| V _{LZ} | 300 | 150 | mV |
| V _{HZ} | 300 | 150 | mV |
| C _L | 50 | 30 | pF |



Propagation Delay



Test Circuits for All Outputs



NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

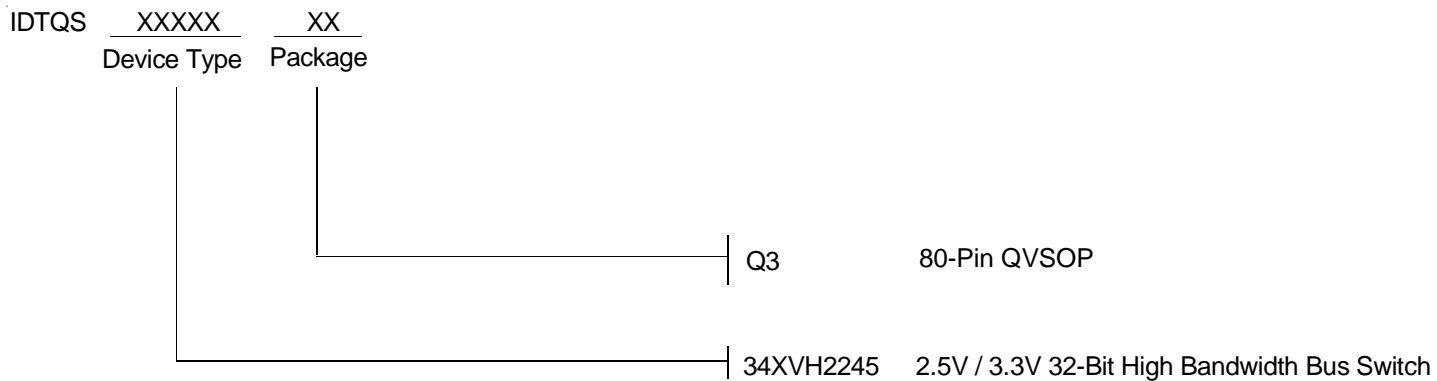
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|------------------------------------|-------------------|
| t _{PLZ} /t _{PZL} | V _{LOAD} |
| t _{PHZ} /t _{PZH} | GND |
| t _{PD} | Open |

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

- 8/6/2002 Updated according to PCN Logic-0206-11
- 3/3/2003 Changed Icc limits



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