Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805/A
IDT49FCT806/A

FEATURES:

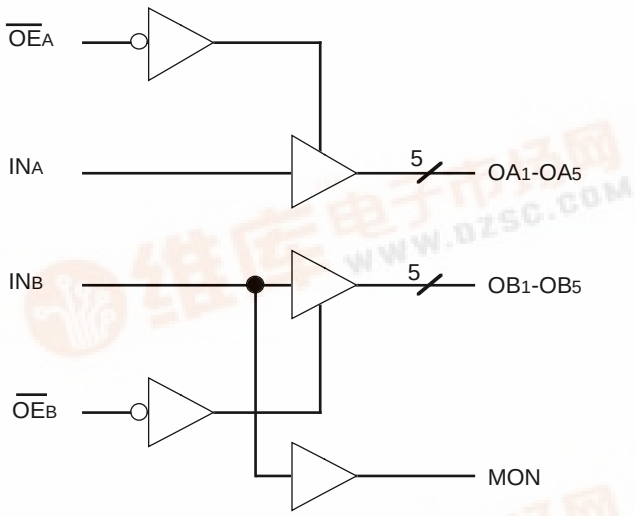
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 700ps (max.)
- Low duty cycle distortion < 1ns (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- Rail-to-rail output voltage swing
- High drive: -24mA I_{OH}, 64mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- Available in DIP, SOIC, SSOP (805 only), QSOP (805 only), Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced dual metal CMOS technology. The IDT49FCT805/A is a non-inverting clock driver and the IDT49FCT806/A is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The devices feature a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The IDT49FCT805/A and IDT49FCT806/A offer low capacitance inputs with hysteresis. Rail-to-rail output swing improves noise margin and allows easy interface with CMOS inputs.

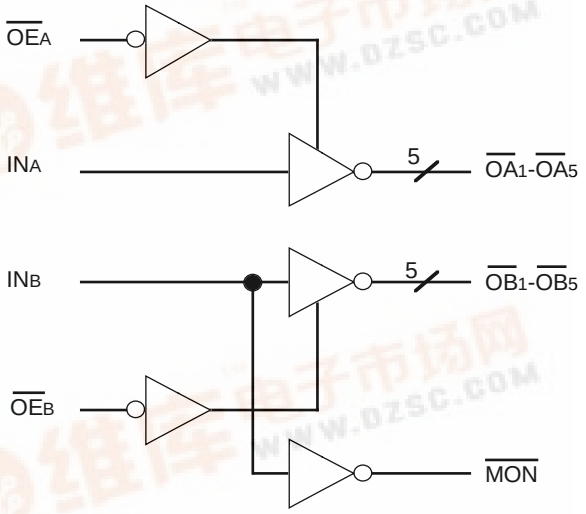
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 01

IDT49FCT806



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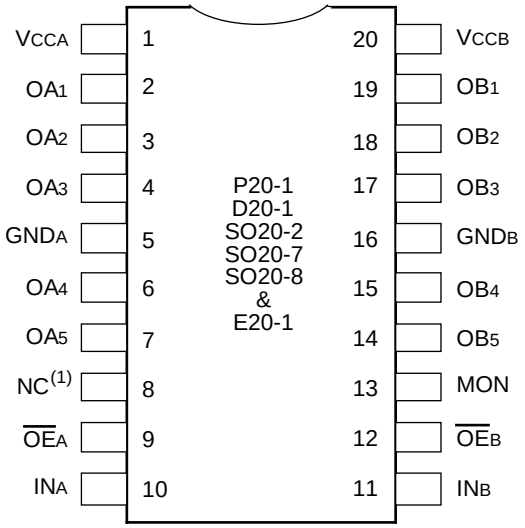
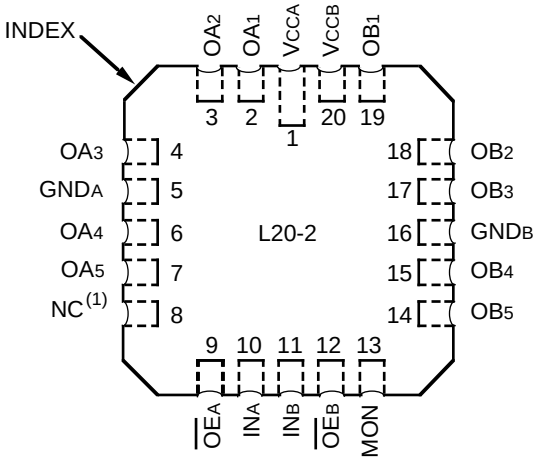
PIN CONFIGURATIONS

IDT49FCT805



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

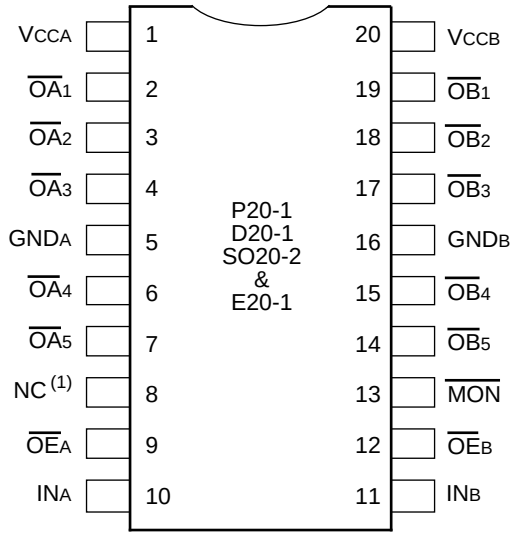
2574 drw 03



LCC
TOP VIEW

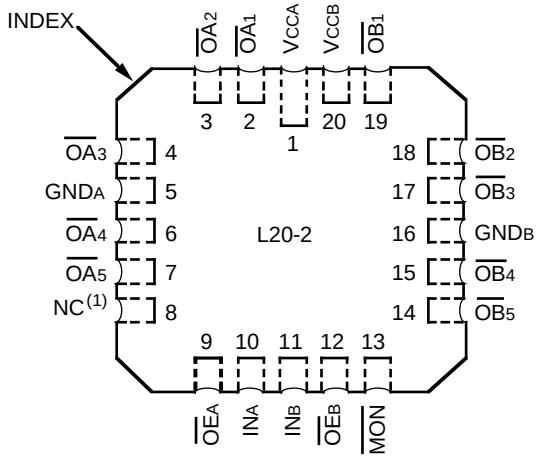
2574 drw 04

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 05



LCC
TOP VIEW

2574 drw 06

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs (FCT805)
$\overline{OA}_n$, $\overline{OB}_n$	Clock Outputs (FCT806)
MON	Monitor Output (FCT805)
$\overline{MON}$	Monitor Output (FCT806

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NOTE:

1. Pin 8 is not internally connected on devices with a "K" prefix in the date code. On older devices, pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at the board level.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(1)

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON	$\overline{OA}_n$, $\overline{OB}_n$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

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NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current(5)	V_{CC} = Max.	V_I = GND	—	—	±1	µA
I_{OZH}	Off State (HIGH Z)(5)	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	Output Current(5)		V_O = GND	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN}= –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	3.6	4.3	—	
			I_{OH} = -24mA MIL. I_{OH} = -24mA COM'L.	2.4	3.8	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL}= 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OH} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	
V_H	Input Hysteresis for all inputs	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	1.0	2.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.20	mA/ MHz/bit
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo= 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ =V_{CC} Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	3.8	
		V_{CC} = Max. Outputs Open fo = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.1	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.1	8.5[5]	

2574 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O= Output Frequency
   N_O= Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	6.3	1.5	5.3	1.5	6.0	ns
t_R	Output Rise Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
$t_{SK}(o)$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.9	—	0.7	—	0.9	ns
$t_{SK}(p)$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL}-t_{PLH}\rvert$)		—	1.0	—	1.1	—	1.0	—	1.1	ns
$t_{SK}(t)$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	8.0	1.5	8.5	1.5	8.0	1.5	8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	7.0	1.5	7.5	1.5	7.0	1.5	7.5	ns

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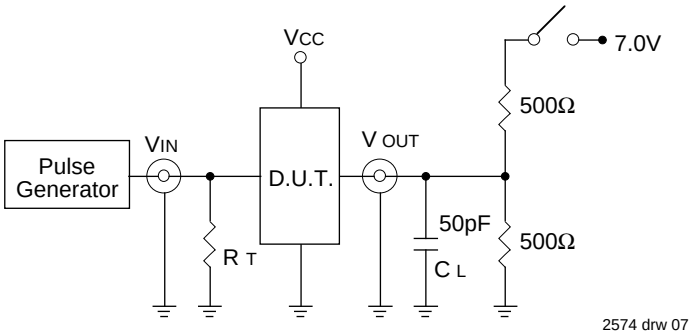
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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ENABLE AND DISABLE TIME SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

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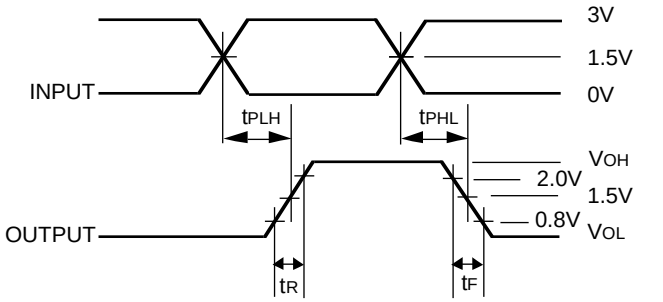
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

PACKAGE DELAY



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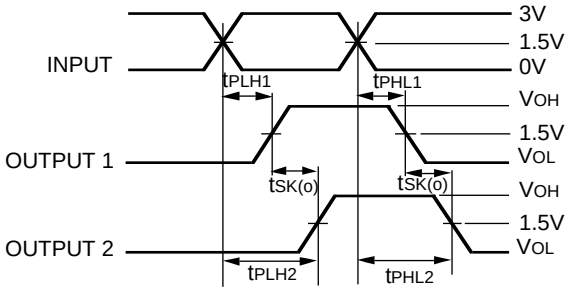
OUTPUT SKEW - tSK(o)



$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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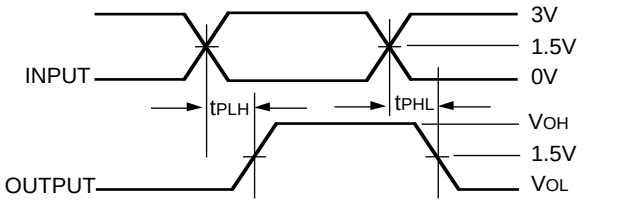
PULSE SKEW - tSK(p)



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

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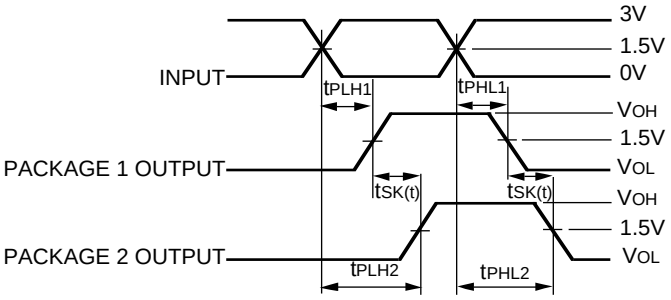
PACKAGE SKEW - tSK(t)



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Package 1 and Package 2 are same device type and speed grade

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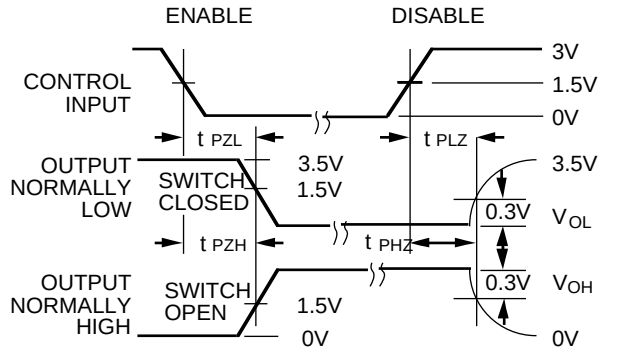
ENABLE AND DISABLE TIMES



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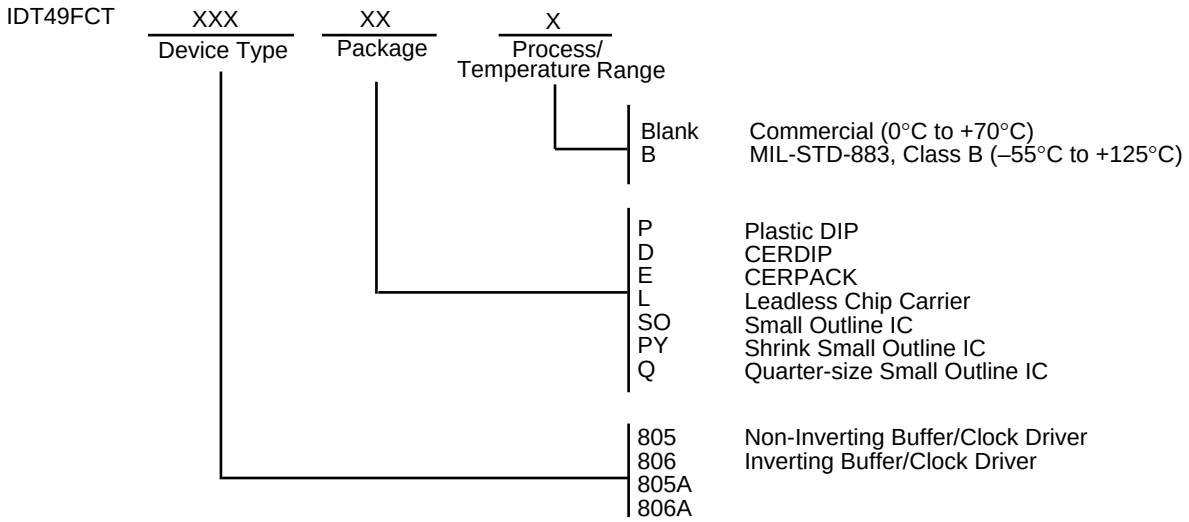
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0MHz$; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

ORDERING INFORMATION



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