



Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805BT/CT
IDT49FCT806BT/CT

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA IOH, 48mA IOL
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, QSOP, Cerpack and LCC packages

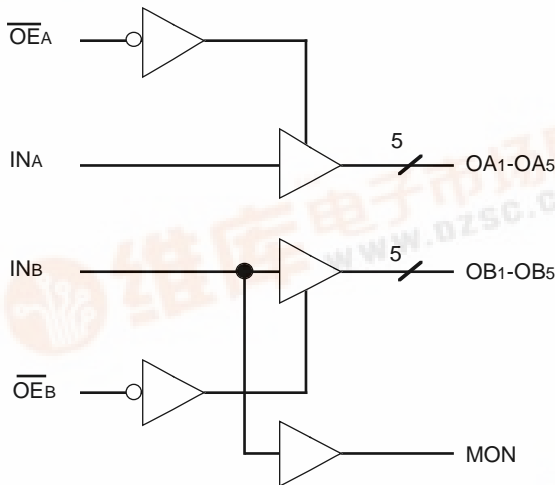
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805BT/CT and IDT49FCT806BT/CT are clock drivers built using advanced dual metal CMOS technology. The IDT49FCT805BT/CT is a non-inverting clock driver and the IDT49FCT806BT/CT is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The 805BT/CT and 806BT/CT have extremely low output skew, pulse skew, and package skew. The devices has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The 805BT/CT and 806BT/CT offer low capacitance inputs with hysteresis.

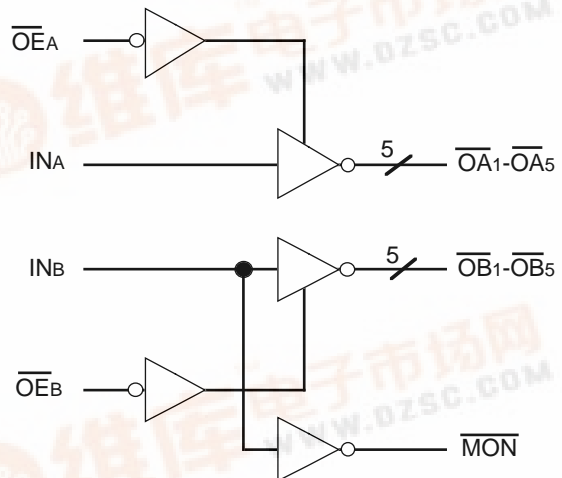
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805T



2920 drw 01

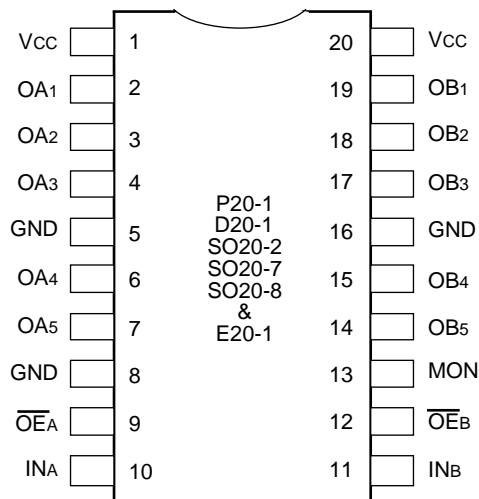
IDT49FCT806T



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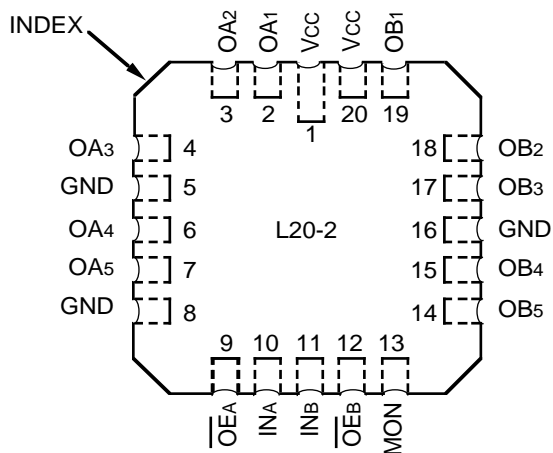
PIN CONFIGURATIONS

IDT49FCT805T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

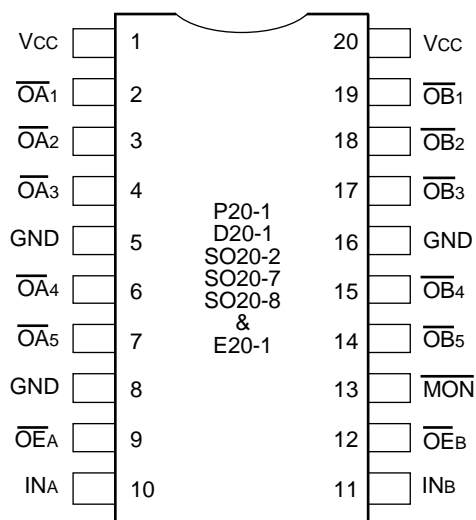
2920 drw 03



LCC
TOP VIEW

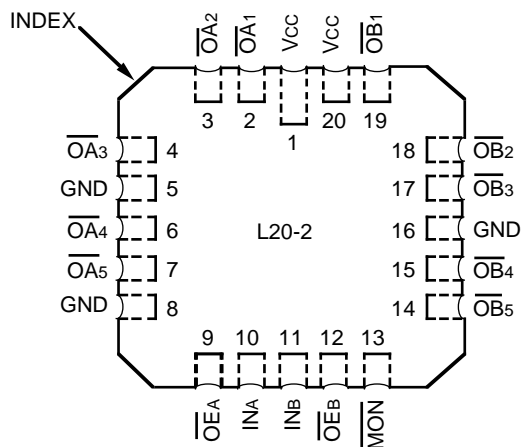
2920 drw 04

IDT49FCT806T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

2920 drw 05



LCC
TOP VIEW

2920 drw 06

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OA _n , OB _n	Clock Outputs (FCT805T)
$\overline{OA}_n, \overline{OB}_n$	Clock Outputs (FCT806T)
MON	Monitor Output (FCT805T)
\overline{MON}	Monitor Output (FCT806T)

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FUNCTION TABLE⁽¹⁾

Inputs		Outputs			
		49FCT805T		49FCT806T	
$\overline{OE}_A, \overline{OE}_B$	INA, INB	OA _n , OB _n	MON	$\overline{OA}_n, \overline{OB}_n$	\overline{MON}
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:

1. H = HIGH, L = LOW, Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals.
- Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

NOTE:

2920 Ink 04

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁵⁾	V _{CC} = Max. V _I = 2.7V	—	—	±1	µA
I _{IL}	Input LOW Current ⁽⁵⁾	V _{CC} = Max. V _I = 0.5V	—	—	±1	µA
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max. V _O = 2.7V	—	—	±1	µA
I _{OZL}		V _O = 0.5V	—	—	±1	µA
I _I	Input HIGH Current ⁽⁵⁾	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	±1	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND	-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.3	—	V
		I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	µA
V _H	Input Hysteresis for all inputs	—	—	150	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	5	500	µA

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ± 5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/$ MHz/bit
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_o = 25\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	4.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_o = 50\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	33	55.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	33.5	57.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input; ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_o = \text{Output Frequency}$
 $N_o = \text{Number of Outputs at } f_o$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE^(3,4)

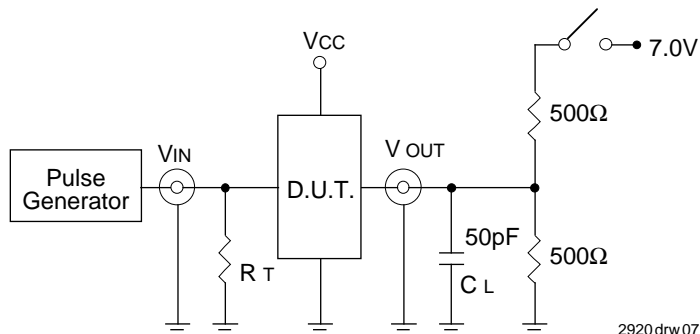
Symbol	Parameter	Condition ⁽¹⁾	IDT49FCT805BT/806BT				IDT49FCT805CT/806CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH}	Propagation Delay	C _L = 50pF R _L = 500Ω	1.5	5.0	1.5	5.7	1.5	4.5	1.5	5.2	ns
t _{PHL}	IN _A to OA _n , IN _B to OB _n										
t _R	Output Rise Time		—	1.5	—	2.0	—	1.5	—	2.0	ns
t _F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
t _{SK(o)}	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.9	—	0.5	—	0.7	ns
t _{SK(p)}	Pulse skew: skew between opposite transitions of same output (t _{PHL} –t _{PLH})		—	0.7	—	0.9	—	0.6	—	0.8	ns
t _{SK(t)}	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1.5	—	1.0	—	1.2	ns
t _{PZL}	Output Enable Time		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns
t _{PZH}	\overline{OE}_A to OA _n , \overline{OE}_B to OB _n										
t _{PLZ}	Output Disable Time	1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns	
t _{PHZ}	\overline{OE}_A to OA _n , \overline{OE}_B to OB _n										

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, t_{SK(t)} are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



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ENABLE AND DISABLE TIME SWITCH POSITION

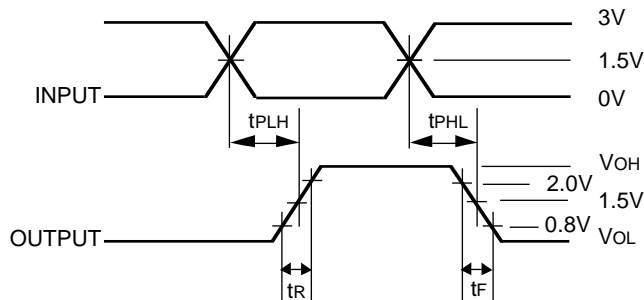
Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

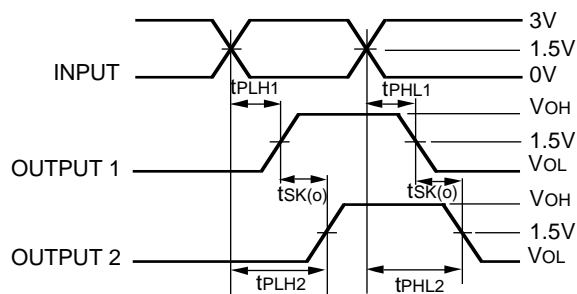
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PACKAGE DELAY



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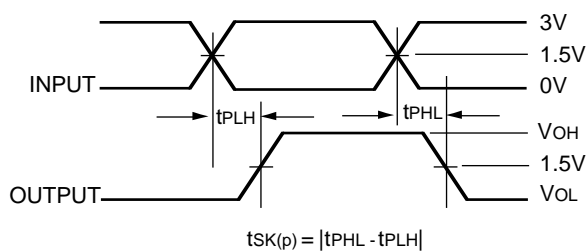
OUTPUT SKEW- tsk(o)



$$tsk(o) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

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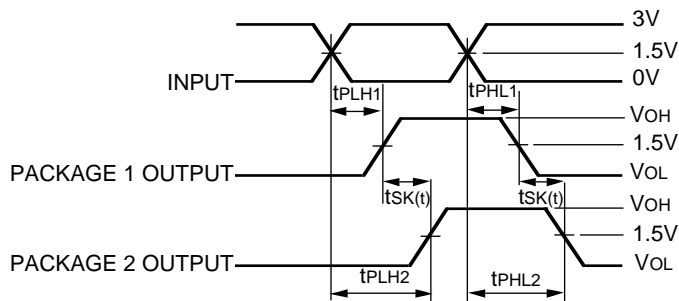
PULSE SKEW - tsk(p)



$$tsk(p) = |tPHL - tPLH|$$

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PACKAGE SKEW - tsk(t)

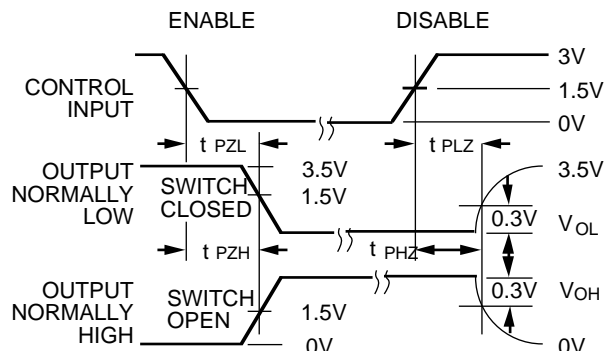


$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Package 1 and Package 2 are same device type and speed grade

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ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION

