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QUAD PCM CODEC WITH PROGRAMMABLE GAIN

IDT821034

FEATURES:

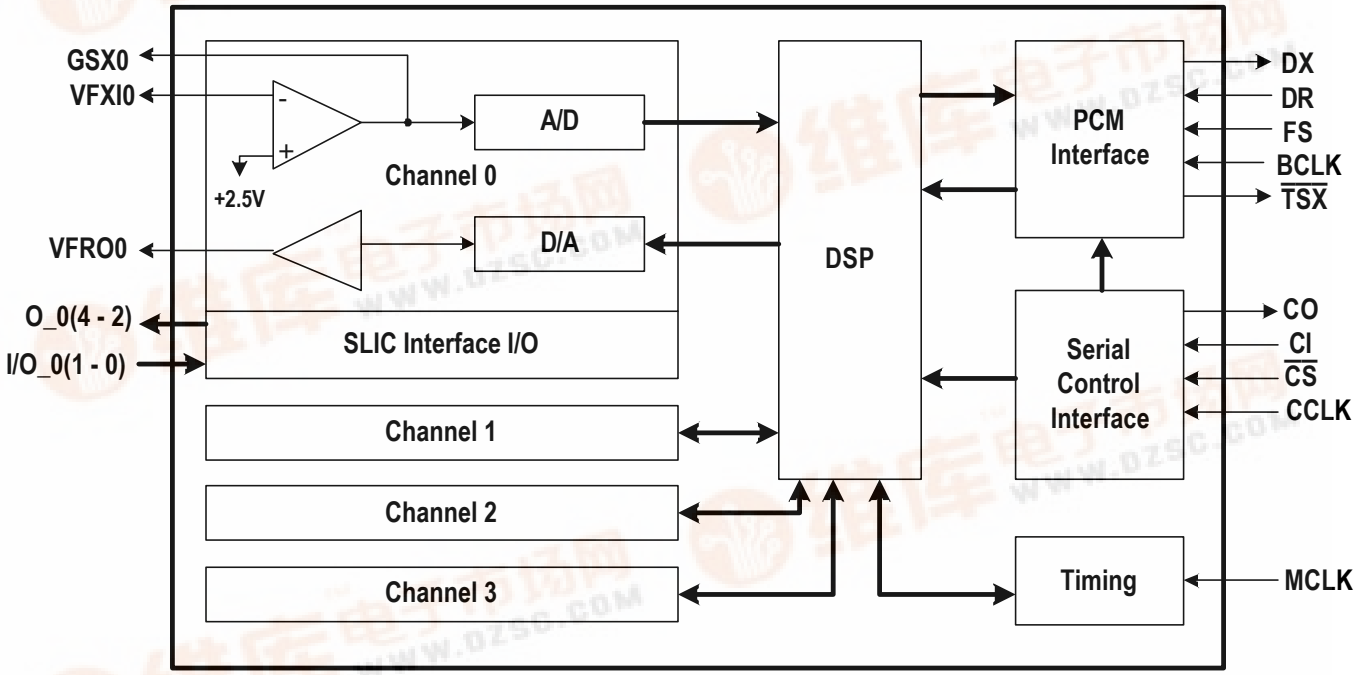
- 4 channel CODEC with on-chip digital filters
- Software Selectable A-law/μ-law companding
- Programmable gain setting
- Automatic master clock frequency selection: 2.048MHz, 4.096 MHz or 8.192MHz
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512 kbits/s to 8.192 Mbits/s
- 5 SLIC signaling pins per channel
- Flexible Serial Control Interface to microcontroller
- Software programmable timing modes
- TTL and CMOS compatible digital I/O
- Meets or exceeds ITU-T G.711 - G.714 requirements
- +5 V single power supply
- Low power consumption: 100mW Typ.
- Operating temperature range: -40 °C to +85 °C
- Packages available: 52 pin PQFP

DESCRIPTION:

The IDT821034 is a single-chip, four channel PCM CODEC with on-chip filters and programmable gain setting. This device provides both μ-Law and A-Law companding digital-to-analog and analog-to-digital conversions based on ITU-T G.711 - G.714 specifications. The digital filters in IDT821034 provides the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. The IDT821034 has a flexible PCM interface with software selectable timing modes and independently programmable time slot for each transmit and receive channel. It also integrates the SLIC signaling functions through internal registers. The CODEC and SLIC control/status registers are accessed via the Serial Control Interface.

The IDT821034 can be used in digital telecommunication applications such as PBX, Central Office Switch, Digital Telephone and Integrated Voice/ Data Access Unit.

FUNCTIONAL BLOCK DIAGRAM



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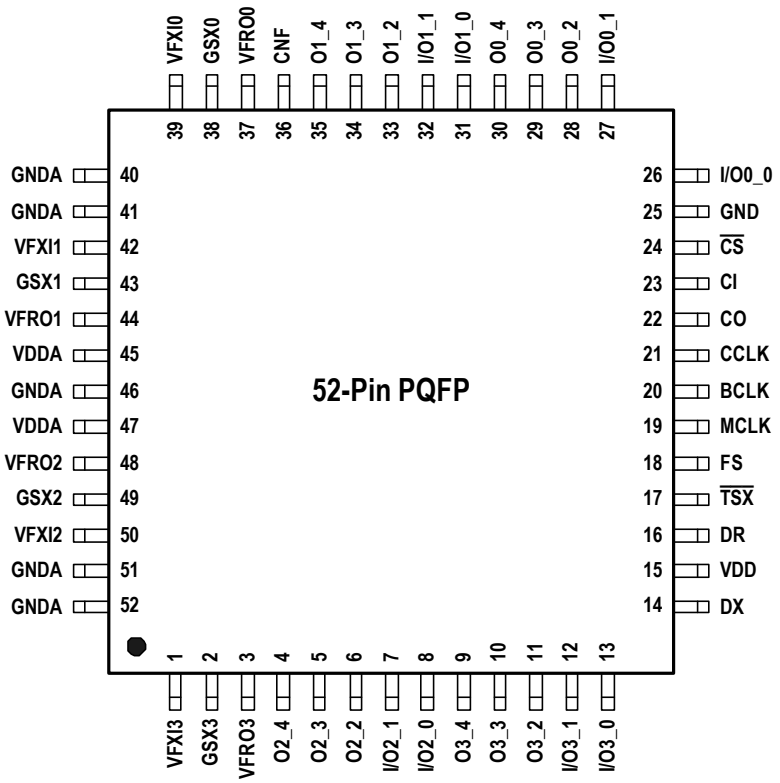
PIN CONFIGURATIONS



PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA	--	46 51 52 40 41	**Analog Ground.** All ground pins should be connected to the ground plane of the circuit board.
VDDA	--	47 45	**+5 V Analog Power Supply.** This pin should be bypassed to ground using 0.1µF capacitor. All power supply pins should be connected to the power plane of the circuit board.
VFRO3 VFRO2 VFRO1 VFRO0	O	3 48 44 37	**Voice Frequency Receiver Output.** This is the output of receive power amplifier. It can drive 2000 Ω (or greater) load.
GSX3 GSX2 GSX1 GSX0	O	2 49 43 38	**Gain Setting Transmit Amplifier Output.** This pin is the output of the gain setting amplifier, and the input to the differential transmit filter. It should be connected to the corresponding VFXI pin through a resistive network to set the transmit gain. Refer to Figure 5 for details.
VFXI3 VFXI2 VFXI1 VFXI0	I	1 50 42 39	**Voice Frequency Transmitter Input.** This pin is the input to the gain setting amplifier in the transmit path.
O3_4 O3_3 O3_2	O	9 10 11	**SLIC Signaling Output for Channel 3.**
O2_4 O2_3 O2_2	O	4 5 6	**SLIC Signaling Output for Channel 2.**

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin Number	Description
O1_4 O1_3 O1_2	O	35 34 33	**SLIC Signaling Output for Channel 1.**
O0_4 O0_3 O0_2	O	30 29 28	**SLIC Signaling Output for Channel 0.**
I/O3_1 I/O3_0	I/O	12 13	**SLIC Signaling I/O for Channel 3.**
I/O2_1 I/O2_0	I/O	7 8	**SLIC Signaling I/O for Channel 2.**
I/O1_1 I/O1_0	I/O	32 31	**SLIC Signaling I/O for Channel 1.**
I/O0_1 I/O0_0	I/O	27 26	**SLIC Signaling I/O for Channel 0.**
DX	O	14	**Transmit PCM Data Output.** PCM data is shifted out of DX on rising edges of BCLK.
VDD	--	15	**+5 V Digital Power Supply.** All power supply pins should be connected to the power plane of the circuit board.
DR	I	16	**Receive PCM Data Input.** PCM data is shifted into DR on falling edges of BCLK.
$\overline{TSX}$	O	17	**Time Slot Indicator Output, Open Drain** This pin pulses low during the active time slot of each channel. A low level on this pin indicates active DX output.
FS	I	18	**Frame Synchronization.** The FS pulse serves as the reference to time slots. The width of the FS pulse should be at least one BCLK cycle.
MCLK	I	19	**Master Clock.** Master Clock provides the clock for DSP. It can be 2.048 MHz, 4.096 MHz or 8.192 MHz. It must be synchronous to FS.
BCLK	I	20	**Bit Clock.** Bit Clock shifts out PCM data on DX pin and shifts in PCM data on DR pin. The clock can vary from 512 kHz to 8.192 MHz at 64 kHz increment, depending on the time slot requirement of the system.
CCLK	I	21	**Serial Control Interface Clock.** This is the clock for Serial Control Interface. It can be up to 8.192 MHz.
CO	O	22	**Serial Control Interface Data Tri-State Output.** This pin is used to monitor SLIC working status. It is in high impedance state when $\overline{CS}$ is high.
CI	I	23	**Serial Control Interface Data Input.** Data input on this pin can control both CODEC and SLIC.
$\overline{CS}$	I	24	**Chip Select.** A low level on this pin enables the Serial Control Interface.
GND	--	25	**Ground.** All ground pins should be connected to the ground plane of the circuit board.
CNF	O	36	**Capacitor For Noise Filter.** This pin should be connected to GNDA via a 0.1 µF capacitor.

FUNCTIONAL DESCRIPTION

The IDT821034 contains four channel PCM CODEC with on chip digital filters. It provides the four-wire solution for the subscriber line circuitry in digital switches. The device converts analog voice signal into digital PCM samples, and converts digital PCM samples back to analog signal. Digital filters are used to bandlimit the voice signals during conversion.

The frequency of the master clock (MCLK) can be 2.048 MHz, 4.096 MHz or 8.192 MHz. Internal circuitry determines the master clock frequency automatically.

Four channels of serial PCM data are time multiplexed via two pins, DX and DR. The time slots of the four channels can be programmed dynamically. The control words can be written by a microcontroller via the Serial Control Interface. Dynamic time-slot assignment can accommodate 8 to 128 time slots corresponding to the bit clock (BCLK) frequency from 512 kHz to 8.192 MHz.

The IDT821034 offers two timing modes, delay mode and non-delay mode. Mode selection is done by programming the Configuration Register. The two modes are distinguished by time slot zero definition. In delay mode, the time slot zero is defined as starting on the first rising edge of BCLK after FS = '1' is detected by the falling edge of BCLK (Figure 7). While in non-delay mode, the time slot zero starts when both BCLK and FS are high (Figure 8).

The device provides a programmable interface to SLIC (Subscriber Line Interface Circuit). Each channel of the IDT821034 has three output pins and two I/O pins for SLIC signaling. These interface pins are mapped to internal registers and are accessed by the microcontroller via the Serial Control Interface. In this way, the IDT821034 provides high level of integration in line card design.

The Serial Control Interface of IDT821034 consists of four pins (CI, CO, $\overline{CS}$ and CCLK), as shown in Figure 1, for the communication to a microcontroller. Via this interface, the microcontroller can control the CODEC and SLIC working modes as well as monitor the SLIC status.

OPERATION CONTROL

The following operation description applies to all four channels of the IDT821034.

Initial State

The IDT821034 has a built-in power on reset circuit. After initial power up, the device defaults to the following mode:

1. A-law is selected;
2. Delay mode is selected;
3. I/O pins of SLIC interface are set to input mode;
4. SLIC Control and Status Register bits are set to '0';
5. All four channels are placed in standby mode;
6. All transmit and receive time slots are disabled with Time Slot Registers set to zero;
7. DX is set to high impedance state.

Operating Modes

There are two operating modes for each transmit or receive channel: standby mode and normal mode. When the IDT821034 is first powered on, standby mode is the default mode. Microcontroller can also set the device into this mode via the Serial Control Interface. In standby mode, the Serial Control Interface remains active to receive commands from the microcontroller. All other circuits are powered down with the analog outputs placed in high impedance state. All circuits which contain programmed information retain the data in this mode.

Each of the four channels in the IDT821034 can be in either normal mode or standby mode. The mode selection of each channel is done by the microcontroller via the Serial Control Interface. When in normal mode, each channel of the IDT821034 is able to transmit and receive both PCM and analog information. This is the operating mode when a telephone call is in progress.

Gain Programming

Transmit gain and receive gain of each channel in IDT821034 can be varied by programming DSP digital filter coefficients. Transmit gain can be varied within the range of -3 dB to +13 dB; while receive gain can be varied within the range of -13 dB to +3 dB. This function allows the IDT821034 to be used with SLICs of different gain requirement.

Gain programming coefficient can be written into IDT821034 via Serial Control Interface. The detailed operation will be covered in Serial Control Interface description. The gain programming coefficients should be calculated as:

Transmit : Coeff_X = round [gain_X0dB × gain_X]
Receive: Coeff_R = round [gain_R0dB × gain_R]
where:

gain_X0dB = 1820;
gain_X is the target gain;
Coeff_X should be in the range of 0 to 8192.
gain_R0dB = 2506;
gain_R is the target gain;
Coeff_R should be in the range of 0 to 8192.

A gain programming coefficient is 14-bit wide and in binary format. The 7 Most Significant Bits of the coefficient is called GA_MSB_Transmit for transmit path, or is called GA_MSB_Receive for receive path; The 7 Least Significant Bits of the coefficient is called GA_LSB_ Transmit for transmit path, or is called GA_LSB_Receive for receive path.

An example is given below to clarify the calculation of the coefficient. To program a +3 dB gain in transmit path and a -3.5 dB gain in receive path:

Linear Code of +3 dB $= 10^{3/20}$
$= 1.412537545$

Coeff_X = round (1820 × 1.412537545)
= 2571
= 0010100, 0001011
(in binary format)

GA_MSB_Transmit = 0010100
GA_LSB_Transmit = 0001011

Linear Code of -3.5 dB $= 10^{(-3.5/20)}$
$= 0.668343917$

Coeff_R = round (2506 × 0.668343917)
= 1675
= 0001101, 0001011
(in binary format)

GA_MSB_Receive = 0001101
GA_LSB_Receive = 0001011

SIGNAL PROCESSING

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) are used in the IDT821034 to provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering and sample rate conversion.

Transmit Signal Processing

In the transmit path, the analog input signal is received with a gain setting amplifier. The signal gain is set by the resistive feedback network as shown in the application circuit (Figure 5). The output of the gain setting amplifier is connected internally to the input of the anti-alias filter for the oversampling ADC. The digital output of the oversampling ADC is decimated and sent to the DSP. The transmit filter is implemented in the DSP as a digital bandpass filter. The filtered signal is further decimated and compressed to PCM format.

Transmit PCM Interface

The transmit PCM interface clocks the PCM data out of DX pin on rising edges of BCLK according to the time slot assignment. The frame sync (FS) pulse identifies the beginning of a transmit frame, or time slot zero. The time slots for all channels are referenced to FS. The IDT821034 contains user programmable Transmit Time Slot Register for each transmit channel. The register is 7 bits wide and can accommodate up to 128 time slots (corresponding to the maximum BCLK frequency of 8.192 MHz) in each frame. The PCM Data is transmitted serially on DX pin with the Most Significant Bit (MSB), or Bit 7, first.

When the device is first powered up, all transmit time slots are disabled with Transmit Time Slot Registers set to zero. DX pin remains in high-impedance state. To power up or power down each transmit channel, Configuration Register and the corresponding Time Slot Register must be programmed.

Receive Signal Processing

In the receive path, the PCM code is received at the rate of 8,000 samples per second. The PCM code is expanded and sent to the DSP for interpolation and receive channel filtering function. The receive filter is implemented in the DSP as a digital lowpass filter. The filtered signal is then sent to an oversampling DAC. The DAC output is post-filtered and then delivered at VFRO pin by a power amplifier. The amplifier can drive resistive load higher than 2 kΩ.

Receive PCM Interface

The receive PCM interface clocks the PCM data into DR pin on falling edges of BCLK according to the time slot assignment. The receive time slot definition and programming is similar to that of the transmit time slot. The IDT821034 contains a user programmable Receive Time Slot Register for each receive channel. The register is 7 bits wide and can accommodate up to 128 time slots (corresponding to the maximum BCLK frequency of 8.192 MHz) in each frame. The PCM Data is received serially on DR pin with the MSB (Bit 7) first.

When the device is first powered up, all receive time slots are disabled with Receive Time Slot Registers set to zero. Data on DR pin is ignored. To power up or power down each receive channel, Configuration Register and the corresponding Time Slot Register must be programmed.

Serial Control Interface

A Serial Control Interface is provided for a microprocessor to access the control and status registers of IDT821034. The control registers include Configuration Register, Time Slot Registers, SLIC Control Registers and Gain Adjustment Registers. They are used to program the working modes of CODEC and SLIC. The status registers include SLIC Status Registers. They are used to monitor SLIC functions. All registers are 8 bits wide.

The Serial Control Interface consists of CO, CI, $\overline{CS}$ and CCLK pins (see Figure 1). A microprocessor initiates a write or read cycle after low level is asserted on $\overline{CS}$ pin. In the microprocessor write cycle, 8 bits of serial data on CI pin are shifted into the device at falling edges of CCLK. In the microprocessor read cycle, 8 bits of serial data are shifted out of the device on CO pin at rising edges of CCLK. At the end of each 8-bit transaction, the microprocessor sets $\overline{CS}$ high to terminate the cycle. Multiple accesses to the device are separated by an idle state (high level) of $\overline{CS}$. The width of $\overline{CS}$ high level is at least three CCLK cycles.

The IDT821034 has a Configuration Register. Its register bits are designated CR.7 - CR.0. The definition of the bits in Configuration Register is shown in Table 1. If the leading data bit on CI pin is '1' in a microprocessor write cycle, the 8-bit data on CI pin is latched into Configuration Register with MSB first.

There are eight Time Slot Registers for four transmit channels and four receive channels. The definition of the bits in Time Slot Register is shown in Table 2. Since PCM sample rate is 8k samples/sec and each sample is 8 bits wide, each time slot occupies 64 kbits/sec of data rate. The number of time slots in a frame is equal to the ratio of the bit clock frequency (BCLK) to 64 kHz. For the maximum BCLK frequency of 8.192 MHz, the number of time slots in a frame is 8.192MHz/64kHz, or 128. The minimum number of time slots (corresponding to the minimum BCLK frequency of 512 kHz) in a frame is 8. The relationship between frequently used BCLK frequencies and the number of time slots in a frame is shown in Table 3. Bit 6-0 in each Time Slot Register identify the time slot number (0 to 127) of the corresponding transmit or receive channel. Time Slot Registers can be accessed by specifying the transmit/receive select (CR.1 and CR.0) and channel address (CR.3 and CR.2) in Configuration Register. If CR.6 = '0' and the leading data bit on CI pin is '0' in a microprocessor write cycle, the 8-bit data on CI pin is latched into the selected Time Slot Register with MSB first.

There are four SLIC Control Registers for four channel SLIC signaling control. The definition of the bits in a SLIC Control Register is shown in Table 4. SLIC Control Registers can be accessed by specifying the channel address (CR.3 and CR.2) in Configuration Register. If CR[6:4] = '101' and the leading data bit on CI pin is '0' in a microprocessor write or read cycle, the 8-bit data on CI pin is latched into the selected SLIC Control Register with MSB first.

There are four SLIC Status Registers for four channel SLIC monitoring. The bits in each SLIC Status Register are mapped to the SLIC signaling output and I/O pins of the corresponding channel as shown in Table 5. It should be noted that the last 3 bits of the SLIC Status Register are always mapped to I/O1_0, I/O2_0 and I/O3_0. This feature allows a rapid read process of the SLIC status when Channel 0 is selected. The SLIC Status Registers can be accessed by specifying the channel address (CR.3 and CR.2) in the Configuration Register. If CR[6:4] = '101', as a result of the previous write to the Configuration Register, the subsequent microprocessor cycle is a read cycle. The content of the selected SLIC Status Register is shifted out of the device on CO pin with MSB first.

There are 16 Gain Adjustment Registers for both transmit and receive paths of four channels. For each path, there are two

corresponding 8-bit Gain Adjustment Registers: MSB GA Register, which stores the 7 Most Significant bits of gain adjustment coefficient; and LSB GA Register, which stores the 7 Least Significant bits of gain adjustment coefficient. All Gain Adjustment Registers start with '0'. Gain Adjustment Registers can be accessed by specifying the channel address (CR.3 and CR.2) in Configuration Register. If CR[6:4] = '100', CR.0 = '1' and the leading data bit on CI pin is '0' in a microprocessor write cycle, the 8-bit data on CI pin is latched into the selected MSB GA Register with MSB first; If CR[6:4] = '100', CR.0 = '0' and the leading data bit on CI pin is '0' in a microprocessor write cycle, the 8-bit data on CI pin is latched into the selected LSB GA Register with MSB first.

All microprocessor cycles are either write cycles or read cycles. In typical applications, the microprocessor will write control registers as ordered pairs for CODEC Mode programming (Figure 2), SLIC Mode programming (Figure 3), or Gain Mode programming (Figure 4). The first write in the pair is to Configuration Register. This is identified by a leading '1' on CI pin. If CR.6 = '0' after writing Configuration Register, the programming is for CODEC mode and the succeeding operation is a write cycle with a leading '0' on CI pin. The write is intended for the selected Time Slot Register. The timing diagram for CODEC Mode programming is shown in Figure 11. If CR.6 = '1' and CR.5 = '0' and CR.4 = '1' after writing Configuration Register, the programming is for SLIC control function and the succeeding operation is a read/write cycle. The write, also with a leading '0' on CI pin, is intended for the selected SLIC Control Register, while the simultaneous read is from the SLIC Status Register of the same channel. The timing diagram for SLIC Mode programming is shown in Figure 10. If CR.6 = '1', CR.5 = '0' and CR.4 = '0' after writing Configuration Register, the programming is for Gain adjustment function and the succeeding operation is a write cycle with a leading '0' on CI pin. The write is intended for the selected Gain Adjustment Register. The timing diagram for Gain Mode programming is shown in Figure 13.

Configuration Register, Time Slot Registers, SLIC Control Registers and Gain Adjustment Registers are write only registers while SLIC Status Registers are read only registers. Refer to Figure 12 for the detail timing of the Serial Control Interface.

An alternative method of receiving data from SLIC Status Register is designed for IDT821034. This procedure is initiated when a '1111-1110' command appears on CI. To read from the SLIC Status Registers when using this method, Configuration Register should be set to indicate the following operation is a SLIC programming, and then assert a '1111-1111' command on CI. The data from SLIC Status Registers will clock out of CO pin on CCLK rising edges when $\overline{CS}$ is low. The timing diagram of this method is shown in Figure 14. When using this method, CO and CI pins can be connected together. Either CO or CI will be in high Z state, depending on the Serial Control Interface is in write cycle or read cycle. When a command of '1111-1101' appears on CI, the device will terminate this procedure.

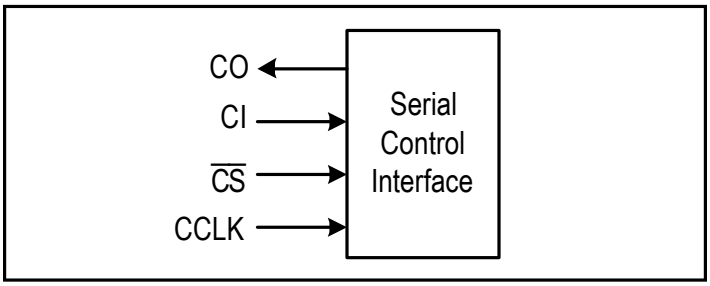


Figure 1. Serial Control Interface Signals

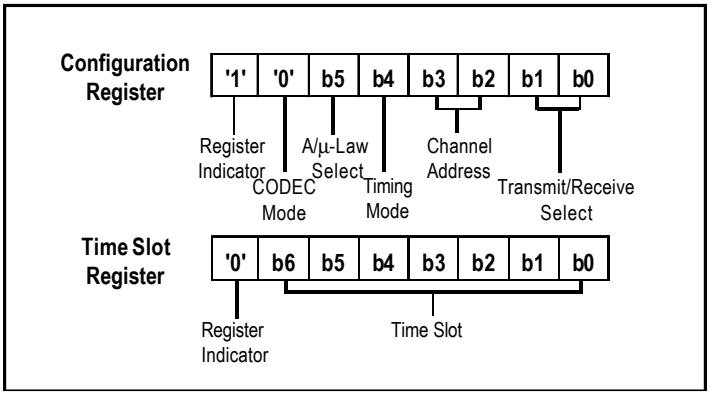


Figure 2. Registers for CODEC Mode Programming

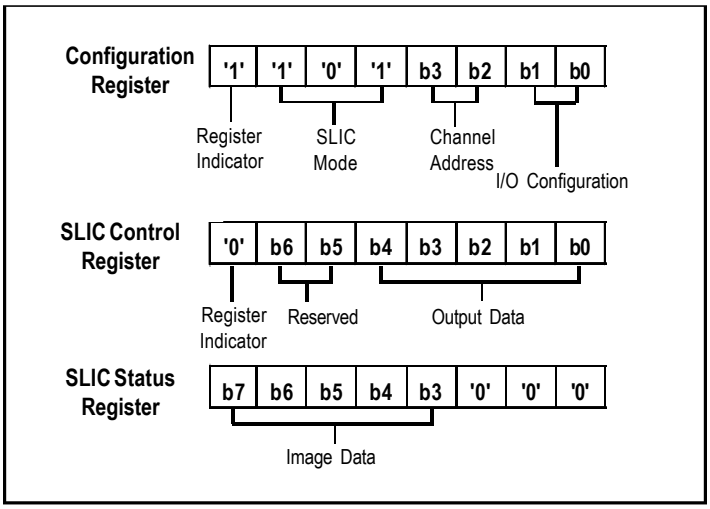


Figure 3. Registers for SLIC Mode Programming

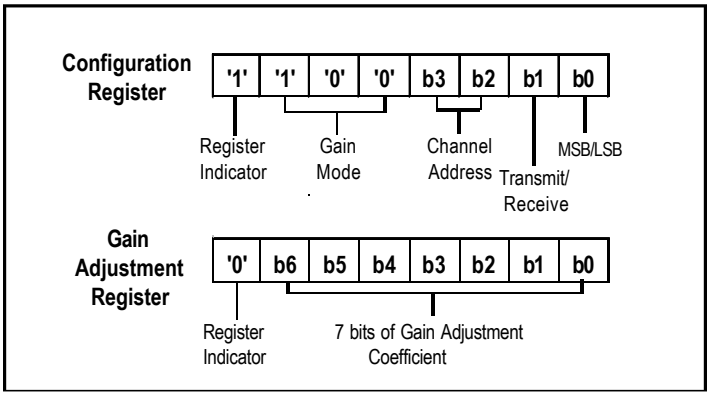


Figure 4. Registers for Gain Mode Programming

Bit	Name		Value	Description
CR.7	Register Indicator			Always '1'
CR.6 **CR.5**	Mode Select 1 Mode Select 0		00 01 10 11	μ-Law CODEC Mode (This is global setting for all channels.) A-Law CODEC Mode (This is global setting for all channels.) SLIC/Gain Mode Reserved (This mode should not be programmed for normal operation.)
CR.4	CODEC Mode (CR.6 = '0')	Timing Mode Select	0 1	Non-delay Mode (This is global setting for all channels.) Delay Mode (This is global setting for all channels.)
	SLIC/Gain Mode (CR.6 = '1')	SLIC/Gain Mode Select	0 1	Gain Mode SLIC Mode
CR.3 **CR.2**	Channel Address 1 Channel Address 0		00 01 10 11	Select Channel 0 for CODEC or SLIC programming Select Channel 1 for CODEC or SLIC programming Select Channel 2 for CODEC or SLIC programming Select Channel 3 for CODEC or SLIC programming
CR.1 **CR.0**	CODEC Mode (CR.6 = '0')	Transmitter Select Receiver Select	00 01 10 11	Channel power down Channel power up with receive time slot assignment Channel power up with transmit time slot assignment Channel power up with both receive and transmit time slot assignment
	SLIC Mode (CR.6 = '1', CR.4 = '1')	I/O_1 Configuration I/O_0 Configuration	00 01 10 11	Configure I/O_1 as an output pin and I/O_0 as an output pin Configure I/O_1 as an output pin and I/O_0 as an input pin Configure I/O_1 as an input pin and I/O_0 as an output pin Configure I/O_1 as an input pin and I/O_0 as an input pin
	Gain Mode (CR.6 = '1', CR.4 = '0')	CR.1: Transmit/Receive Select	0 1	Receive gain will be adjusted Transmit gain will be adjusted
		CR.0: MSB/LSB Select	0 1	Indicates the following 8 bits contain the 7 Least Significant bits of gain adjustment coefficient Indicates the following 8 bits contain the 7 Most Significant bits of gain adjustment coefficient

Table 1. Description of Configuration Register

Bit	Name	Description
7	Register Indicator	Always '0'
6 5 4 3 2 1 0	Time Slot Bit 6 Time Slot Bit 5 Time Slot Bit 4 Time Slot Bit 3 Time Slot Bit 2 Time Slot Bit 1 Time Slot Bit 0	Bit 6-0 indicate which time slot is selected for the transmit/receive channel. Time Slot 0 is aligned to FS.

Table 2. Definition of Time Slot Register

BCLK Frequency	512 kHz	1.544 MHz	2.048 MHz	4.096 MHz	8.192 MHz
Number of Time Slot	8	24	32	64	128

Table 3. Relationship between BCLK Frequency and Time Slot Number

Bit	Name	Description
7	Register Indicator	Always '0'
6	--	Reserved, always '0'
5	--	Reserved, always '0'
4	O_4 Data	Output data on O_4 pin of the selected channel
3	O_3 Data	Output data on O_3 pin of the selected channel
2	O_2 Data	Output data on O_2 pin of the selected channel
1	I/O_1 Data	Output data on I/O_1 pin (if defined as an output) of the selected channel
0	I/O _0 Data	Output data on I/O_0 pin (if defined as an output) of the selected channel

Table 4. Definition of SLIC Control Register

Bit	Name	Description
7	I/On_0 Image	Mapped to I/On_0 pin of the selected channel n
6	I/On_1 Image	Mapped to I/On_1 pin of the selected channel n
5	On_2 Image	Mapped to On_2 pin of the selected channel n
4	On_3 Image	Mapped to On_3 pin of the selected channel n
3	On_4 Image	Mapped to On_4 pin of the selected channel n
2	I/O1_0 Image	Always mapped to the I/O1_0 pin
1	I/O2_0 Image	Always mapped to the I/O2_0 pin
0	I/O3_0 Image	Always mapped to the I/O3_0 pin

Table 5. Definition of SLIC Status Register

APPLICATION NOTE

The IDT821034 is mainly used in line card application. Figure 5 shows a typical system with telephony line interface.

The IDT821034 offers not only encoding/decoding function, but also a signaling channel, which can simplify the circuit design of the control interface. In addition, the dynamic time slot assignment of IDT821034 reduces the hardware requirement for PCM interface. The device also supports 8.192 Mbps PCM data rate, which can increase the time slot density up to 128.

Signal to total distortion ratio (both STD_X and STD_R) are guaranteed over -55 dBm0 to +3 dBm0 range with a specific gain setting (0 dB for both transmit path and receive path). Since there is a finite noise floor associated with the quantization effect of both data converters and digital filter coefficients, the overall signal to total distortion ratio of each path is a function of the gain setting. In system design, attention should be paid to the gain setting for the best signal to total distortion performance.

Generally, a channel gain of a line-card system is contributed by both SLIC and CODEC. In a system design using IDT821034, the SLIC gain should be taken into account to optimize the SNR. In the transmit path of IDT821034, there are two resistors (R1 and R3 in Figure 5) which enable the analog gain to be adjusted around 0 dB. Further gain adjustment can be obtained by programming the DSP filters. Since this adjustment is close to 0 dB, the SNR remains at the optimum value. In the receive path of IDT821034, analog gain adjustment is not available. Thus, the adjustment of CODEC gain will be performed only by programming the DSP filters. In this way, the SLIC gain should be such that the DSP gain is closest to 0 dB. This will maximize the achievable SNR in the overall system. For example, if the design target for receive path gain is -3.5 dB and -7 dB for local and long distance calls respectively, the recommended solution is to set SLIC gain at -3.5 dB. As a result, the gain of CODEC, which is adjusted by programming DSP coefficients, will be 0 dB and -3.5 dB.

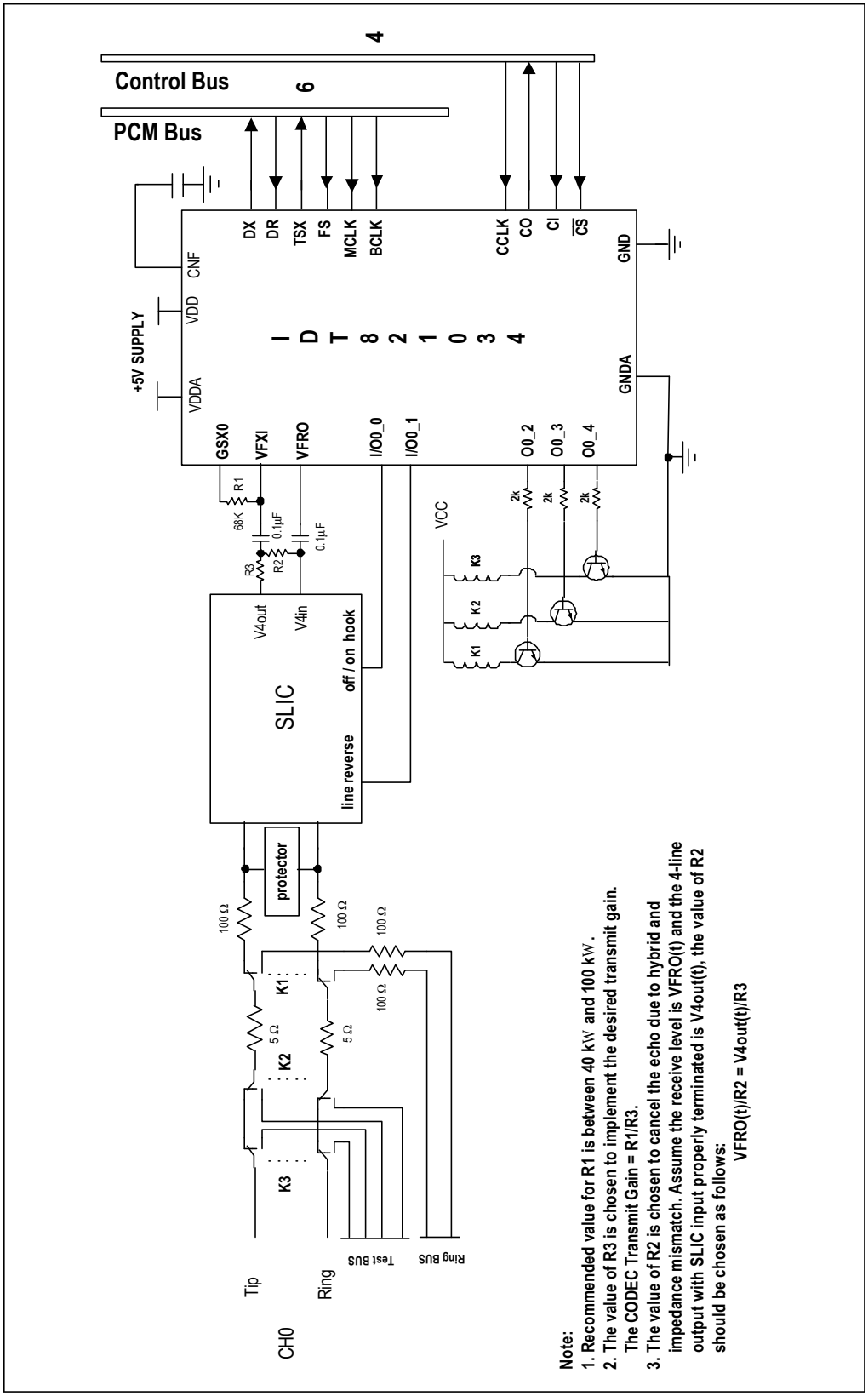


Figure 5. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Com'l & Ind'l	Unit
Power Supply Voltage	≤ 6.5	V
Voltage on Any Pin with Respect to Ground	-0.5 to 5.5	V
Package Power Dissipation	≤ 600	mW
Storage Temperature	-65 to +150	°C
Total SLIC Control pins output current per device Source from VDD : Sink from GND:	 50 50	mA

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	4.75		5.25	V

NOTE: MCLK: 2.048 MHz, 4.096 MHz or 8.192 MHz with tolerance of ± 50 ppm

ELECTRICAL CHARACTERISTICS

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.4	V	DX, TSX, CO, I_L = 14 mA
				0.8	V	All other digital outputs, I_L = 4 mA.
				0.2	V	All digital pins, I_L = 1 mA.
V_{OH}	Output High Voltage	VDD - 0.6			V	DX, CO, I_H = -7 mA. All other digital outputs, I_H = -4 mA.
		VDD - 0.2			V	All digital pins, I_H = -1 mA
I_I	Input Current	-10		10	µA	All digital inputs, GND<V_{IN}<V_{DD}
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Note: The I/O_n and O_n outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{DD1}	Operating Current		25	40	mA	All channels are active.
I_{DD0}	Standby Current		4	6	mA	All channels are powered down, with MCLK present.

Note: Power measurements are made at MCLK = 4.096 MHz, outputs unloaded.

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{FXI}	Input Voltage, VFXI	2.3	2.4	2.55	V	
V_{FRO1}	Output Voltage, VFRO	2.25	2.4	2.6	V	Alternating ±zero μ-law PCM code applied to DR
V_{FRO2}	Output Voltage Swing, VFRO	3.25			Vp-p	RL = 2000 Ω
R_I	Input Resistance, VFXI	2.0			MΩ	0.25 V < VFXI < 4.75 V
R_G	Load Resistance, GSX	10			kΩ	
R_O	Output Resistance VFRO			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR.
R_L	Load Resistance, VFRO	2000			Ω	External loading
I_I	Input Leakage Current, VFXI	-1.0		1.0	μA	0.25 V < VFXI < VDD -0.25 V
I_Z	Output Leakage Current, VFRO	-10		10	μA	Power down
C_G	Load Capacitance, GSX			50	pF	
C_L	Load Capacitance, VFRO			100	pF	External loading
A_V	DC Voltage Gain, VFXI to GSX	5000				
f_U	Unity Gain Bandwidth, VFXI to GSX	1	3		MHz	

TRANSMISSION CHARACTERISTICS

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Absolute Gain

Parameter	Description	Typ	Deviation	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute	0.00	± 0.25	dB	Signal input of 0 dBm0, μ-law or A-law
G_{RA}	Receive Gain, Absolute	-0.15	± 0.25	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0 1020 Hz , RL = 10 kΩ

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	
GT_R	Receive Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, Relative to G_{XA}					
	f = 50 Hz			-40	dB	
	f = 60 Hz			-40	dB	
	f = 300 Hz to 3400 Hz	-0.15		0.15	dB	
	f = 3600 Hz			-0.1	dB	
	f = 4600 Hz and above			-35	dB	
G_{RR}	Receive Gain, Relative to G_{RA}					
	f below 300 Hz			0	dB	
	f = 300 Hz to 3400 Hz	-0.15		0.15	dB	
	f = 3600 Hz			-0.2	dB	
	f = 4600 Hz and above			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XA}	Transmit Delay, Absolute *			340	µs	
D_{XR}	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	µs	
	f = 600 Hz –1000 Hz			150	µs	
	f = 1000 Hz – 2600 Hz			80	µs	
	f = 2600 Hz – 2800 Hz			280	µs	
D_{RA}	Receive Delay, Absolute *			260	µs	
D_{RR}	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	µs	
	f = 600 Hz –1000 Hz			80	µs	
	f = 1000 Hz – 2600 Hz			120	µs	
	f = 2600 Hz – 2800 Hz			150	µs	

Note*: Minimum value in transmit and receive path.

Distortion

Parameter	Description	Min	Typ*	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio					ITU-T O.132
	Input level = 0 dBm0	36			dB	Sine Wave Method (C-message weighted for µ-law; Psophometrically weighted for A-law)
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
STDR	Receive Signal to Total Distortion Ratio					ITU-T O.132
	Input level = 0 dBm0	36			dB	Sine Wave Method (C-message weighted for µ-law; Psophometrically weighted for A-law)
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-50	dBm0	Four Tone Method

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for µ-law			18	dBrnC0	
NXP	Transmit Noise, P Message Weighted for A-law			-68	dBm0p	
NRC	Receive Noise, C Message Weighted for µ-law			12	dBrnC0	
NRP	Receive Noise, P Message Weighted for A-law			-78	dBm0p	
NRS	Noise, Single Frequency			-53	dBm0	VFXI = 0 Vrms, tested at VFRO
	f = 0 kHz – 100 kHz					
PSRX	Power Supply Rejection Transmit					VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
PSRR	Power Supply Rejection Receive					PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
SOS	Spurious Out-of-Band Signals at VFRO Relative to Input PCM code applied:					0 dBm0, 300 Hz – 3400 Hz input
	4600 Hz – 20 kHz			-40	dB	
	20 kHz – 50 kHz			-30	dB	

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VFXI of interfering channel. Idle PCM code into channel under test.
XT_{R-X}	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VFXI = 0 Vrms for channel under test.
XT_{X-X}	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VFXI of interfering channel. VFXI = 0 Vrms for channel under test.
XT_{R-R}	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Note: Crosstalk into the transmit channels (VFXI) can be significantly affected by parasitic capacitive coupling from GSX and VFRO outputs. PCB layouts should be arranged to minimize these parasitics. The resistor value of Rf (from GSX to VFXI) should be kept as low as possible to minimize crosstalk. The limits given above are based on Rf < 200 kΩ.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VFXI. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. VFXI = 0 Vrms.

Note: Crosstalk into the transmit channels (VFXI) can be significantly affected by parasitic capacitive coupling from GSX and VFRO outputs. PCB layouts should be arranged to minimize these parasitics. The resistor value of Rf (from GSX to VFXI) should be kept as low as possible to minimize crosstalk. The limits given above are based on Rf < 200 kΩ.

TIMING CHARACTERISTICS

Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	BCLK Duty Cycle	40		60	%	BCLK = 512 kHz to 8.192 MHz
t2	BCLK Rise and Fall Time			15	ns	BCLK = 512 kHz to 8.192 MHz
t3	MCLK Duty Cycle	40		60	%	MCLK = 2.048 MHz, 4.096 MHz or 8.192 MHz
t4	MCLK Rise and Fall Time			15	ns	MCLK = 2.048 MHz, 4.096 MHz or 8.192 MHz
t5	CCLK Rise and Fall Time			15	ns	CCLK ≤ 8.192 MHz

Transmit

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	Data Enabled Delay Time			25	ns	C_{LOAD} = 100 pF
t12	Data Delay Time from BCLK			25	ns	C_{LOAD} = 100 pF
t13	Data Float Delay Time	3		8	ns	C_{LOAD} = 0 pF
t14	Frame sync Hold Time	25			ns	
t15	Frame sync High Setup Time	25			ns	
t16	$\overline{TSX}$ Enable Delay Time			25	ns	C_{LOAD} = 100 pF
t17	$\overline{TSX}$ Disable Delay Time			25	ns	C_{LOAD} = 100 pF
t21	Receive Data Setup Time	30			ns	
t22	Receive Data Hold Time	15			ns	

Note: Timing parameter t12 is referenced to a high-impedance state.

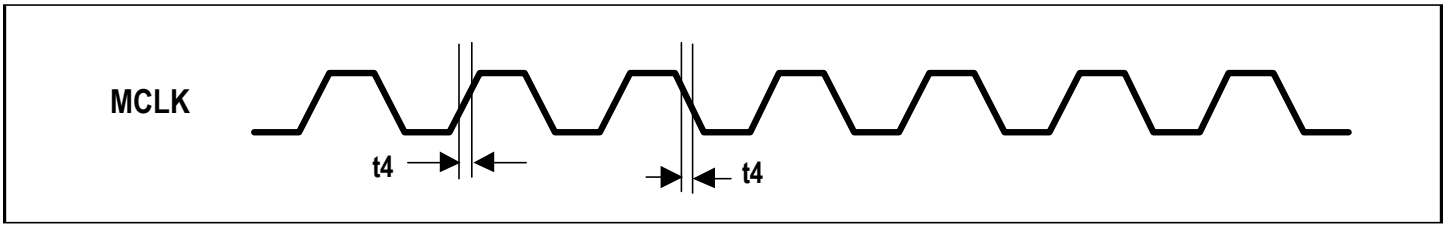


Figure 6. MCLK Timing

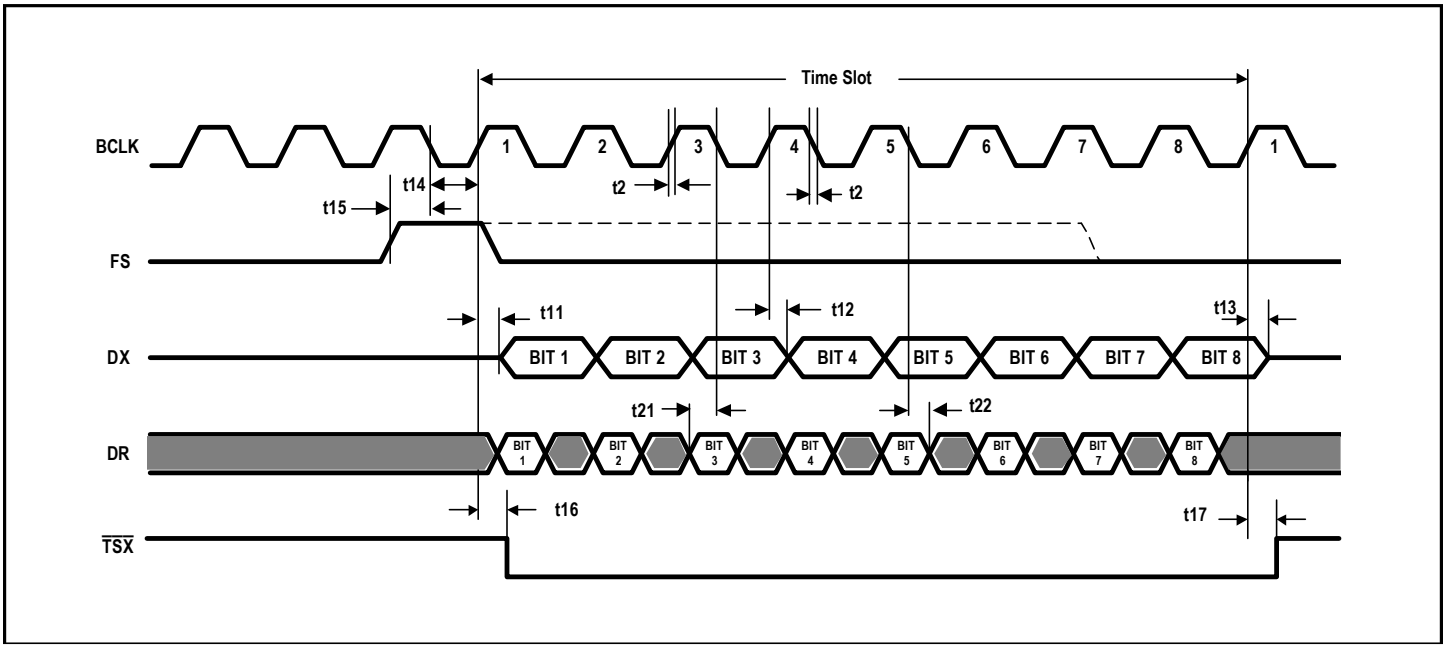


Figure 7. Transmit and Receive Timing in Delay Mode

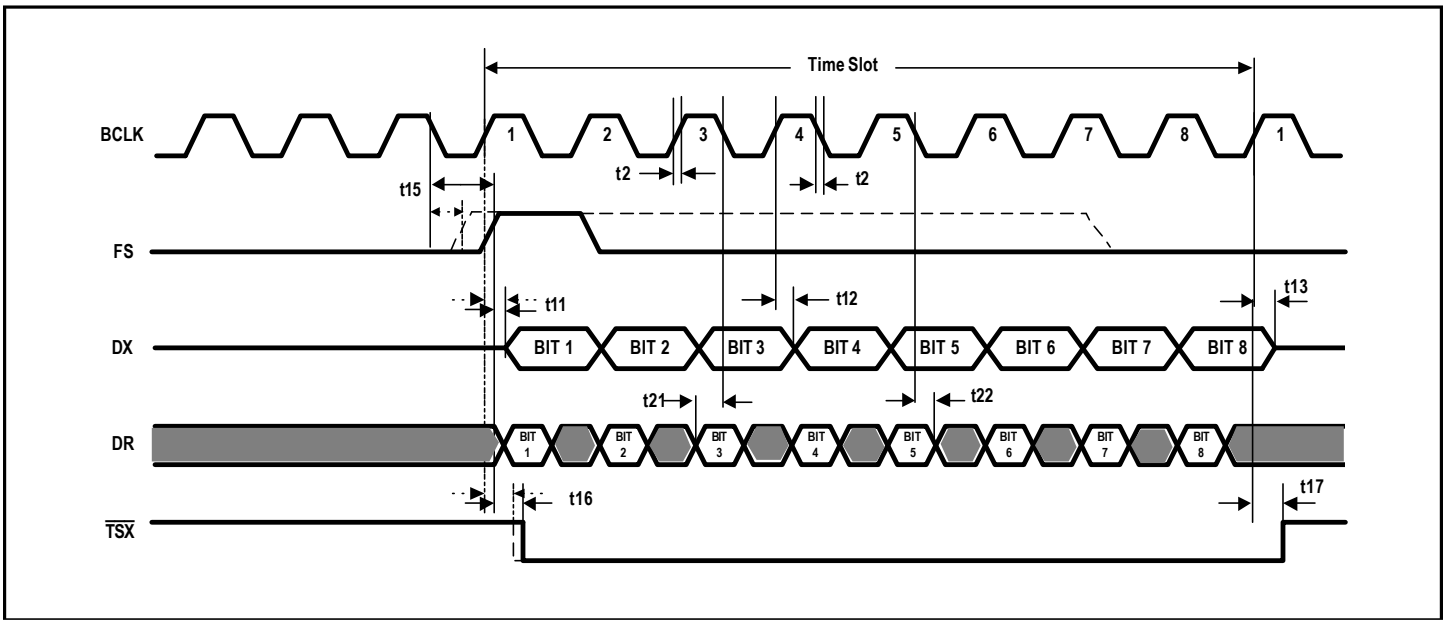


Figure 8. Transmit and Receive Timing in Non-Delay Mode

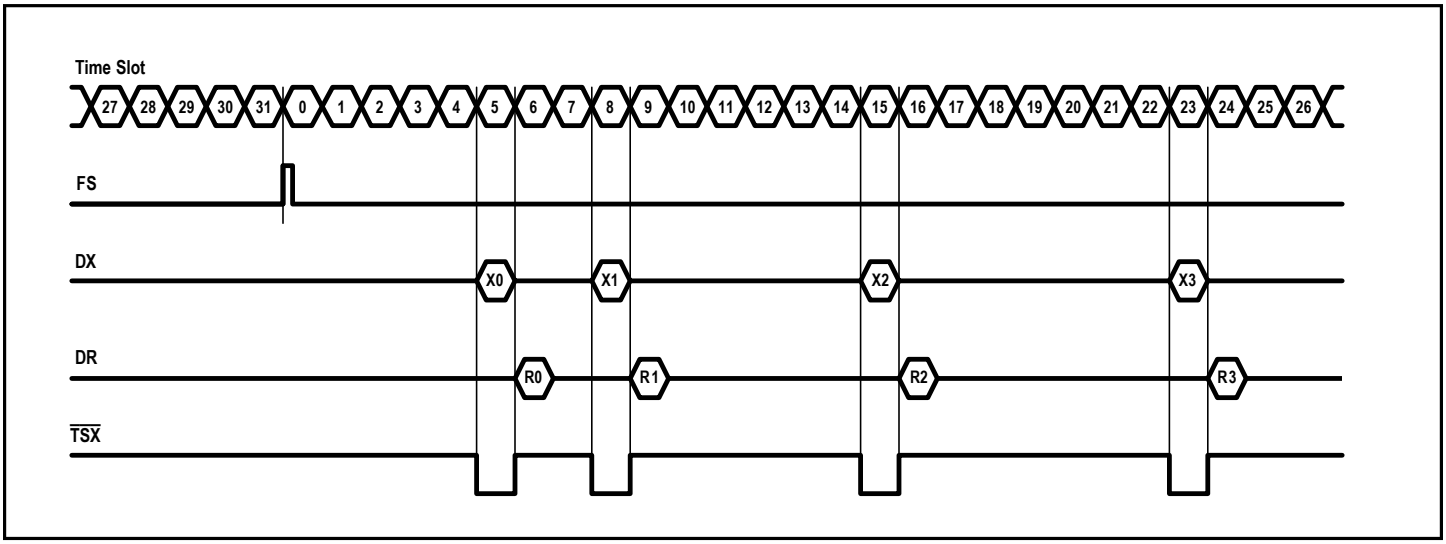


Figure 9. Typical Frame Sync Timing (2 MHz Operation)

Serial Control Interface Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t31	$\overline{CS}$ Hold Time	30			ns	
t32	$\overline{CS}$ Setup Time	30			ns	
t33	$\overline{CS}$ to CO Valid Delay Time			30	ns	
t34	CO Float Delay Time			10	ns	
t35	CI Setup Time	30			ns	
t36	CI Hold Time	30			ns	
t37	$\overline{CS}$ Idle Time	3			cycles of CCLK	
t38	CCLK to CO Valid Delay Time			30	ns	

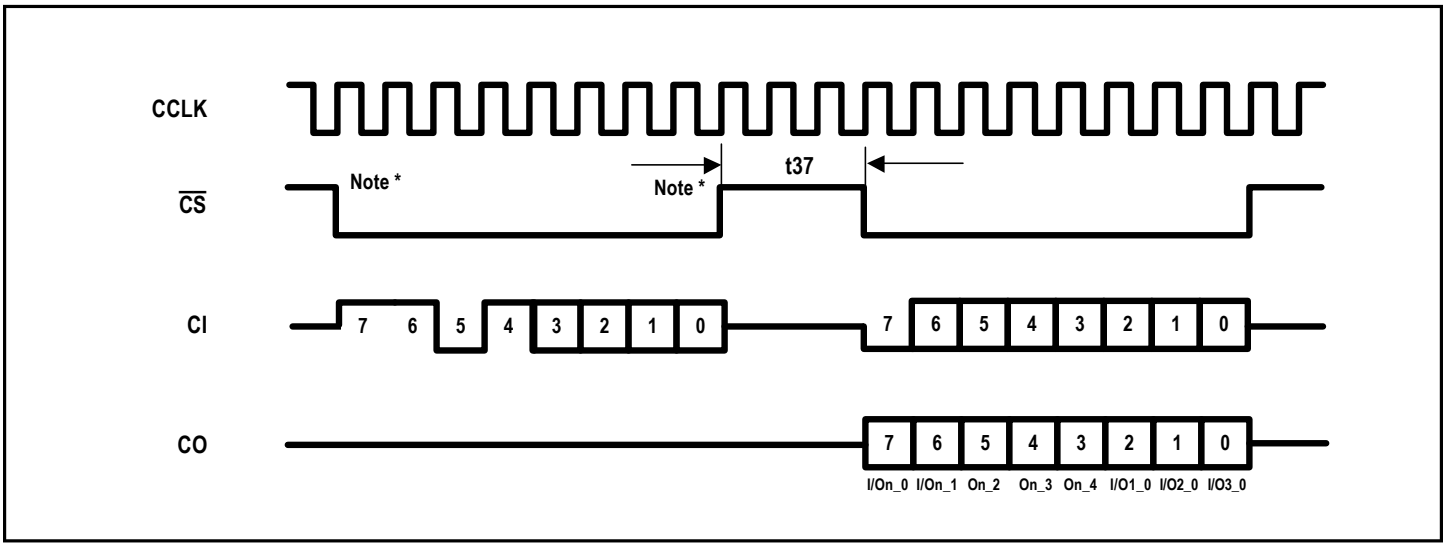


Figure 10. SLIC Programming Mode Timing

Note *: CCLK should have one cycle before $\overline{CS}$ goes low, and two cycles after $\overline{CS}$ goes high.

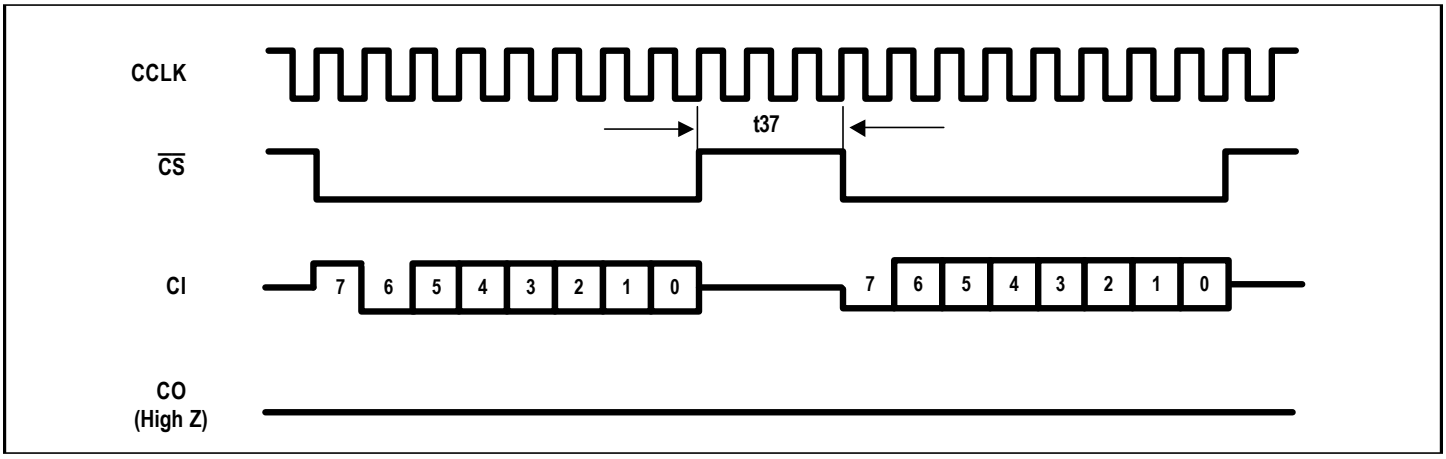


Figure 11. CODEC Programming Mode Timing

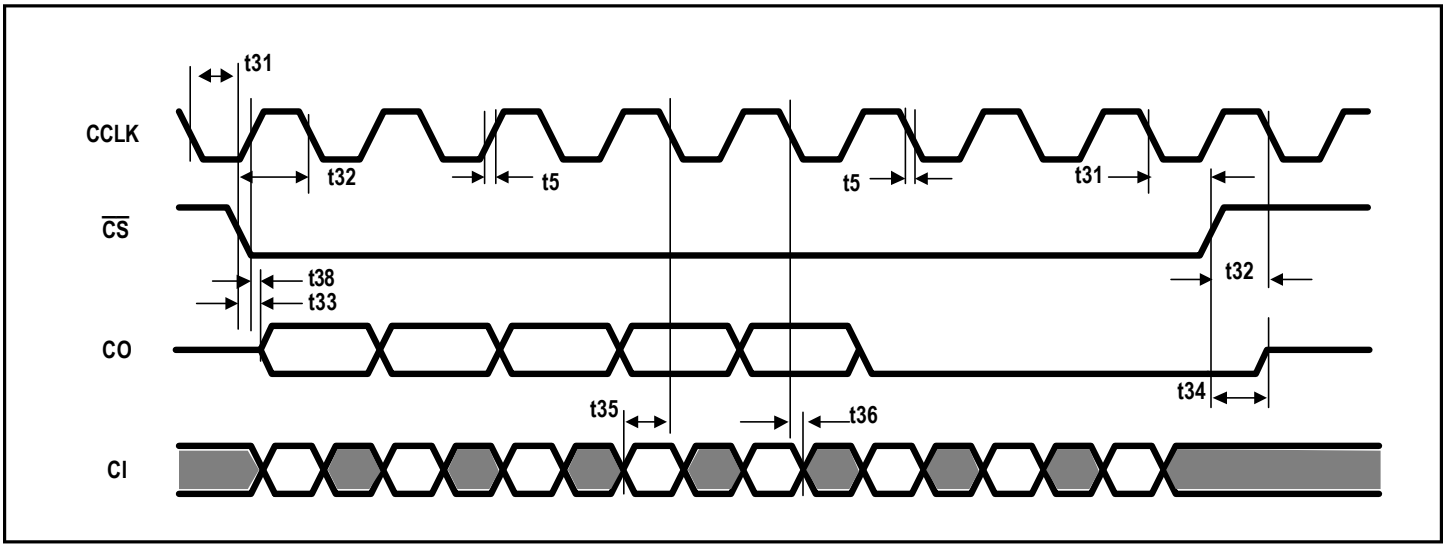


Figure 12. Serial Control Interface Timing

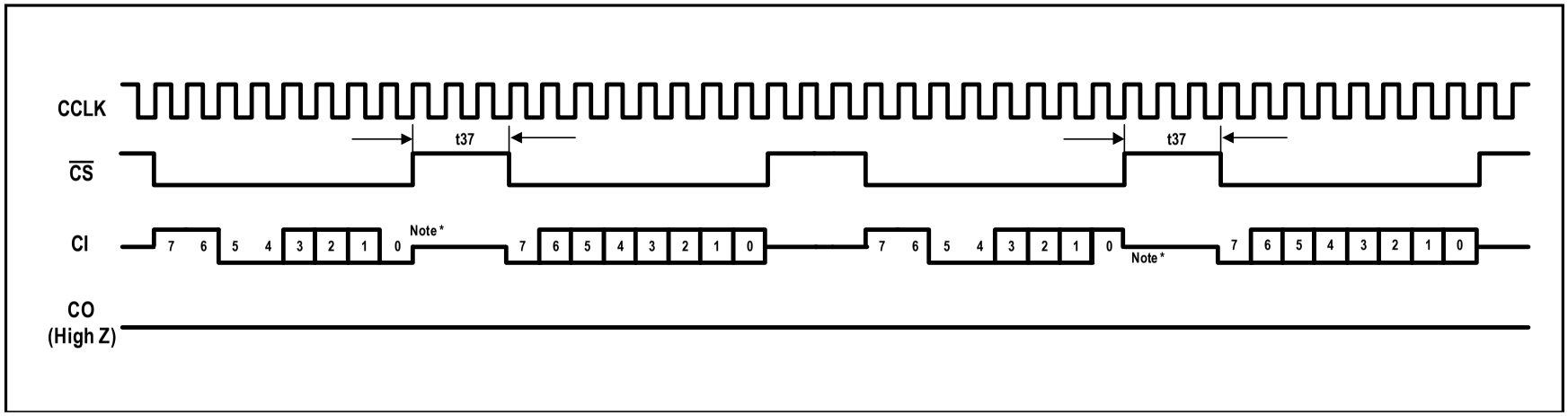


Figure 13. Gain Programming Mode Timing

Note *: Whether MSB GA Register is accessed first or LSB GA Register is accessed can be ignored.

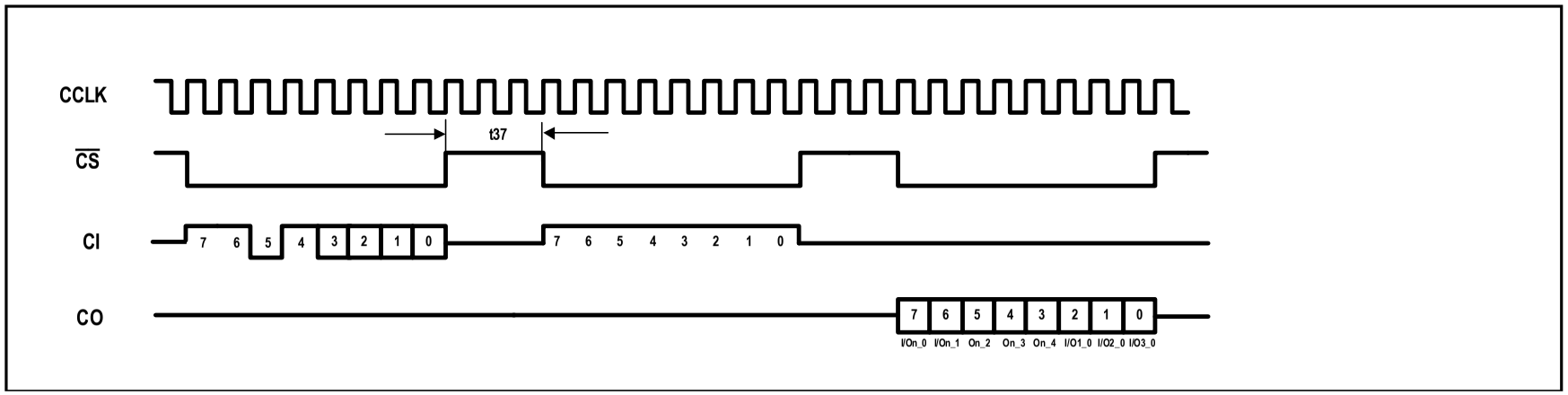
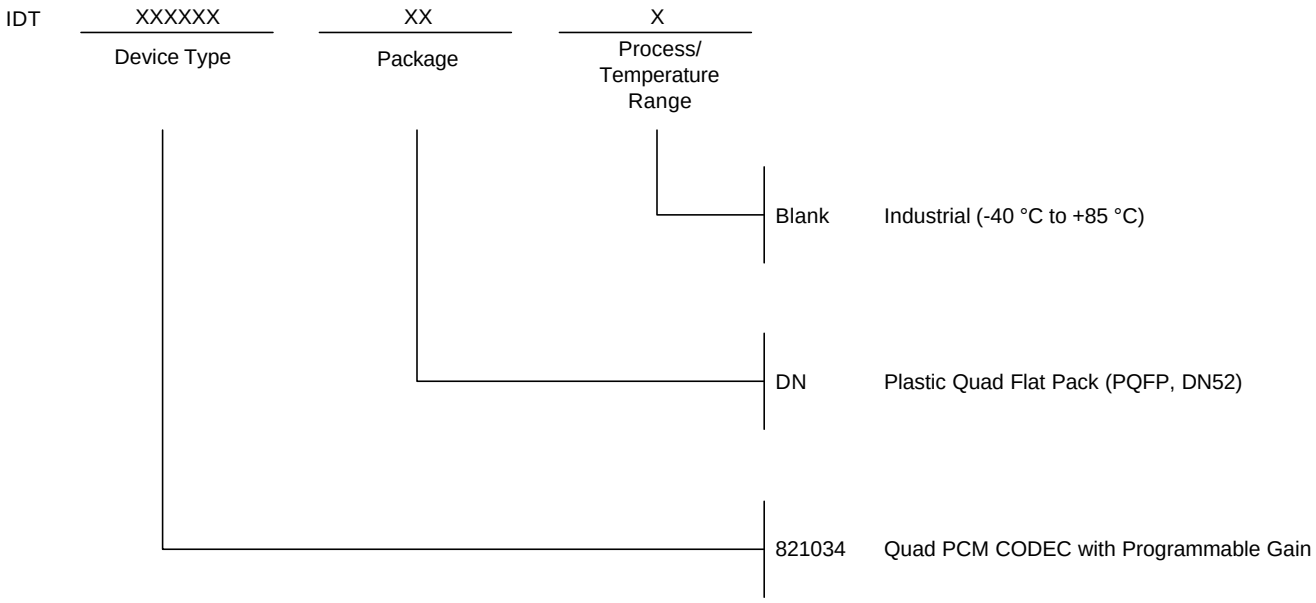


Figure 14. Timing Diagram of the Alternative Method to Read From SLIC Status Register

ORDERING INFORMATION



Data Sheet Document History

01/16/2002	pgs. 1, 4-8, 10
01/08/2003	pgs. 1, 19
05/13/2003	pgs. 2, 5, 8, 15, 16, 18

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