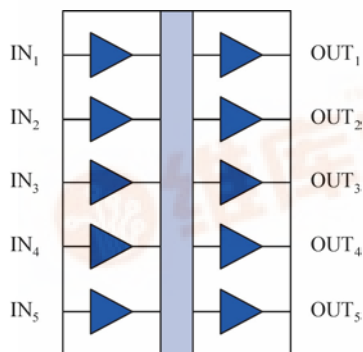
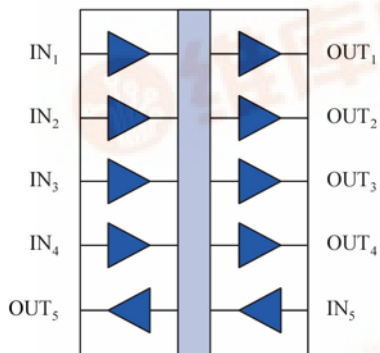


## High Speed Five Channel Digital Couplers

### Functional Diagram



IL260



IL261

### Features

- 3.3 V or 5 V CMOS/TTL Compatible
- 110 Mbps Data Rate
- 2500 V<sub>RMS</sub> Isolation (1 min)
- 2 ns Typical Pulse Width Distortion
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- 30 kV/ms Typical Transient Immunity
- 2 ns Channel to Channel Skew
- 0.3" and 0.15" 16-Pin SOIC Packages
- Extended Temperature Range (-40°C to +85°C)
- UL1577 Approval Pending
- IEC 61010-1 Approval Pending

### Applications

- ADCs and DACs
- Multiplexed Data Transmission
- Data Interfaces
- Board-To-Board Communication
- Digital Noise Reduction
- Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting
- Plasma Displays

### Description

NVE's family of high-speed digital isolators are CMOS devices created by integrating active circuitry and our GMR-based and patented\* IsoLoop® technology. The IL260 and IL261 are five channel versions of the world's fastest digital isolator with a 110 Mbps data rate. This device provides the designer with the most compact isolated logic devices yet available. All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns achieving the best specifications of any isolator device. Typical transient immunity of 30 kV/μs is unsurpassed. High channel density make them ideally suited to isolating multiple ADCs and DACs, parallel buses and peripheral interfaces.

Performance is specified over the temperature range of -40°C to +85°C without any derating.



## Absolute Maximum Ratings

| Parameters                    | Symbol             | Min.                  | Typ. | Max.         | Units | Test Conditions |
|-------------------------------|--------------------|-----------------------|------|--------------|-------|-----------------|
| Storage Temperature           | $T_s$              | -55                   |      | 175          | °C    |                 |
| Ambient Operating Temperature | $T_A$              | -55                   |      | 125          | °C    |                 |
| Supply Voltage                | $V_{DD1}, V_{DD2}$ | -0.5                  |      | 7            | V     |                 |
| Input Voltage                 | $V_I$              | -0.5                  |      | $V_{DD}+0.5$ | V     |                 |
| Output Voltage                | $V_O$              | -0.5                  |      | $V_{DD}+0.5$ | V     |                 |
| Output Current                | $I_O$              | -10                   |      | 10           | mA    | Drive Channel   |
| Lead Solder Temperature       |                    |                       |      | 280          | °C    | 10 s            |
| ESD                           |                    | 2 kV Human Body Model |      |              |       |                 |

## Recommended Operating Conditions

| Parameters                                   | Symbol             | Min. | Typ. | Max.     | Units | Test Conditions     |
|--|--------------------|------|------|----------|-------|---------------------|
| Ambient Operating Temperature <sup>(1)</sup> | $T_A$              | -40  |      | 85       | °C    |                     |
| Supply Voltage                               | $V_{DD1}, V_{DD2}$ | 3.0  |      | 5.5      | V     | 3.3/5.0 V Operation |
| Supply Voltage                               | $V_{DD1}, V_{DD2}$ | 4.5  |      | 5.5      | V     | 5 V Operation       |
| Logic High Input Voltage                     | $V_{IH}$           | 2.4  |      | $V_{DD}$ | mA    |                     |
| Logic Low Input Voltage                      | $V_{IL}$           | 0    |      | 0.8      | V     |                     |
| Minimum Input Signal Rise and Fall Times     | $t_{IR}, t_{IF}$   |      |      | 1        | µsec  |                     |

## Insulation Specifications

| Parameters                       | Symbol | Min.  | Typ.            | Max. | Units             | Test Conditions      |
|----------------------------------|--------|-------|-----------------|------|-------------------|----------------------|
| Creepage Distance (external)     |        |       |                 |      |                   |                      |
| 0.15" SOIC                       |        | 4.026 |                 |      | mm                |                      |
| 0.30" SOIC                       |        | 8.077 |                 |      | mm                |                      |
| Leakage Current <sup>(5)</sup>   |        |       | 0.2             |      | µA <sub>RMS</sub> | 240 V <sub>RMS</sub> |
| Barrier Impedance <sup>(5)</sup> |        |       | $>10^{14}    7$ |      | Ω    pC           |                      |

## Safety & Approvals

### IEC61010-1

TUV Certificate Numbers: *Approval Pending*

### Classification

| Model            | Package          | Pollution Degree | Material Group | Max. Working Voltage |
|------------------|------------------|------------------|----------------|----------------------|
| IL260, IL261     | .30" 16-pin SOIC | II               | III            | 300 V <sub>RMS</sub> |
| IL260-3, IL261-3 | .15" 16-pin SOIC | II               | III            | 150 V <sub>RMS</sub> |

### UL 1577

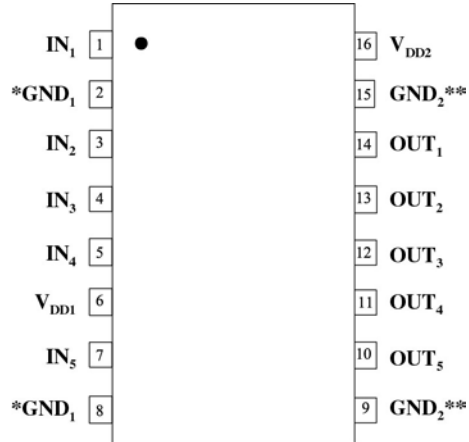
Component Recognition program. File #: *Approval Pending*  
 Rated 2500V<sub>RMS</sub> for 1 minute (SOIC, PDIP), 1000V<sub>RMS</sub> for 1 minute (MSOP)

## Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### IL260 Pin Connections

|    |                  |  |
|----|------------------|--|
| 1  | IN <sub>1</sub>  | Input 1  |
| 2  | GND <sub>1</sub> | Ground <i>Pins 2 and 8 connected internally</i>  |
| 3  | IN <sub>2</sub>  | Input 2  |
| 4  | IN <sub>3</sub>  | Input 3  |
| 5  | IN <sub>4</sub>  | Input 4  |
| 6  | V <sub>DD1</sub> | Supply Voltage 1                                 |
| 7  | IN <sub>5</sub>  | Input 5  |
| 8  | GND <sub>1</sub> | Ground <i>Pins 2 and 8 connected internally</i>  |
| 9  | GND <sub>2</sub> | Ground <i>Pins 9 and 15 connected internally</i> |
| 10 | OUT <sub>5</sub> | Output 5   |
| 11 | OUT <sub>4</sub> | Output 4   |
| 12 | OUT <sub>3</sub> | Output 3   |
| 13 | OUT <sub>2</sub> | Output 2   |
| 14 | OUT <sub>1</sub> | Output 1   |
| 15 | GND <sub>2</sub> | Ground <i>Pins 9 and 15 connected internally</i> |
| 16 | V <sub>DD2</sub> | Supply Voltage 2                                 |

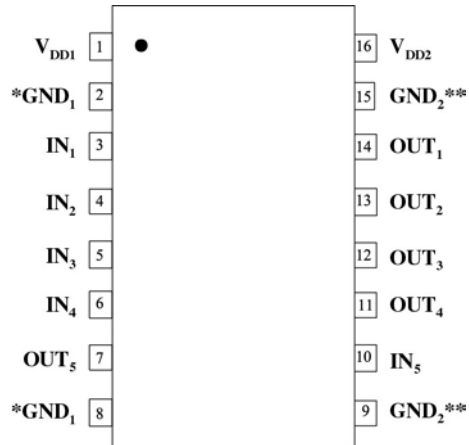


**IL260**

\* Pins 2 and 8 internally connected  
 \*\* Pins 9 and 15 internally connected

### IL260 Pin Connections

|    |                  |  |
|----|------------------|--|
| 1  | V <sub>DD1</sub> | Supply Voltage 1                                 |
| 2  | GND <sub>1</sub> | Ground <i>Pins 2 and 8 connected internally</i>  |
| 3  | IN <sub>1</sub>  | Input 1  |
| 4  | IN <sub>2</sub>  | Input 2  |
| 5  | IN <sub>3</sub>  | Input 3  |
| 6  | IN <sub>4</sub>  | Input 4  |
| 7  | OUT <sub>5</sub> | Output 5   |
| 8  | GND <sub>1</sub> | Ground <i>Pins 2 and 8 connected internally</i>  |
| 9  | GND <sub>2</sub> | Ground <i>Pins 9 and 15 connected internally</i> |
| 10 | IN <sub>5</sub>  | Input 5  |
| 11 | OUT <sub>4</sub> | Output 4   |
| 12 | OUT <sub>3</sub> | Output 3   |
| 13 | OUT <sub>2</sub> | Output 2   |
| 14 | OUT <sub>1</sub> | Output 1   |
| 15 | GND <sub>2</sub> | Ground <i>Pins 9 and 15 connected internally</i> |
| 16 | V <sub>DD2</sub> | Supply Voltage 2                                 |



**IL261**

\* Pins 2 and 8 internally connected  
 \*\* Pins 9 and 15 internally connected

### 3.3 Volt Electrical Specifications

Electrical Specifications are  $T_{min}$  to  $T_{max}$

| Parameters  | Symbol           | Min.                         | Typ.                     | Max.       | Units         | Test Conditions  |
|---|------------------|------------------------------|--------------------------|------------|---------------|--|
| Input Quiescent Current<br>IL260<br>IL261   | $I_{DD1}$        |                              | 30<br>1.5                | 50<br>2.0  | $\mu A$<br>mA |  |
| Output Quiescent Current<br>IL260<br>IL261  | $I_{DD2}$        |                              | 6.5<br>5.5               | 10<br>8    | mA<br>mA      |  |
| Logic Input Current   | $I_i$            | -10                          |                          | 10         | $\mu A$       |  |
| Logic High Output Voltage   | $V_{OH}$         | $V_{DD}-0.1$<br>$0.8*V_{DD}$ | $V_{DD}$<br>$V_{DD}-0.5$ |            | V             | $I_O = -20 \mu A, V_i = V_{IH}$<br>$I_O = -4 \text{ mA}, V_i = V_{IH}$ |
| Logic Low Output Voltage  | $V_{OL}$         |                              | 0<br>0.5                 | 0.1<br>0.8 | V             | $I_O = 20 \mu A, V_i = V_{IL}$<br>$I_O = 4 \text{ mA}, V_i = V_{IL}$   |
| Switching Specifications  |                  |                              |                          |            |               |  |
| Maximum Data Rate   |                  | 100                          | 110                      |            | Mbps          | $C_L = 15 \text{ pF}$  |
| Minimum Pulse Width   | PW               | 10                           |                          |            | ns            | 50% Points, $V_o$  |
| Propagation Delay Input to Output<br>(High to Low)                                | $t_{PHL}$        |                              | 12                       | 18         | ns            | $C_L = 15 \text{ pF}$ ,  |
| Propagation Delay Input to Output<br>(Low to High)                                | $t_{PLH}$        |                              | 12                       | 18         | ns            | $C_L = 15 \text{ pF}$ ,  |
| Pulse Width Distortion $ t_{PHL}-t_{PLH} $ <sup>(2)</sup>                         | PWD              |                              | 2                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Propagation Delay Skew <sup>(3)</sup>   | $t_{PSK}$        |                              | 4                        | 6          | ns            | $C_L = 15 \text{ pF}$  |
| Output Rise Time (10-90%)   | $t_R$            |                              | 2                        | 4          | ns            | $C_L = 15 \text{ pF}$  |
| Output Fall Time (10-90%)   | $t_F$            |                              | 2                        | 4          | ns            | $C_L = 15 \text{ pF}$  |
| Common Mode Transient Immunity<br>(Output Logic High to Logic Low) <sup>(4)</sup> | $ CM_H ,  CM_L $ | 20                           | 30                       |            | kV/ $\mu s$   | $V_{CN} = 300 \text{ V}$   |
| Channel to Channel Skew   |                  |                              | 2                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Dynamic Power Consumption <sup>(6)</sup>  |                  |                              | 200                      | 240        | $\mu A/MHz$   | per channel  |

### 5 Volt Electrical Specifications

Electrical Specifications are  $T_{min}$  to  $T_{max}$

| Parameters   | Symbol           | Min.                         | Typ.                     | Max.       | Units         | Test Conditions  |
|--|------------------|------------------------------|--------------------------|------------|---------------|--|
| Input Quiescent Current<br>IL260<br>IL261                          | $I_{DD1}$        |                              | 30<br>2.5                | 50<br>3.0  | $\mu A$<br>mA |  |
| Output Quiescent Current<br>IL260<br>IL261                         | $I_{DD2}$        |                              | 10<br>8                  | 15<br>12   | mA<br>mA      |  |
| Logic Input Current  | $I_i$            | -10                          |                          | 10         | $\mu A$       |  |
| Logic High Output Voltage  | $V_{OH}$         | $V_{DD}-0.1$<br>$0.8*V_{DD}$ | $V_{DD}$<br>$V_{DD}-0.5$ |            | V             | $I_O = -20 \mu A, V_i = V_{IH}$<br>$I_O = -4 \text{ mA}, V_i = V_{IH}$ |
| Logic Low Output Voltage   | $V_{OL}$         |                              | 0<br>0.5                 | 0.1<br>0.8 | V             | $I_O = 20 \mu A, V_i = V_{IL}$<br>$I_O = 4 \text{ mA}, V_i = V_{IL}$   |
| Switching Specifications   |                  |                              |                          |            |               |  |
| Maximum Data Rate  |                  | 100                          | 110                      |            | Mbps          | $C_L = 15 \text{ pF}$  |
| Minimum Pulse Width  | PW               | 10                           |                          |            | ns            | 50% Points, $V_o$  |
| Propagations Delay Input to Output<br>(High to Low)                | $t_{PHL}$        |                              | 10                       | 15         | ns            | $C_L = 15 \text{ pF}$ ,  |
| Propagations Delay Input to Output<br>(Low to High)                | $t_{PLH}$        |                              | 10                       | 15         | ns            | $C_L = 15 \text{ pF}$ ,  |
| Pulse Width Distortion $ t_{PHL}-t_{PLH} $ <sup>(2)</sup>          | PWD              |                              | 2                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Propagation Delay Skew <sup>(3)</sup>                              | $t_{PSK}$        |                              | 4                        | 6          | ns            | $C_L = 15 \text{ pF}$  |
| Output Rise Time (10-90%)  | $t_R$            |                              | 1                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Output Fall Time (10-90%)  | $t_F$            |                              | 1                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Common Mode Transient Immunity<br>(Output Logic High to Logic Low) | $ CM_H ,  CM_L $ | 20                           | 30                       |            | kV/ $\mu s$   | $V_{CN} = 300 \text{ V}$   |
| Channel to Channel Skew  |                  |                              | 2                        | 3          | ns            | $C_L = 15 \text{ pF}$  |
| Dynamic Power Consumption <sup>(6)</sup>                           |                  |                              | 280                      | 340        | $\mu A/MHz$   | per channel  |

**Notes: (Apply to both 3.3 V and 5 V specifications.)**

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $|t_{\text{PHL}} - t_{\text{PLH}}|$ . %PWD is equal to the PWD divided by the pulse width.
3.  $t_{\text{PSK}}$  is equal to the magnitude of the worst case difference in  $t_{\text{PHL}}$  and/or  $t_{\text{PLH}}$  that will be seen between units at 25°C.
4.  $CM_{\text{H}}$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_{\text{o}} > 0.8 V_{\text{DD}}$ .  $CM_{\text{L}}$  is the maximum common mode input voltage that can be sustained while maintaining  $V_{\text{o}} < 0.8 \text{ V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1-8 shorted and pins 9-16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.

**Application Notes**

**Dynamic Power Consumption**

IsoLoop® devices achieve their low power consumption from the manner by which they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on-state and frequency.

The approximate power supply current per channel for

$$\text{IsoLoop}^\circ \text{ is: } I(\text{input}) = 40 \left( \frac{f}{f_{\text{max}}} \right) \left( \frac{1}{4} \right) \text{ mA}$$

where f = operating frequency  
 fmax = 50 MHz

**Power Supply Decoupling**

Both power supplies to these devices must be decoupled with low ESR 100 nF ceramic capacitors. For data rates in excess of 10MBd, use of ground planes for both GND1 and GND2 is highly recommended. Capacitors should be located as close as possible to the device.

**Signal Status on Start-up and Shut Down**

To minimize power dissipation, the input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start-up circuit. Initialization consists of toggling each channel either high then low or low then high, depending on the desired state.

**Data Transmission Rates**

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in ns. It may also be expressed as a percentage:

$$\text{PWD}\% = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example: For data rates of 12.5 Mb

$$\text{PWD}\% = \frac{3 \text{ ns}}{80 \text{ ns}} \times 100\% = 3.75\%$$

This figure is almost three times better than for any available optocoupler with the same temperature range, and two times better than any optocoupler regardless of published temperature range. The IsoLoop® range of isolators will run at almost 35 Mb before reaching the 10% limit.

Propagation delay skew is the difference in time taken for two or more channels to propagate their signals. This becomes significant when clocking is involved since it is undesirable for the clock pulse to arrive before the data has settled. A short propagation delay skew is therefore critical, especially in high data rate parallel systems, to establish and maintain accuracy and repeatability. The IsoLoop® range of isolators all have a maximum propagation delay skew of 6 ns, which is five times better than any optocoupler. The maximum channel-to-channel skew in the IsoLoop® coupler is only 3 ns which is ten times better than any optocoupler.

**Application Diagrams**

**Figure 1 Single Channel  $\Delta\Sigma$**

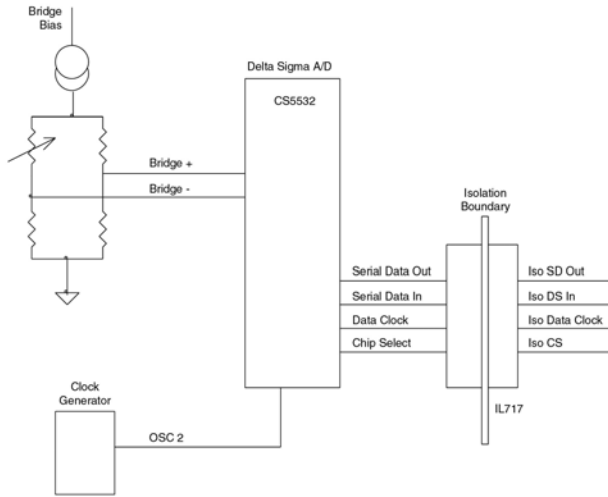
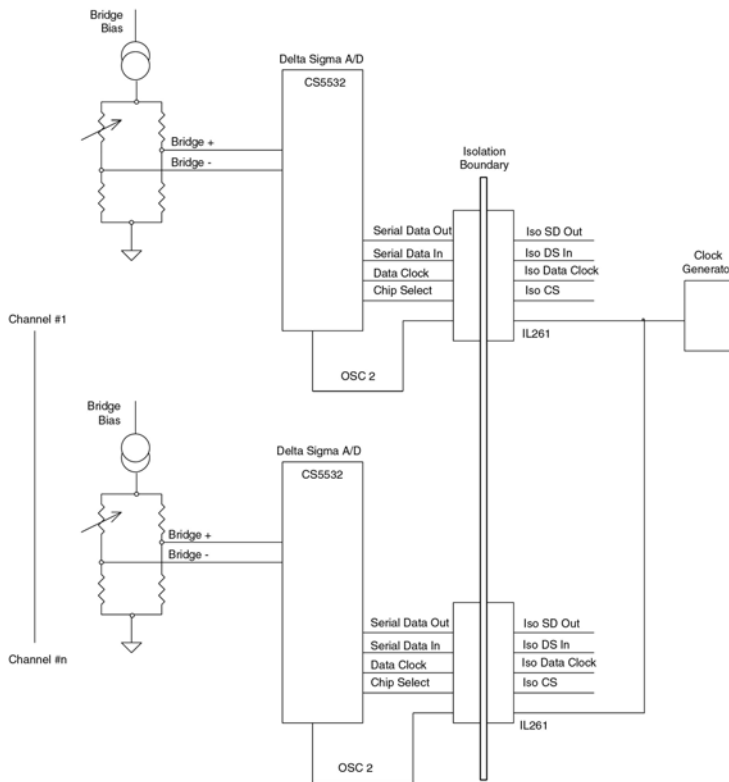


Figure 1 shows a typical single channel  $\Delta\Sigma$  ADC application. The A/D is located on the bridge with no signal conditioning electronics between the bridge sensor and the ADC. In this application, the IL717 is the best choice for isolation. It isolates the control bus from the microcontroller. The system clock is located on the isolated side of the system.

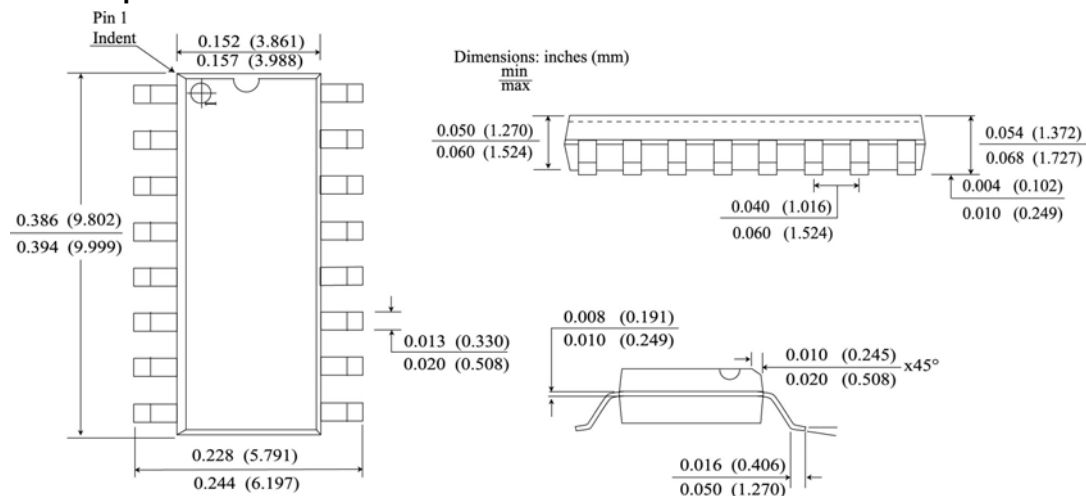
**Figure 2 Multi Channel  $\Delta\Sigma$**



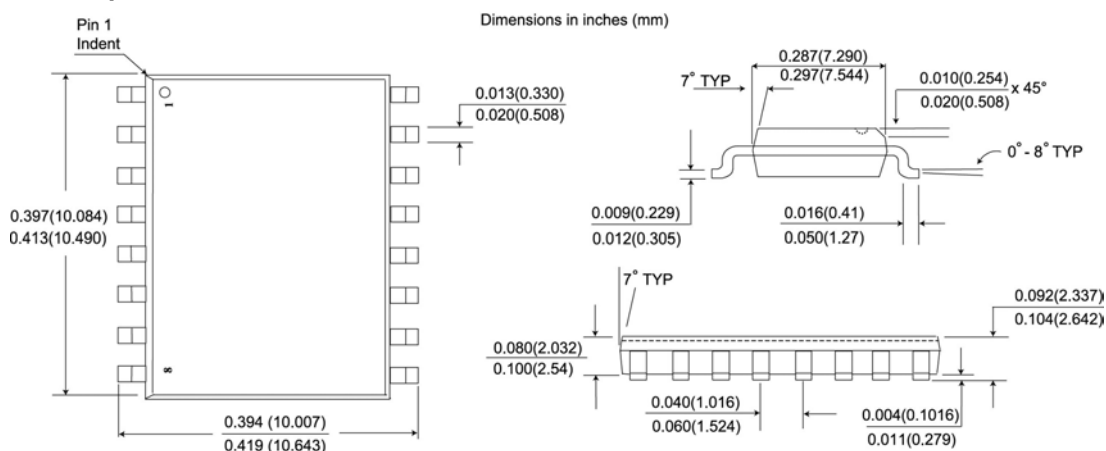
The second  $\Delta\Sigma$  application is where multiple ADC's are configured in a channel-to-channel isolation configuration. The problem for designers is how to control clock jitter and edge placement accuracy of the system clock for each ADC. The best solution is to use a single clock on the system side and distribute this to each ADC. The IL261 adds a 5th channel to the IL717. This 5th channel is used to distribute a single, isolated clock to multiple ADC's as shown in Figure 2.

**Package drawings, dimensions and specifications**

**0.15" 16-pin SOIC**



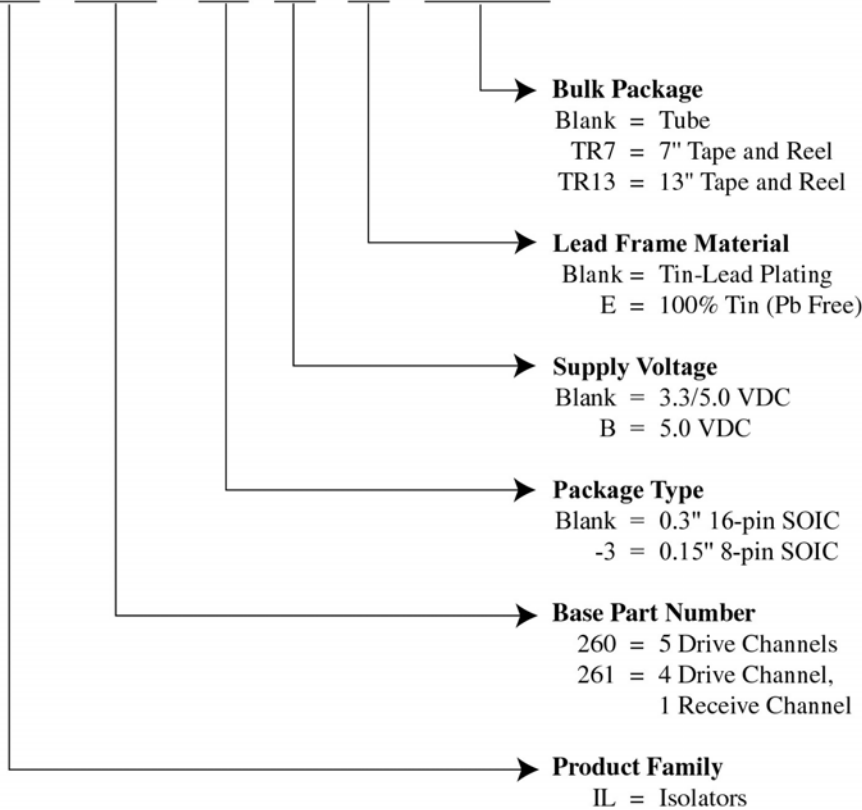
**0.3" 16-pin SOIC**





**Ordering information and valid part numbers.**

**IL 260 -3 B E TR13**



**IL260 Valid Part Numbers**

IL260  
 IL260B  
 IL260E  
 IL260BE  
 IL260ETR13  
 IL260BETR13  
 IL260TR13  
 IL260BTR13  
  
 IL260-3  
 IL260-3B  
 IL260-3E  
 IL260-3BE  
 IL260-3TR7  
 IL260-3BTR7  
 IL260-3TR13  
 IL260-3BTR13  
 IL260-3BETR7  
 IL260-3ETR7  
 IL260-3BETR13  
 IL260-3ETR13

**IL261 Valid Part Numbers**

IL261  
 IL261B  
 IL261E  
 IL261BE  
 IL261ETR13  
 IL261BETR13  
 IL261TR13  
 IL261BTR13  
  
 IL261-3  
 IL261-3B  
 IL261-3E  
 IL261-3BE  
 IL261-3TR7  
 IL261-3BTR7  
 IL261-3TR13  
 IL261-3BTR13  
 IL261-3BETR7  
 IL261-3ETR7  
 IL261-3BETR13  
 IL261-3ETR13

## **About NVE**

An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine leading edge Giant Magnetoresistive (GMR) materials with integrated circuits to make high performance electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at [www.nve.com](http://www.nve.com) or call 952-829-9217 for information on products, sales or distribution.

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ISB-DS-001-IL260/1-A

January 17, 2005