查询INA333AIDRGT供应商 捷多邦，专业PCB打样工厂，24小时加急出货

Micro-Power (50μA), Zerø-Drift, Rail-to-Rail Out Instrumentation Amplifier

FEATURES

- LOW OFFSET VOLTAGE: 25μV (max), G ≥ 100
- LOW DRIFT: 0.1μV/°C, G ≥ 100
- LOW NOISE: 50nV/√Hz, G ≥ 100
- HIGH CMRR: 100dB (min), G ≥ 10
- LOW INPUT BIAS CURRENT: 200pA (max)
- SUPPLY RANGE: +1.8V to +5.5V
- INPUT VOLTAGE: (V–) +0.1V to (V+) –0.1V
- OUTPUT RANGE: (V–) +0.05V to (V+) –0.05V
- LOW QUIESCENT CURRENT: 50μA
- OPERATING TEMPERATURE: –40°C to +125°C
- RFI FILTERED INPUTS
- MSOP-8 AND DFN-8 PACKAGES

APPLICATIONS

- BRIDGE AMPLIFIERS
- ECG AMPLIFIERS
- PRESSURE SENSORS
- MEDICAL INSTRUMENTATION
- PORTABLE INSTRUMENTATION
- WEIGH SCALES
- THERMOCOUPLE AMPLIFIERS
- RTD SENSOR AMPLIFIERS
- DATA ACQUISITION

DESCRIPTION

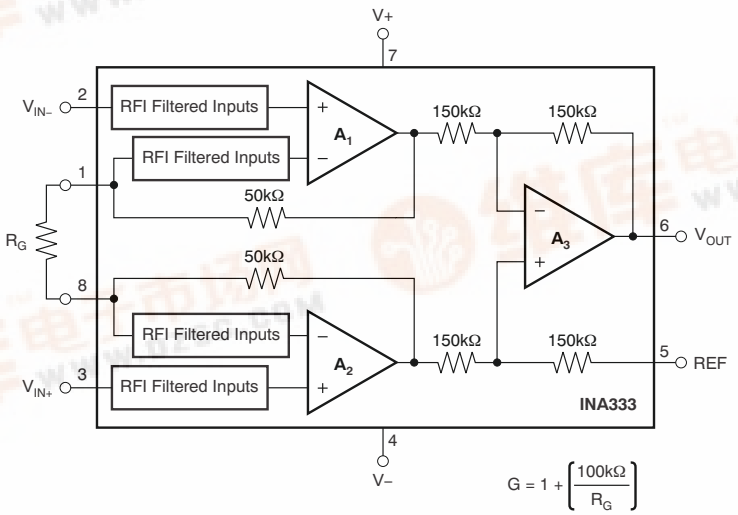
The INA333 is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile 3-op amp design, small size, and low power make it ideal for a wide range of portable applications.

A single external resistor sets any gain from 1 to 1000. The INA333 is designed to use an industry-standard gain equation: $G = 1 + (100k\Omega/R_G)$.

The INA333 provides very low offset voltage (25μV, G ≥ 100), excellent offset voltage drift (0.1μV/°C, G ≥ 100), and high common-mode rejection (100dB at G ≥ 10). It operates with power supplies as low as 1.8V (±0.9V), and quiescent current is only 50μA—ideal for battery-operated systems. Using autocalibration techniques to ensure excellent precision over the extended industrial temperature range, the INA333 also offers exceptionally low noise density (50nV/√Hz) that extends down to dc.

The INA333 is available in both MSOP-8 and DFN-8 surface-mount packages and is specified over the T_A = –40°C to +125°C temperature range.

Sample Request
Click Here



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Products conform to specifications per the terms of the Texas

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA333	MSOP-8	DGK	I333
	DFN-8(2)	DRG	I333A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Available Q4, 2008.

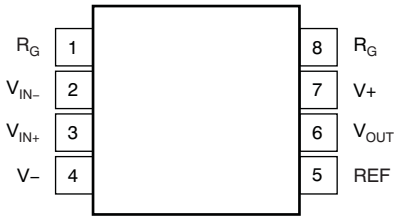
ABSOLUTE MAXIMUM RATINGS(1)

		INA333	UNIT
Supply voltage		+7	V
Analog input voltage range(2)		(V–) – 0.3 to (V+) + 0.3	V
Output short-circuit(3)		Continuous	
Operating temperature range, T_A		–40 to +150	°C
Storage temperature range, T_A		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

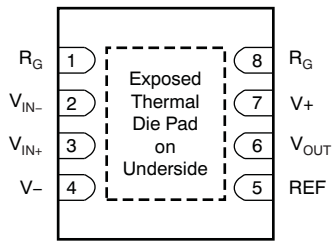
PIN CONFIGURATIONS

DGK PACKAGE
MSOP-8
(TOP VIEW)



INA333

DRG PACKAGE
DFN-8
(TOP VIEW)



INA333

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ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA333 MIN	INA333 TYP	INA333 MAX	UNIT
INPUT(1)						
Offset voltage, RTI(2)	V_{OSI}			±10 ±25/G	±25 ±75/G	µV
vs Temperature					**±0.1 ±0.5/G**	**µV/°C**
vs Power supply	PSR	1.8V ≤ V_S ≤ 5.5V		±1 ±5/G	±5 ±15/G	µV/V
Long-term stability				See note (3)		
Turn-on time to specified V_{OSI}				See Typical characteristics		
Impedance						
Differential	Z_{IN}			100 || 3		GΩ || pF
Common-mode	Z_{IN}			100 || 3		GΩ || pF
Common-mode voltage range	V_{CM}	V_O = 0V	(V–) + 0.1		(V+) – 0.1	V
Common-mode rejection	CMR	DC to 60Hz				
G = 1		V_{CM} = (V–) + 0.1V to (V+) – 0.1V	80	90		dB
G = 10		V_{CM} = (V–) + 0.1V to (V+) – 0.1V	100	110		dB
G = 100		V_{CM} = (V–) + 0.1V to (V+) – 0.1V	100	115		dB
G = 1000		V_{CM} = (V–) + 0.1V to (V+) – 0.1V	100	115		dB
INPUT BIAS CURRENT						
Input bias current	I_B			±70	±200	pA
vs Temperature			**See Typical Characteristic curve**			**pA/°C**
Input offset current	I_{OS}			±50	±200	pA
vs Temperature			**See Typical Characteristic curve**			**pA/°C**
INPUT VOLTAGE NOISE						
Input voltage noise	e_{NI}	G = 100, R_S = 0Ω				
f = 10Hz				50		nV/√Hz
f = 100Hz				50		nV/√Hz
f = 1kHz				50		nV/√Hz
f = 0.1Hz to 10Hz				1		$µV_{PP}$
Input current noise	i_N					
f = 10Hz				100		fA/√Hz
f = 0.1Hz to 10Hz				2		pA_{PP}
GAIN						
Gain equation	G			1 + (100kΩ/R_G)		V/V
Range of gain			1		1000	V/V
Gain error		V_S = 5.5V, (V–) + 100mV ≤ V_O ≤ (V+) – 100mV				
G = 1				±0.01	±0.1	%
G = 10				±0.05	±0.25	%
G = 100				±0.07	±0.25	%
G = 1000				±0.25	±0.5	%

(1) Total V_{OS}, Referred-to-input = (V_{OSI}) + (V_{OSO}/G).
(2) RTI = Referred-to-input.
(3) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1µV.

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ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA333 MIN	INA333 TYP	INA333 MAX	UNIT
GAIN (continued)						
Gain vs Temperature						
G = 1				**±1**	**±5**	**ppm/°C**
G > 1(4)				**±15**	**±50**	**ppm/°C**
Gain nonlinearity		V_S = 5.5V, (V–) + 100mV ≤ V_O ≤ (V+) – 100mV				
G = 1 to 1000		R_L = 10kΩ		10		ppm
OUTPUT						
Output voltage swing from rail(5)		V_S = 5.5V, R_L = 10kΩ		See note (5)	50	mV
Capacitive load drive				500		pF
Short-circuit current	I_{SC}	Continuous to common		–40, +5		mA
FREQUENCY RESPONSE						
Bandwidth, –3dB						
G = 1				150		kHz
G = 10				35		kHz
G = 100				3.5		kHz
G = 1000				350		Hz
Slew rate	SR	V_S = 5V, V_O = 4V Step				
G = 1				0.16		V/µs
G = 100				0.05		V/µs
Settling time to 0.01%	t_S					
G = 1		V_{STEP} = 4V		50		µs
G = 100		V_{STEP} = 4V		400		µs
Settling time to 0.001%	t_S					
G = 1		V_{STEP} = 4V		60		µs
G = 100		V_{STEP} = 4V		500		µs
Overload recovery		50% overdrive		75		µs
REFERENCE INPUT						
R_{IN}				300		kΩ
Voltage range			V–		V+	V
POWER SUPPLY						
Voltage range						
Single			+1.8		+5.5	V
Dual			±0.9		±2.75	V
Quiescent current	I_Q	V_{IN} = V_S/2		50	75	µA
vs Temperature					**80**	**µA**
TEMPERATURE RANGE						
Specified temperature range			–40		+125	°C
Operating temperature range			–40		+150	°C
Thermal resistance	θ_{JA}					
MSOP				100		°C/W
DFN				65		°C/W

(4) Does not include effects of external resistor R_G.
(5) See Typical Characteristics curve, *Output Voltage Swing vs Output Current* (Figure 29).

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TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

INPUT OFFSET VOLTAGE

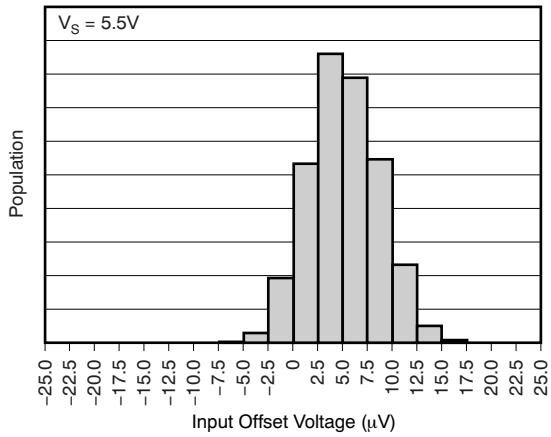

Figure 1.

INPUT VOLTAGE OFFSET DRIFT (–40°C to +125°C)

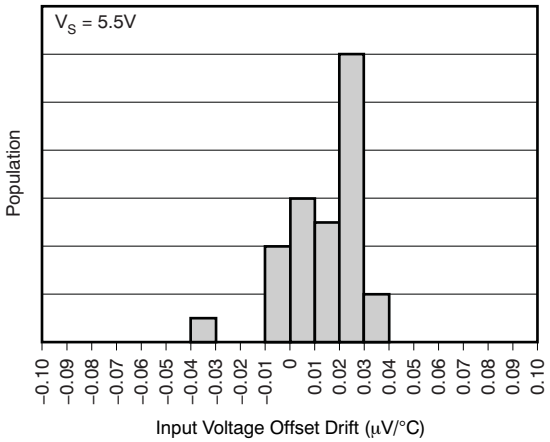

Figure 2.

OUTPUT OFFSET VOLTAGE

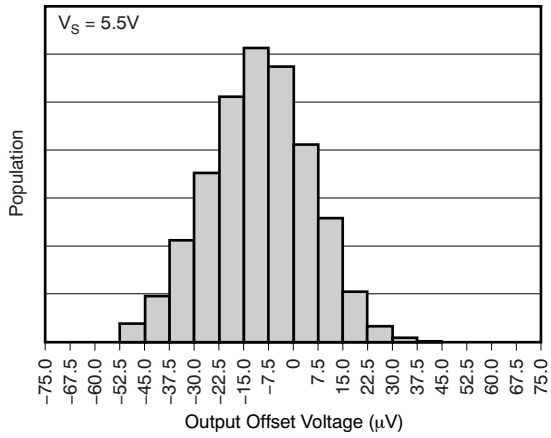

Figure 3.

OUTPUT VOLTAGE OFFSET DRIFT (–40°C to +125°C)

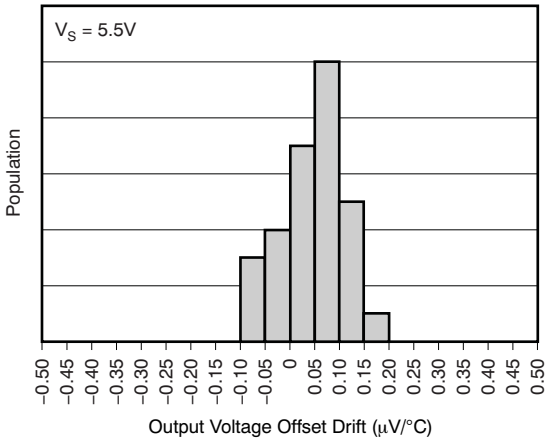

Figure 4.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

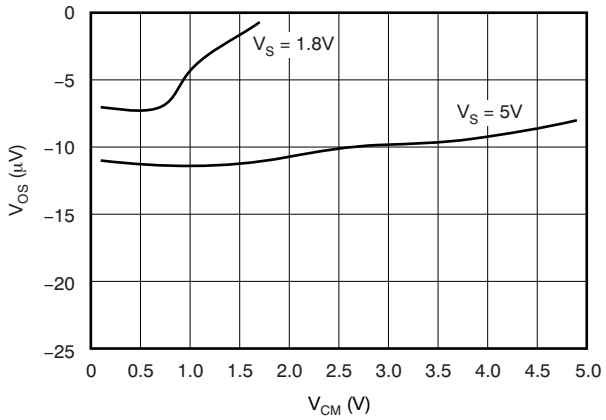

Figure 5.

0.1Hz TO 10Hz NOISE

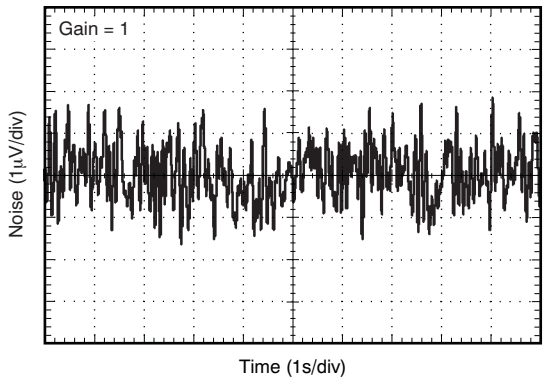

Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

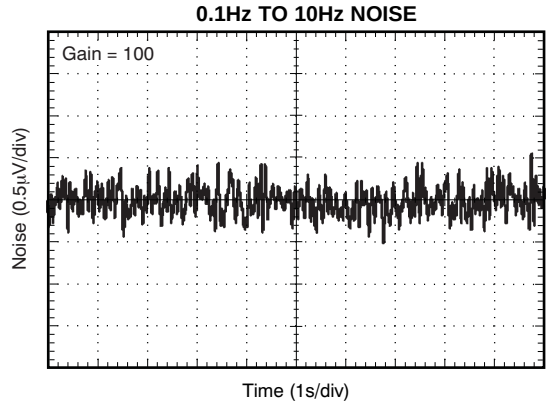

Figure 7.

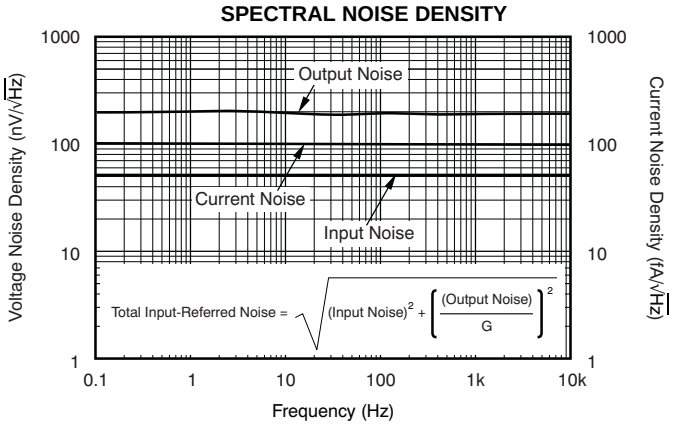

Figure 8.

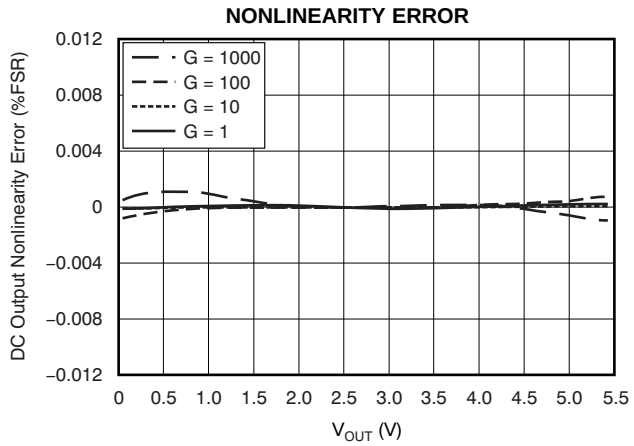

Figure 9.

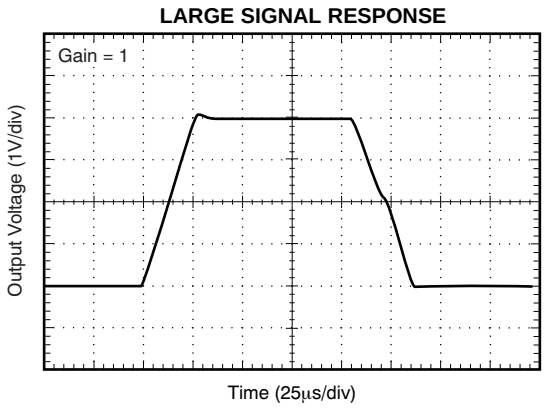

Figure 10.

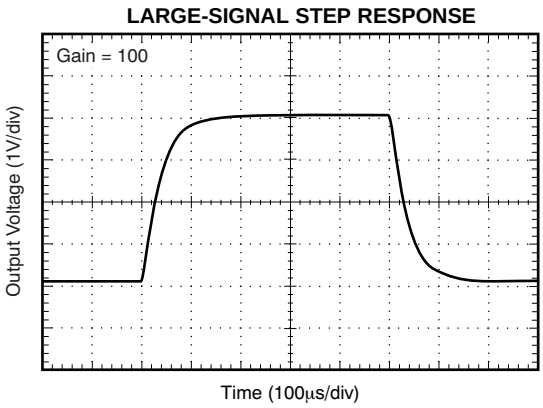

Figure 11.

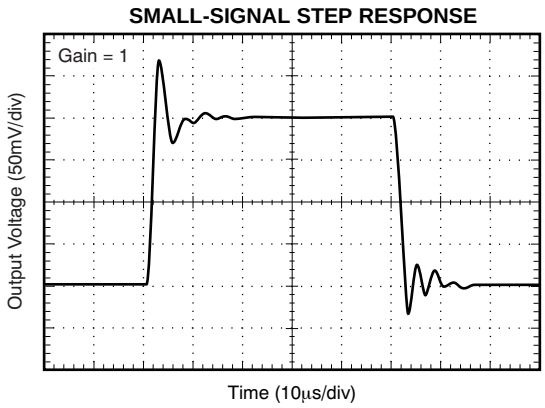

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE

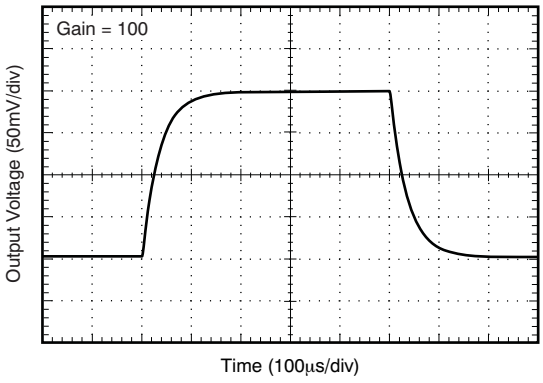

Figure 13.

SETTLING TIME vs GAIN

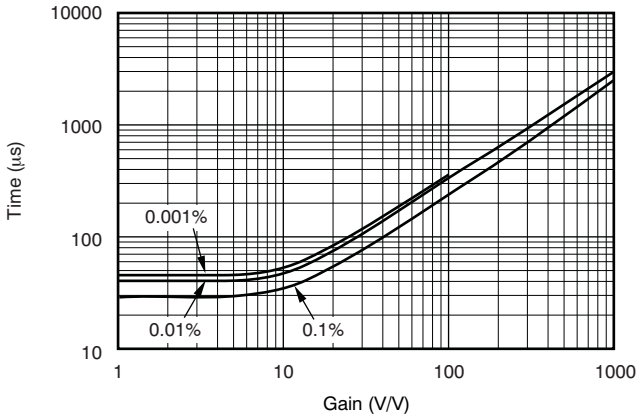

Figure 14.

STARTUP SETTLING TIME

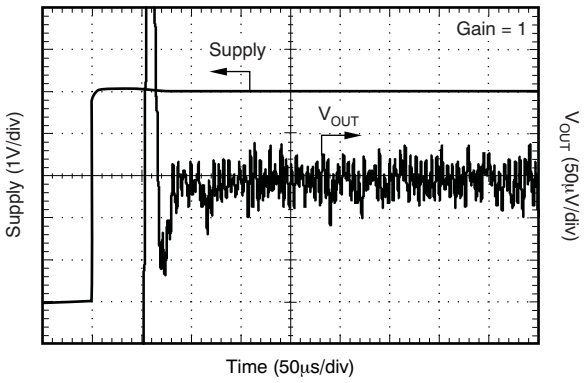

Figure 15.

GAIN vs FREQUENCY

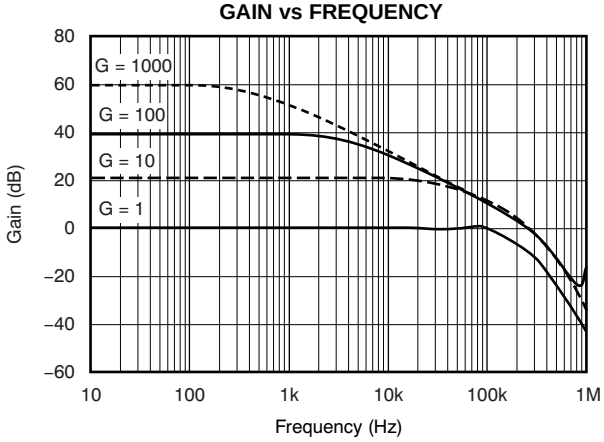

Figure 16.

COMMON-MODE REJECTION RATIO

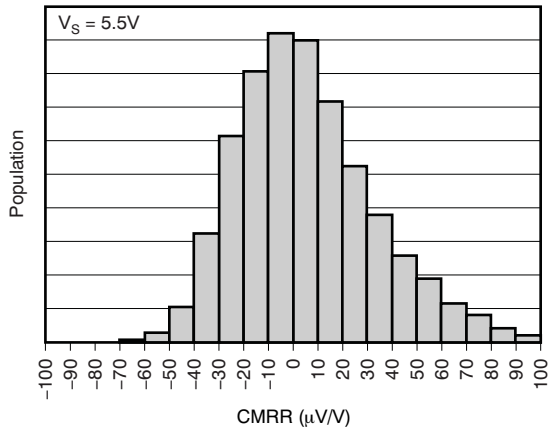

Figure 17.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

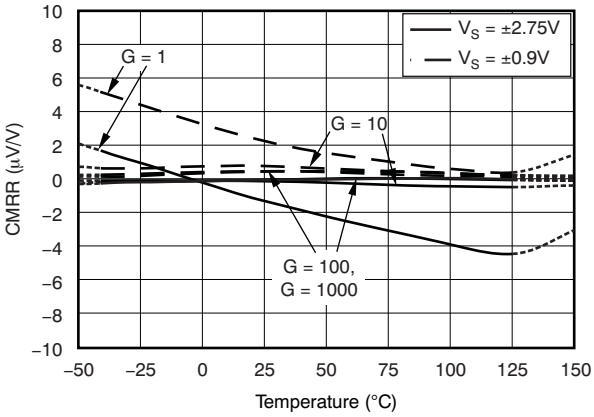

Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs FREQUENCY

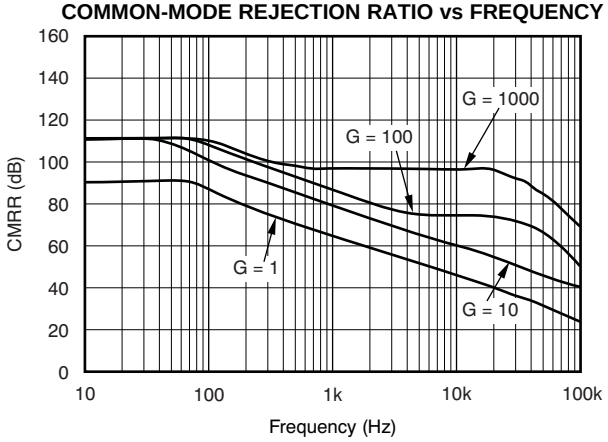

Figure 19.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

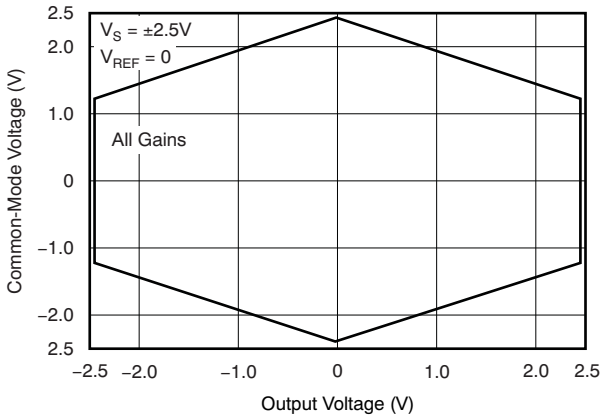

Figure 20.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

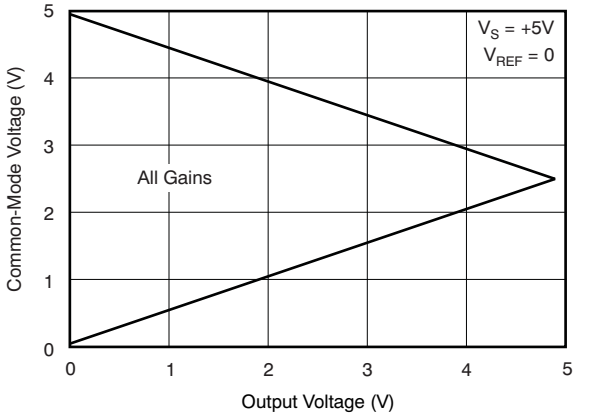

Figure 21.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

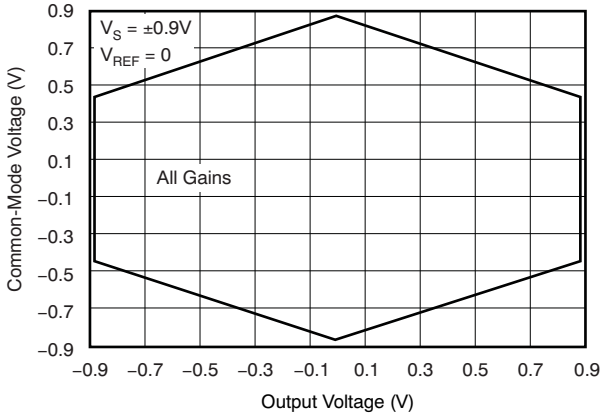

Figure 22.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

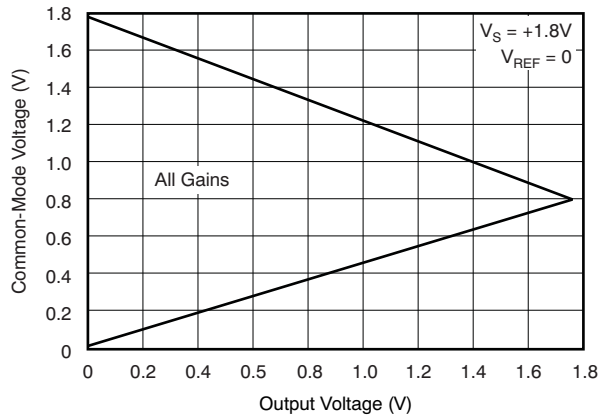

Figure 23.

POSITIVE POWER-SUPPLY REJECTION RATIO

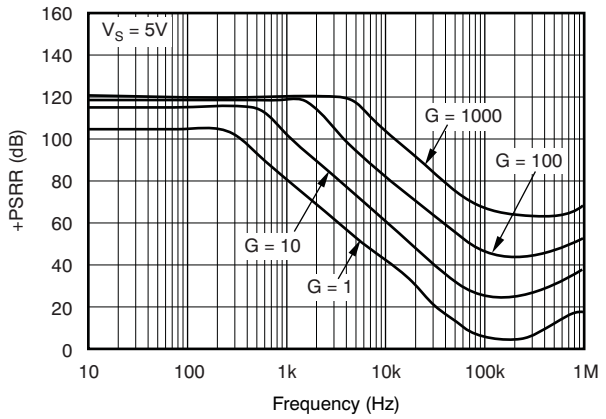

Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

NEGATIVE POWER-SUPPLY REJECTION RATIO

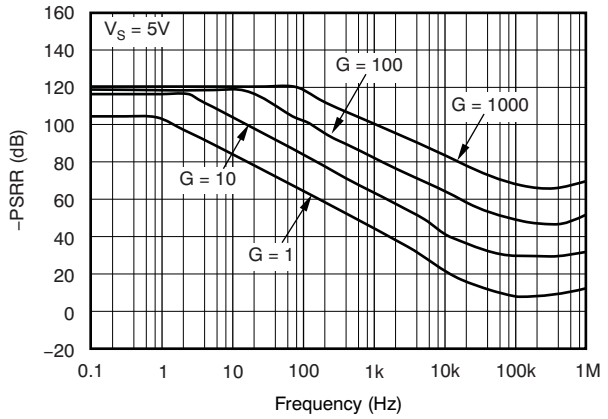

Figure 25.

INPUT BIAS CURRENT vs TEMPERATURE

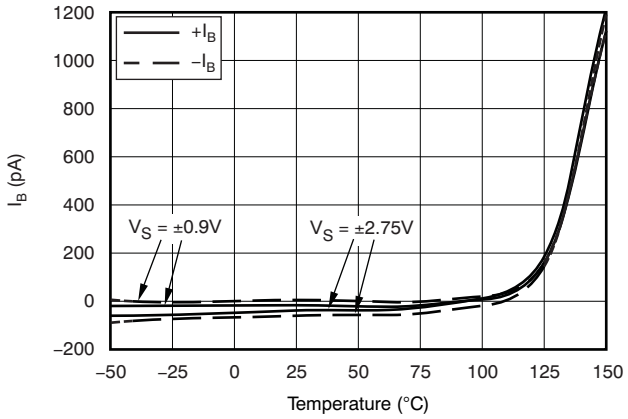

Figure 26.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

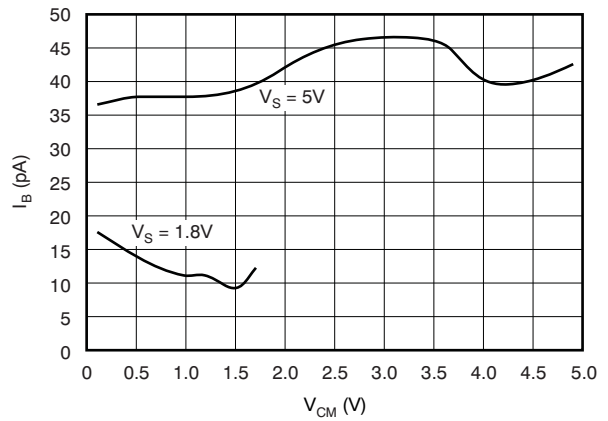

Figure 27.

INPUT OFFSET CURRENT vs TEMPERATURE

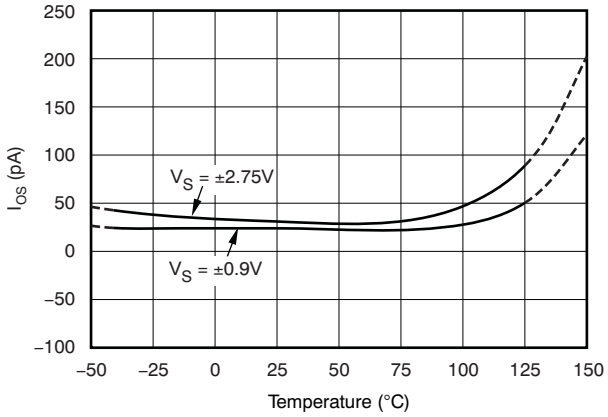

Figure 28.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

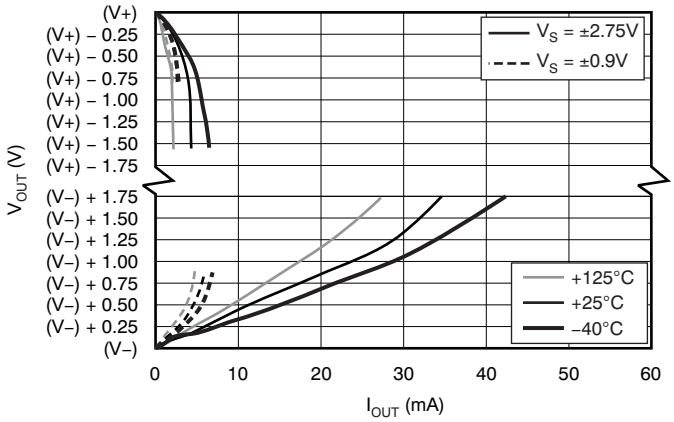

Figure 29.

QUIESCENT CURRENT vs TEMPERATURE

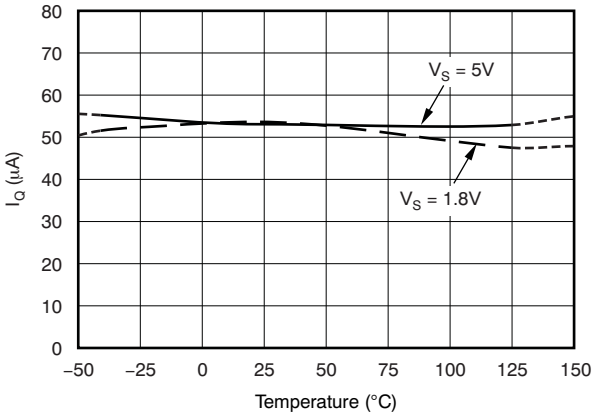

Figure 30.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = 0, and G = 1, unless otherwise noted.

QUIESCENT CURRENT vs COMMON-MODE VOLTAGE

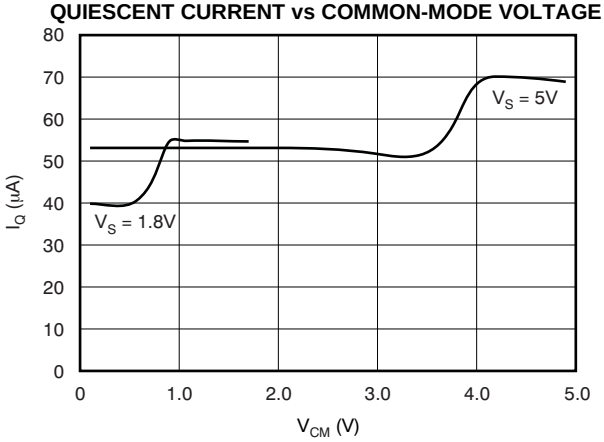

Figure 31.

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APPLICATION INFORMATION

Figure 32 shows the basic connections required for operation of the INA333. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 15Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

SETTING THE GAIN

Gain of the INA333 is set by a single external resistor, R_G, connected between pins 1 and 8. The value of R_G is selected according to Equation 1:

$$G = 1 + (100k\Omega/R_G) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 100kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency.

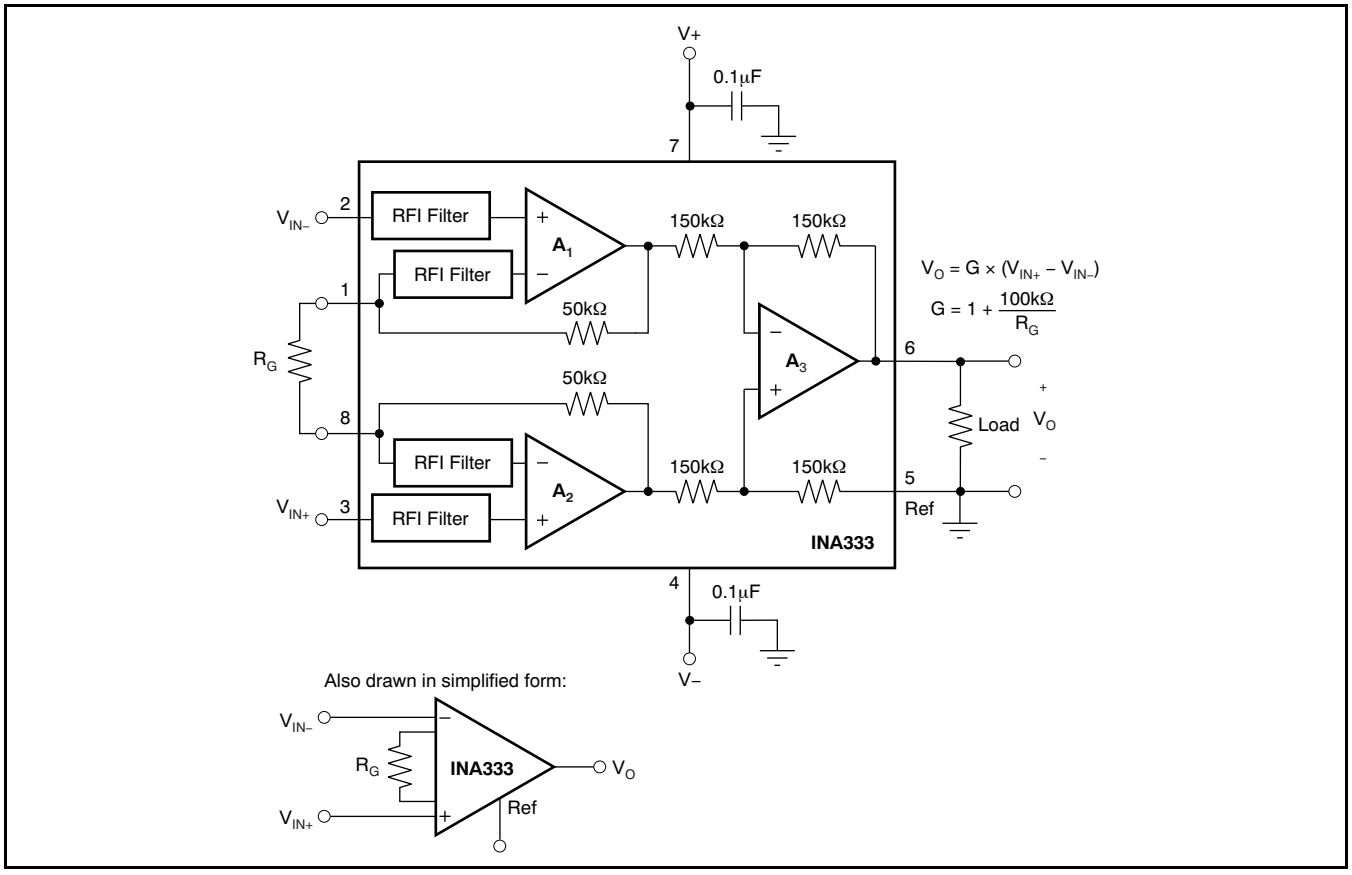

Figure 32. Basic Connections

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

INTERNAL OFFSET CORRECTION

The INA333 internal op amps use an auto-calibration technique with a time-continuous 350kHz op amp in the signal path. The amplifier is zero-corrected every 8µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

OFFSET TRIMMING

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.

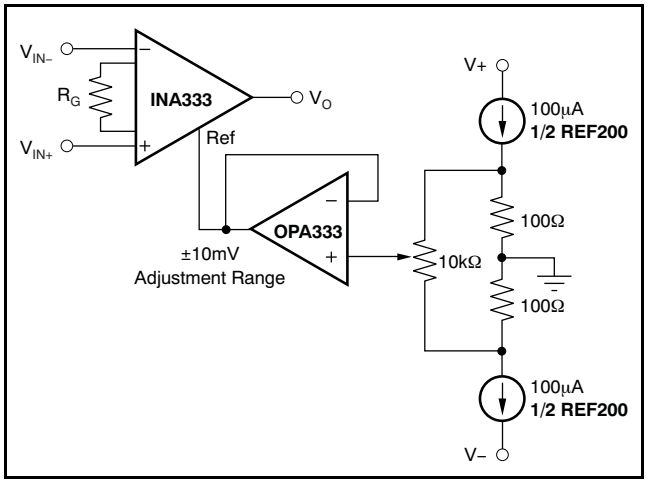

Figure 33. Optional Trimming of Output Offset Voltage

NOISE PERFORMANCE

The auto-calibration technique used by the INA333 results in reduced low frequency noise, typically only 50nV/√Hz, (G = 100). The spectral noise density can be seen in detail in Figure 8. Low frequency noise of the INA333 is approximately 1µV_{PP} measured from 0.1Hz to 10Hz, (G = 100).

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA333 is extremely high—approximately 100GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 34 illustrates various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range of the INA333, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 34). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

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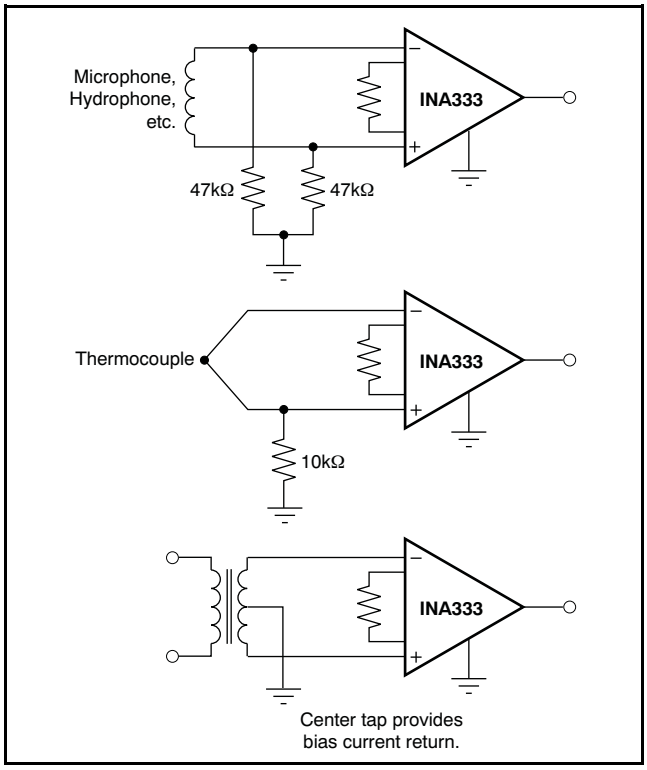

Figure 34. Providing an Input Common-Mode Current Path

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA333 is from approximately 0.1V below the positive supply voltage to 0.1V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 20 to Figure 23).

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0V even though both inputs are overloaded.

OPERATING VOLTAGE

The INA333 operates over a power-supply range of +1.8V to +5.5V (±0.9V to ±2.75V). Supply voltages higher than +7V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

LOW VOLTAGE OPERATION

The INA333 can be operated on power supplies as low as ±0.9V. Most parameters vary only slightly throughout this supply voltage range—see the Typical Characteristics section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 20 to Figure 23) show the range of linear operation for various supply voltages and gains.

SINGLE-SUPPLY OPERATION

The INA333 can be used on single power supplies of +1.8V to +5.5V. Figure 35 illustrates a basic single-supply circuit. The output REF terminal is connected to mid-supply. Zero differential input voltage demands an output voltage of mid-supply. Actual output voltage swing is limited to approximately 50mV above ground, when the load is referred to ground as shown. The typical characteristic curve *Output Voltage Swing vs Output Current* (Figure 29) shows how the output voltage swing varies with output current.

With single-supply operation, V_{IN+} and V_{IN-} must both be 0.1V above ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 35. It shows the INA333 operating from a single 3V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier inputs.

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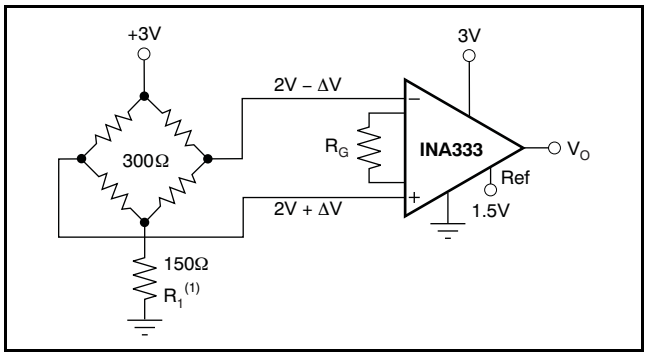

(1) R_1 creates proper common-mode voltage, only for low-voltage operation—see the *Single-Supply Operation* section.

Figure 35. Single-Supply Bridge Amplifier

INPUT PROTECTION

The input terminals of the INA333 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3V, the input signal current should be limited to less than 10mA to protect the internal clamp diodes. This current limiting can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF bypass capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333 has been specifically designed to minimize susceptibility to RFI by incorporating RFI filters at the V_{IN+} and $V_{IN–}$ inputs. As a result, the INA333 demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

APPLICATION IDEAS

Additional application ideas are shown in Figure 36 to Figure 39.

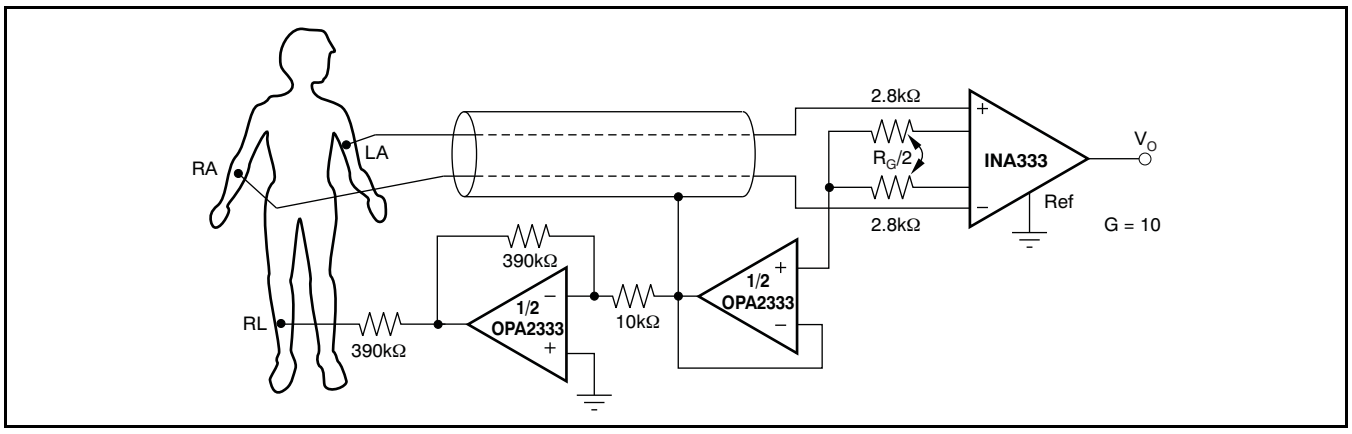

Figure 36. ECG Amplifier With Right-Leg Drive

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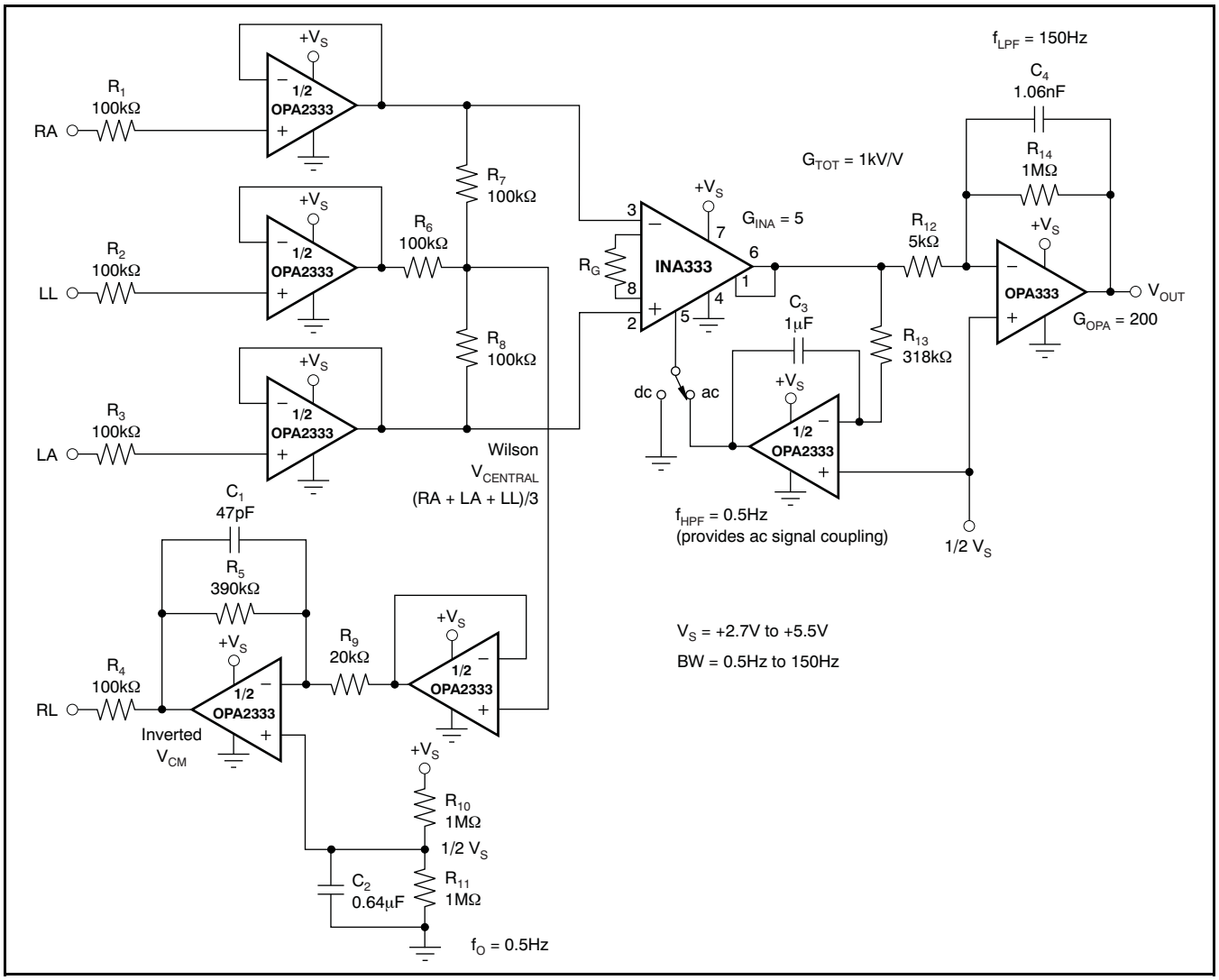


Figure 37. Single-Supply, Very Low Power, ECG Circuit

TINA-TI (FREE DOWNLOAD SOFTWARE)

Using TINA-TI SPICE-Based Analog Simulation Program with the INA333

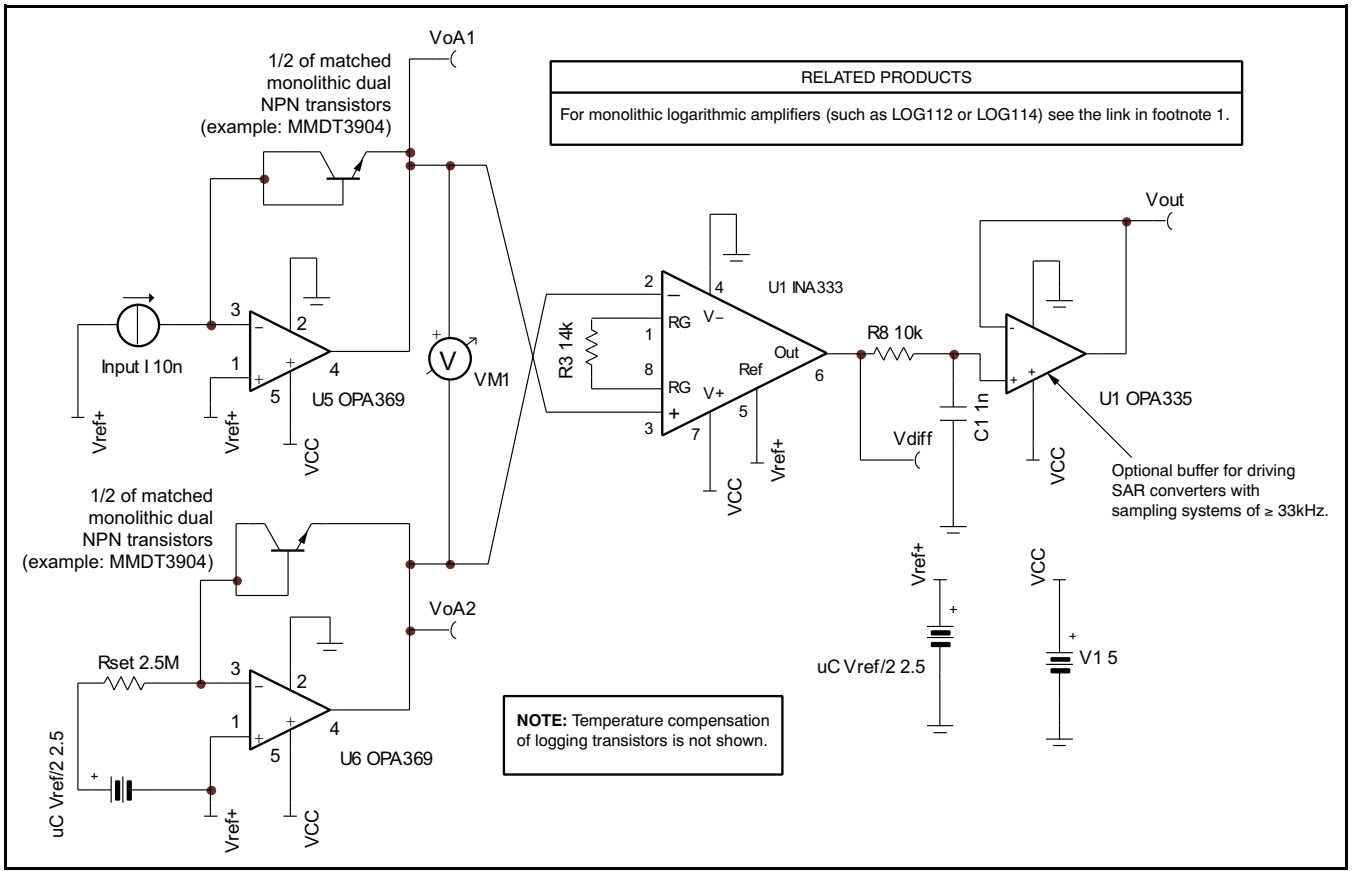
TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 38 and Figure 39 show example TINA-TI circuits for the INA333 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

NOTE: these files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.



(1) The following link launches the TI logarithmic amplifiers web page: Logarithmic Amplifier Products Home Page

Figure 38. Low-Power Log Function Circuit for Portable Battery-Powered Systems (Example Glucose Meter)

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: Log Circuit.

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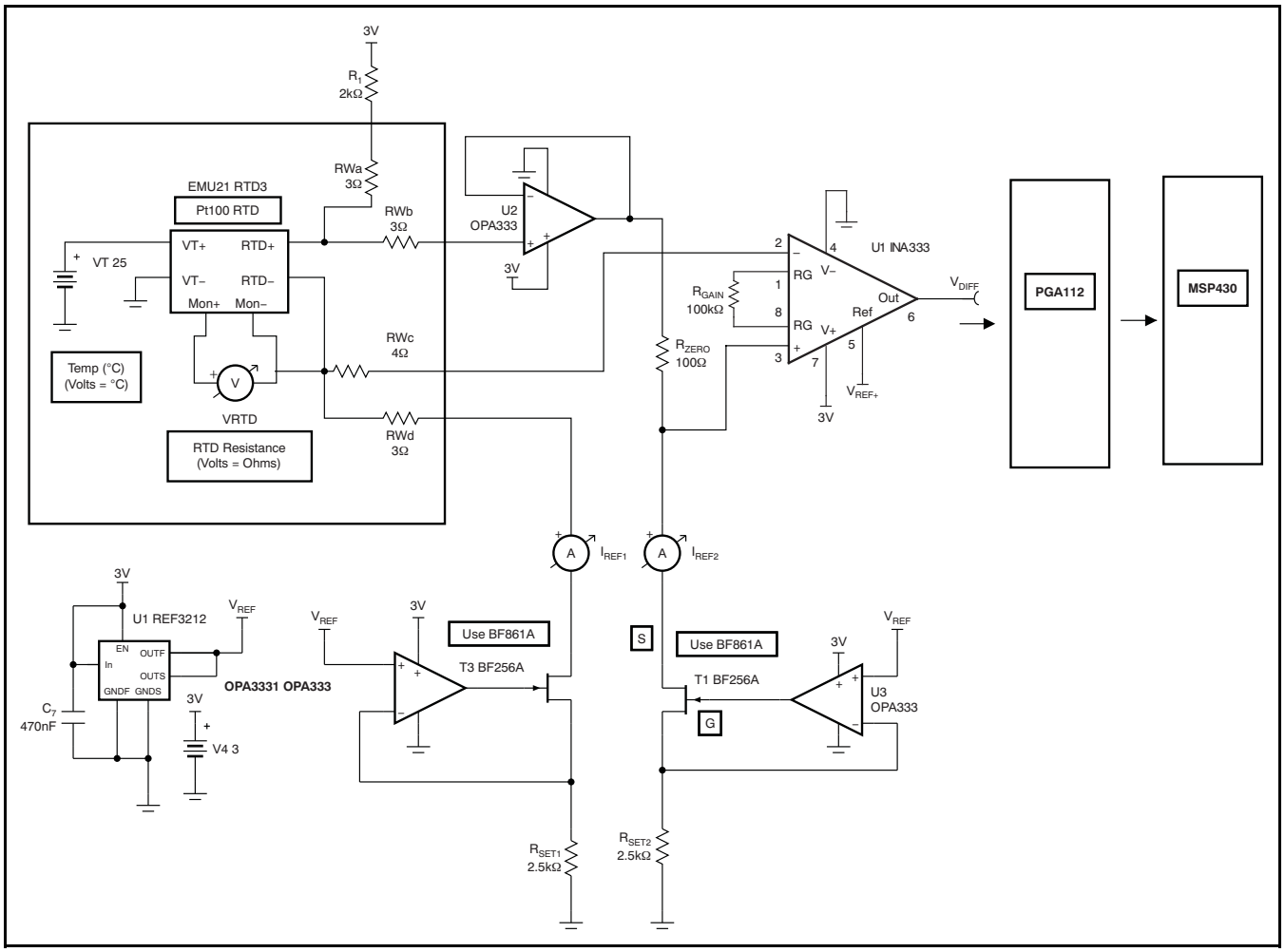

RWa, RWb, RWc, and RWd simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.

Figure 39. Four-Wire, 3V Conditioner for a PT100 RTD With Programmable Gain Acquisition System

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: PT100 RTD.

PACKAGE OPTION ADDENDUM

15-Jul-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA333AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
INA333AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
INA333AIDRGR	PREVIEW	SON	DRG	8	1000	TBD	Call TI	Call TI
INA333AIDRGT	PREVIEW	SON	DRG	8	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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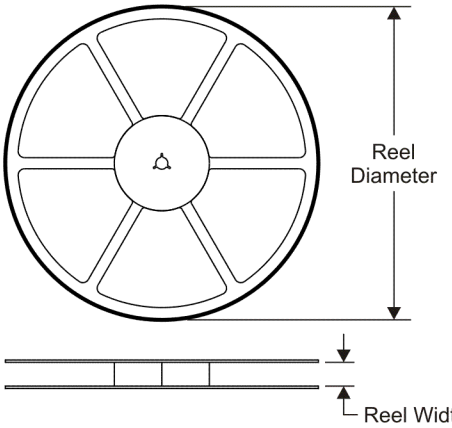
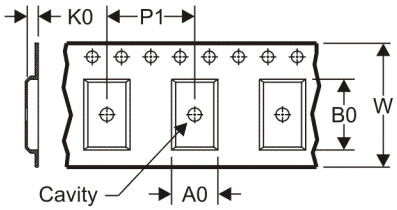
REEL DIMENSIONS

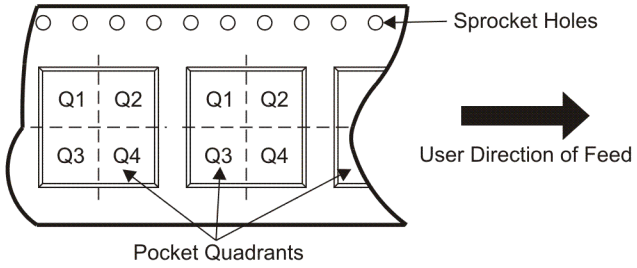


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

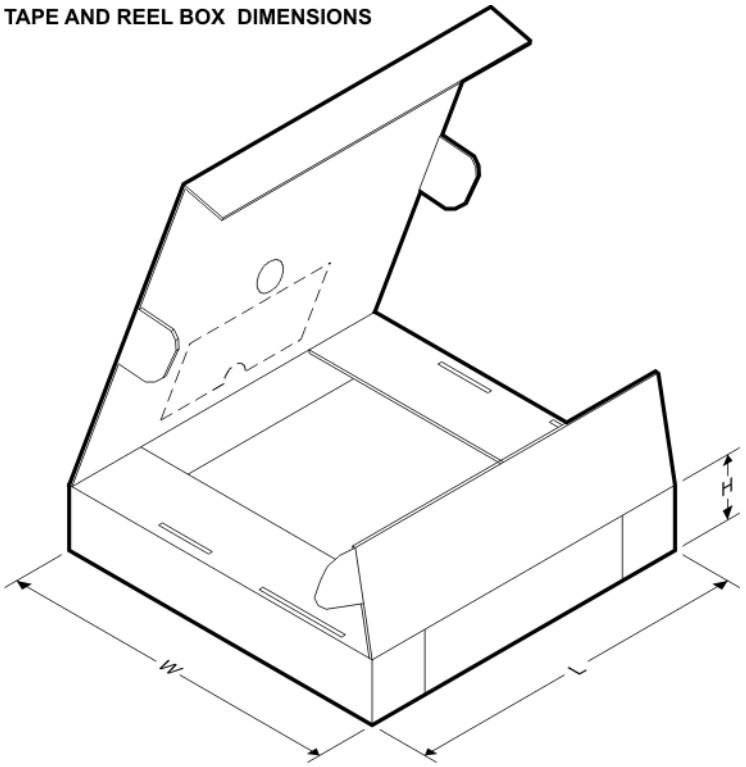
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA333AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
INA333AIDGKT	MSOP	DGK	8	250	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

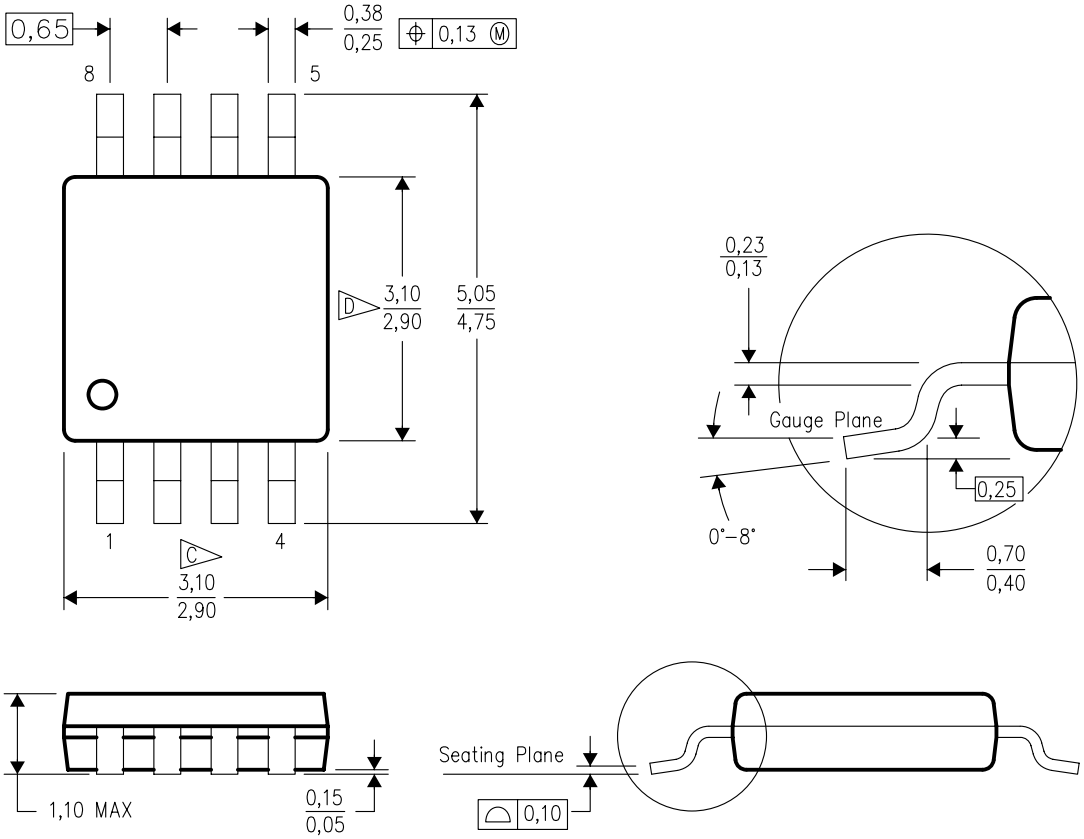
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA333AIDGKR	MSOP	DGK	8	2500	370.0	355.0	55.0
INA333AIDGKT	MSOP	DGK	8	250	370.0	355.0	55.0

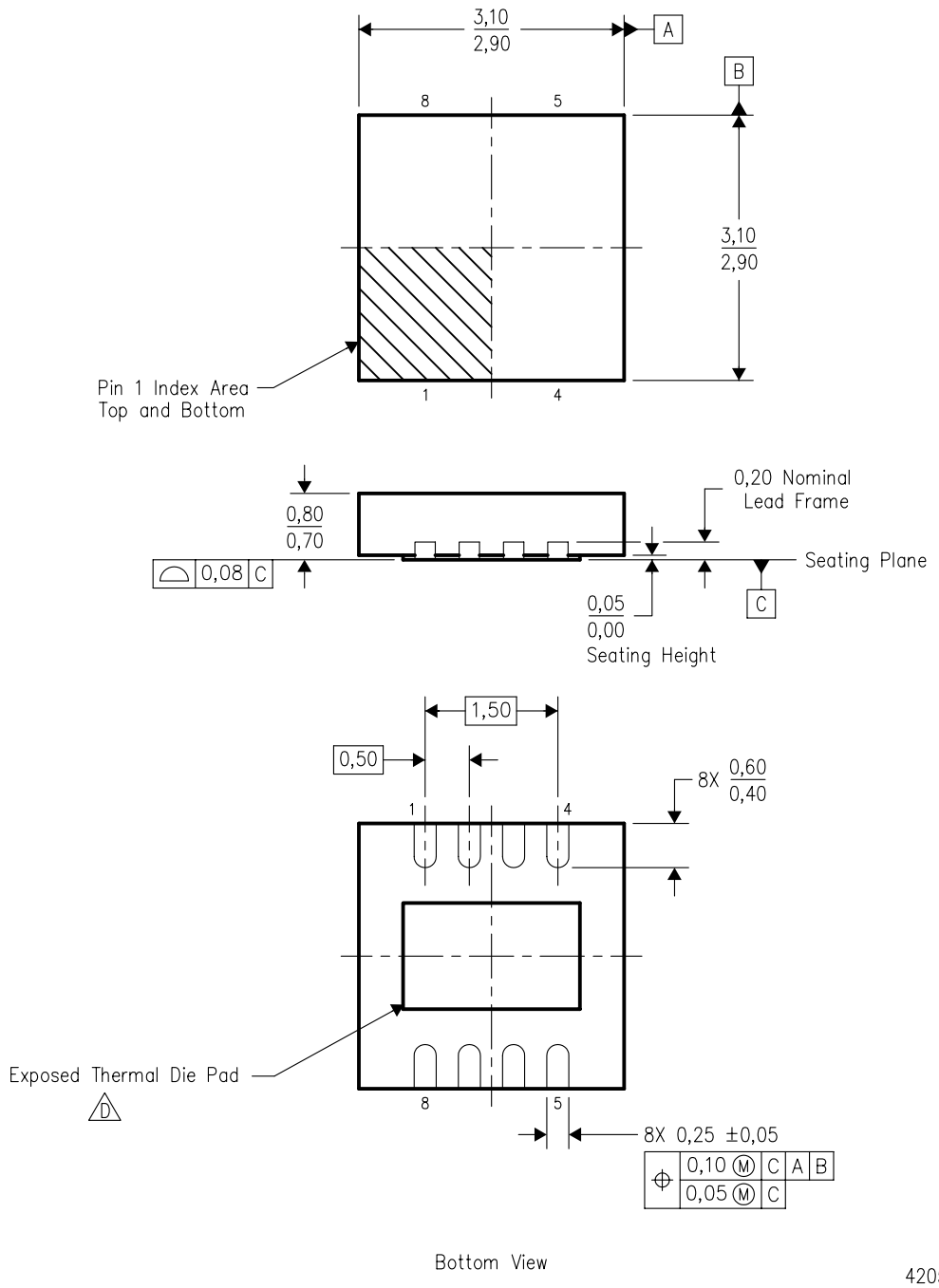
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRG (S–PDSO–N8) PLASTIC SMALL OUTLINE



4205379/B 03/2005

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
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