inova® Semiconductors

PRODUCT DATASHEET

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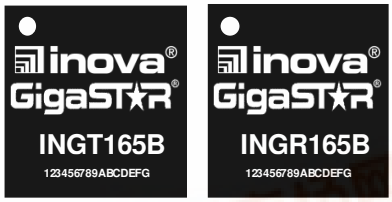
1.32 Gbit/s Serial Link Transmitter and Receiver

GigaSTaR®

INGT165B
INGR165B



12x12 mm, 196 PBGA packages

The GigaSTaR® (**Giga**bit/s **S**erial **T**ransmitter **a**nd **R**eceiver) is a universal high-speed point-to-point communication link. It consists of two devices, the Transmitter INGT165B and the Receiver INGR165B.

The INGT165B Transmitter converts parallel data up to 36-bit to a serial bit-stream. The differential CML (Current Mode Logic) outputs can directly drive Shielded-Twisted-Pair (STP) cables for distances up to 50 meters and can directly interface to inputs of fiber optic modules to span longer distances.

The INGR165B Receiver converts the serial bit-stream to the original parallel data format, fully transparent and without protocol overhead.

Link-synchronization, bit-stream coding/decoding, clock-/frame-recovery and parity-check are managed by internal high-speed resources.

GigaSTaR® links can be operated in parallel, scaling the bandwidth in multiples of 1.188 Gbit/s (payload data rate).

FEATURES

- 36-bit 33 MHz parallel data interface (3.3V CMOS)
- Variable payload data transfer rate up to 1.188 Gbit/s
- Internal RF clock-generation and clock-recovery (PLL)
- Integrated DC-balanced coding for AC coupling
- Integrated cable equalizer (INGR165B)
- Built in parity check
- Low latency of 40 ns per device (type)
- Differential, low-swing CML-signals for the serial link
- High signal robustness, EMI and noise immunity
- Direct interfacing to 50/100 Ohm cables and fiber optic modules
- Single +3.3V DC supply
- Low power dissipation of 1 W per device (type)
- Ambient operating temperature – 40°C to +85° C

APPLICATIONS

- High-speed scanning / printing (photo, exposure- and security systems)
- Mass storage connections
- High-speed and multi-channel imaging
- Telecommunication switches
- High-speed sensors / actuators
- Industrial Control
- High-resolution panel links
- Data broadcast (Video Server)

Figure 1: GigaSTaR® Link

1. GigaSTaR® LINK DESCRIPTION

The GigaSTaR® link is designed for reliable, high-speed, low-latency data transmission.
All functions for data transfer management including the high-frequency blocks are fully integrated in the Transmitter and Receiver devices. Both devices feature a 36-bit “user-friendly” parallel interface with standard logic levels (3.3V CMOS) for easy adaptation to any application.

The link supports an effective (sustained) data rate up to 148.5 MByte/s at the parallel interface, which translates to a serial bit stream of max. 1.188 Gbit/s (payload data rate). With 4 additional bits for link-synchronization, DC-balancing and parity check the maximum bit rate at the serial I/Os is 1.32Gbit/s, for an overall link efficiency of 90 percent. With only 40 ns propagation delay time each for the Transmitter and Receiver, the typical overall latency for a GigaSTaR® link with STP copper cable is:

latency [ns] = 2 * 40 ns + 4ns/m * cable-length [m]

For example, the latency is about 160 ns for a 20 meter connection with Shielded-Twisted-Pair (STP) copper cable.

1.1 CLOCK SYSTEM

The serial bit clock frequency of 1320 MHz is generated by internal PLLs. The Transmitter and Receiver each require an external 66 MHz reference clock.

A continuous phase alignment in the Receiver ensures that the receive clock is synchronous to the transmit clock.

1.2 PARALLEL DATA FORMAT

Both the GigaSTaR® Transmitter and Receiver feature a synchronous 36 bit parallel interface. The maximum frequency at this interface is 33 MHz, equivalent to a period of 30.3 ns for the WRCLK/ RDCLK signals.

Additional parity I/Os allow the transfer of an optional external parity bit synchronous with the parallel data. If an external parity bit is provided, the Transmitter validates the signal before the start of the transmission. If no external parity bit is available, the Transmitter generates this signal automatically.
Parity error flags are provided at both the Transmitter and Receiver devices.

1.3 SERIAL DATA FORMAT

The serial data stream is DC-balanced to support capacitive (AC) coupling for full DC isolation of the link. This is performed by proprietary coding in the Transmitter device.

1.4 LINK MEDIA (COPPER OR FIBER)

The GigaSTaR® Transmitter and Receiver are each equipped with a robust high-speed interface which can be directly connected to impedance-controlled cables (STP or coax), transmission lines or fiber optic modules.

Initial evaluations with 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cables already have proven reliable transmissions at distances of up to 50 meters and beyond (Reference-product: GGSC1608-05/-10/-15/-20/-30/-40/-50, W.L. Gore & Associates).
Copper media require a serial line termination (R/L combination) at the inputs of the GigaSTaR® Receiver for optimized performance, please refer to the ING_TRC piggyback board data sheet for reference values. The capacitors for AC coupling of the serial lines have to be 100nF and are to be applied at both ends of the link medium (see also figure 1). It is required to use ceramic RF capacitors.

With conventional 850 nm fiber optic modules (AC in/out, 3.3V PECL) and multimode fiber distances up to 550 meters have been achieved, see also datasheet of the ING_TRF fiberoptical piggyback board.

2. GigaSTaR® INGT165B TRANSMITTER

2.1 BLOCK DIAGRAM

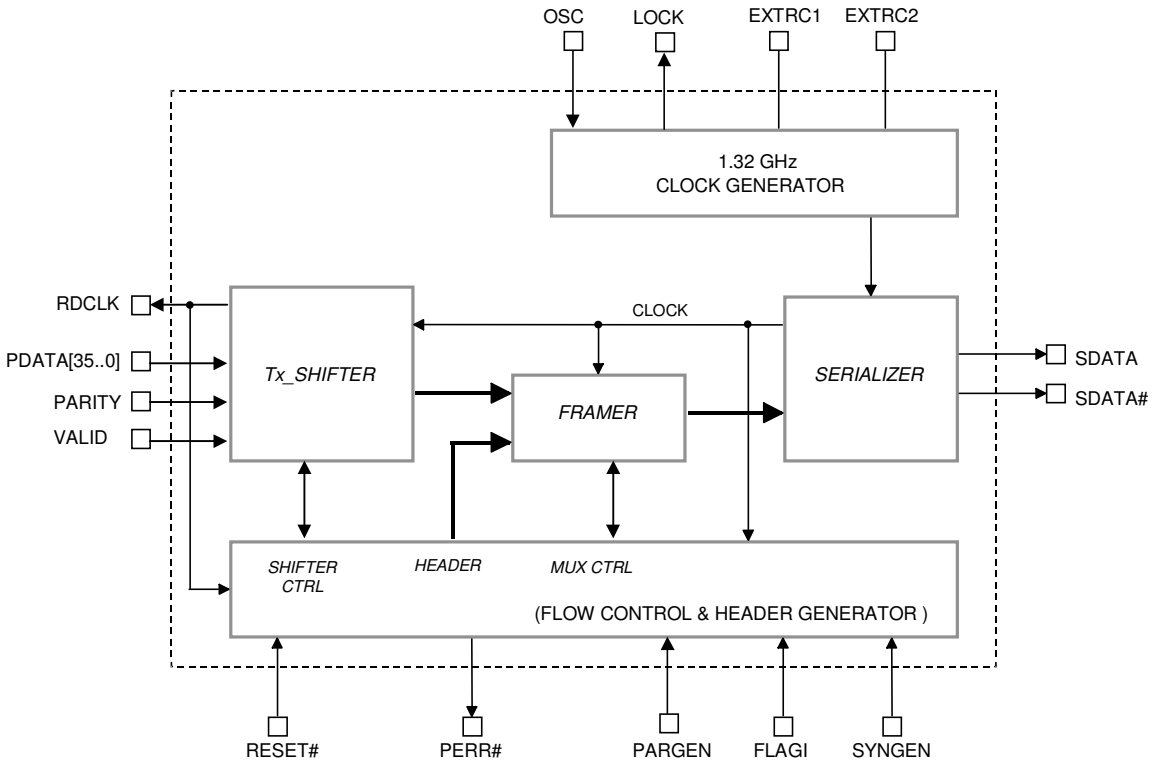


Figure 2: GigaSTaR® Transmitter Block Diagram

2.2 INGT165B TRANSMITTER PARALLEL INTERFACE

The Transmitter parallel interface is designed to support different operating modes providing a maximum flexibility for the design of the application interface.

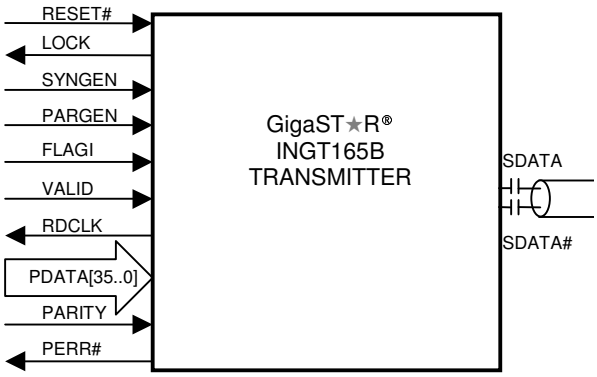


Figure 3: GigaSTaR® Transmitter Parallel Interface

2.2.1 Control Signals

RESET# is an asynchronous active low reset signal. After a power-up sequence and activation of the reference clock, RESET# has to be kept low for at least 1 ms. The link is operational as soon as the LSYNC# signal of the Receiver is going low.

LOCK = '1' indicates that the internal PLL is locked. If LOCK is de-asserted the Transmitter is not ready.

PARGEN = '1' activates the internal parity generation. In this mode the PARITY input pin is ignored. An internal parity bit is generated and transmitted.

The positive edge of FLAGI sets an internal flag which is inserted at the end of the data word currently in transmission. The Receiver decodes the flag out of the serial bit-stream and toggles the level of the FLAGO output. This signal can be used to mark the end of a data frame.

VALID = '1' indicates to the Transmitter that data are available. With the assertion of VALID the RDCLK starts to run. PDATA[35..0] is registered at each rising edge of RDCLK. De-asserting VALID disables RDCLK and stuffing patterns are transmitted over the GigaSTaR® link to maintain synchronization.

PERR#: description see 2.2.2

Note: the SYNGEN input is reserved for optional functions and has to be set to “0”.

2.2.2 Data Interface

The GigaSTaR® parallel data interface is designed to support a variety of application interfaces. It provides read clock (RDCLK) pulses with a cycle time of 30,3 ns (corresponding to 33MHz) to the application output buffers like FIFOs, memory devices, ASICs or PLDs.

A data word at the parallel interface consists of 36 data bits. If PARGEN = '0' the transmitting application has to supply the data's parity at the input PARITY synchronous to the parallel data. PARGEN = '1' logic high activates internal parity generation and the PARITY input pin is ignored. If the application supplies its own parity bit (PARGEN is de-asserted), PERR# reports any mismatch between the internally generated and the external PARITY signal. If this is the case, the internally generated (correct) PARITY is transmitted with the data word. PERR# is always inactive when PARGEN = '1'. The default value of PERR# after reset is ‘1’.

2.2.3 Data Burst Transfers

The data burst timing provides the full data rate of 148.5 MByte/s. VALID is asserted when the first data is valid at PDATA[35.0]. With every rising edge of RDCLK the PDATA inputs are registered, serialized and transmitted. VALID can remain asserted as long as new data are available.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

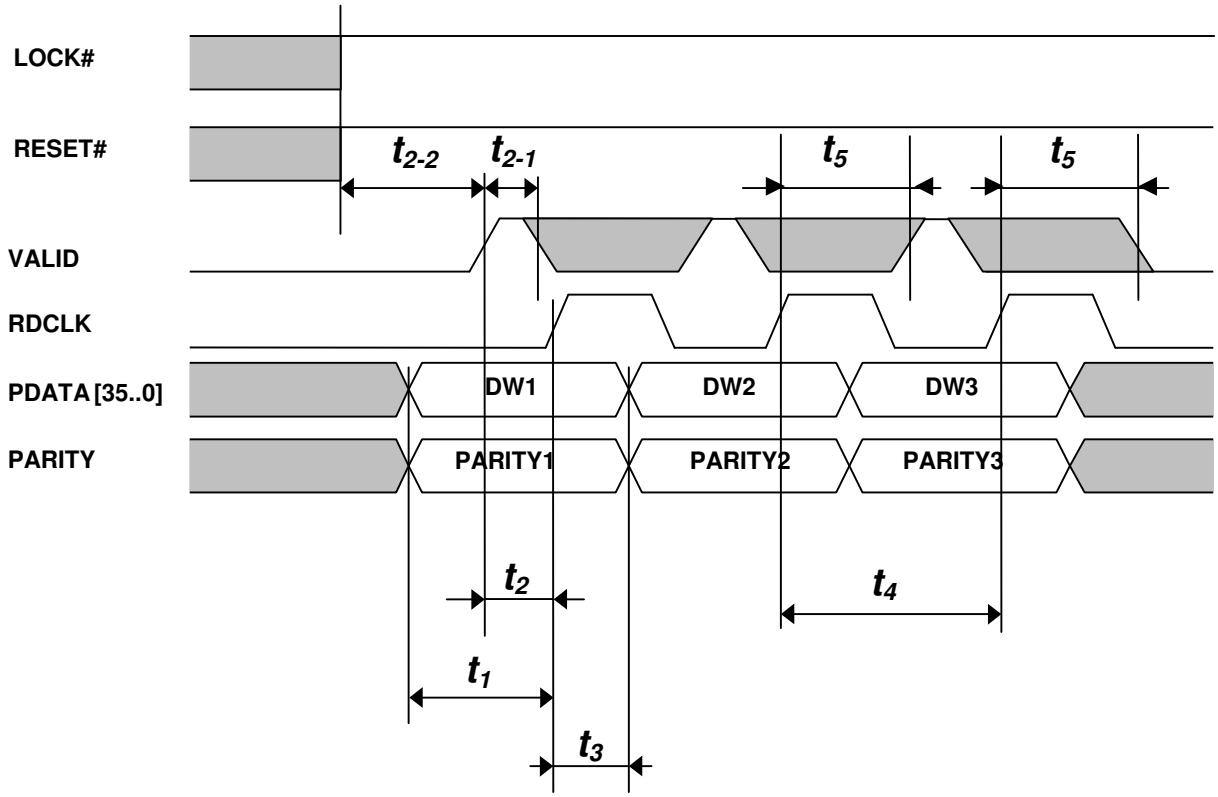


Figure 4: INGT165B Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t_2	VALID active to first rising RDCLK edge	9	12	14	ns
t_{2-1}	VALID high state	5	4		ns
t_{2-2}	LOCK# / RESET# high state before Tx operational *	50			µs
t_3	PDATA and PARITY hold time	9	6		ns
t_4	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t_5	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns

Note : For timings with assertion of FLAGI, please see section 3.2.5

*A dislock pulse generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 1: INGT165B Data Burst Timing Parameters (under recommended operating conditions)

2.2.4 Single Word Transfers

Single Word Transfers are used to support lower data rates than the maximum parallel data rate of 148.5 MByte/s. VALID has to be de-asserted after the parallel read cycle signaled by one RDCLK pulse. Only one data word is transmitted.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

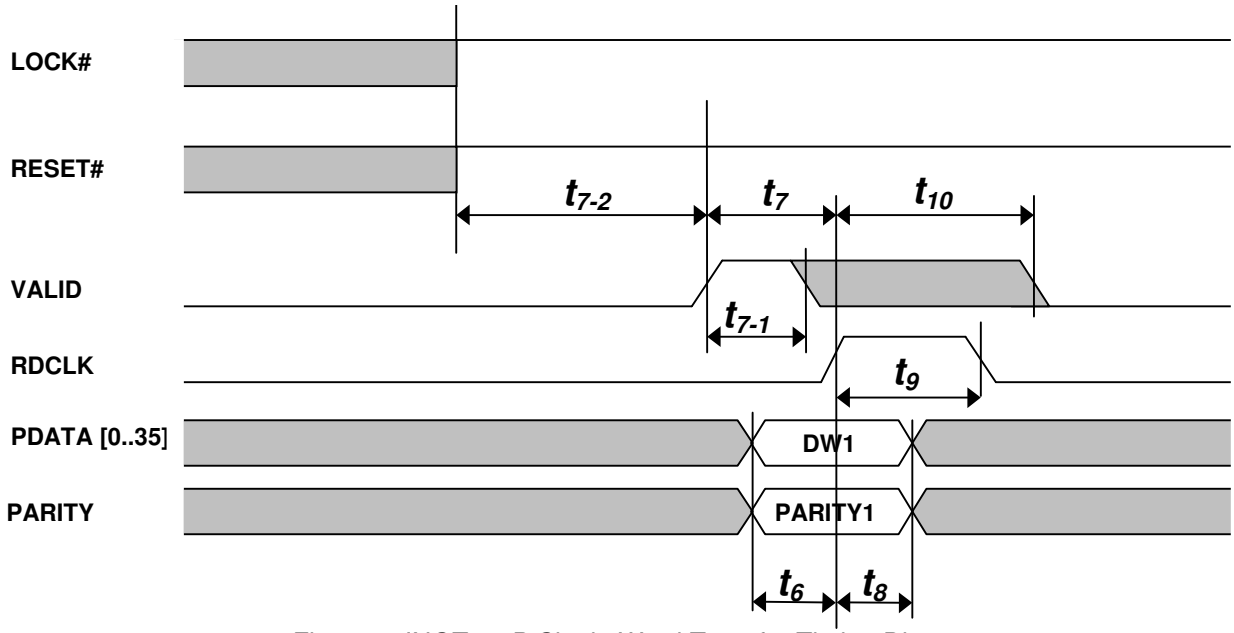


Figure 5: INGT165B Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_6	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t_7	VALID active to rising RDCLK edge	9	12	14	ns
t_{7-1}	VALID high state	5	4		ns
t_{7-2}	LOCK# / RESET# high state before TX operational *	50			µs
t_8	PDATA and PARITY hold time	9	6		ns
t_9	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t_{10}	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns

Note : For timings with assertion of FLAGI, please see section 3.2.5

* A dislock pulse generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 2: INGT165B Single Word Transfer Timing Parameters (Under recommended operating conditions)

3. GigaSTaR® INGR165B RECEIVER

3.1 BLOCK DIAGRAM

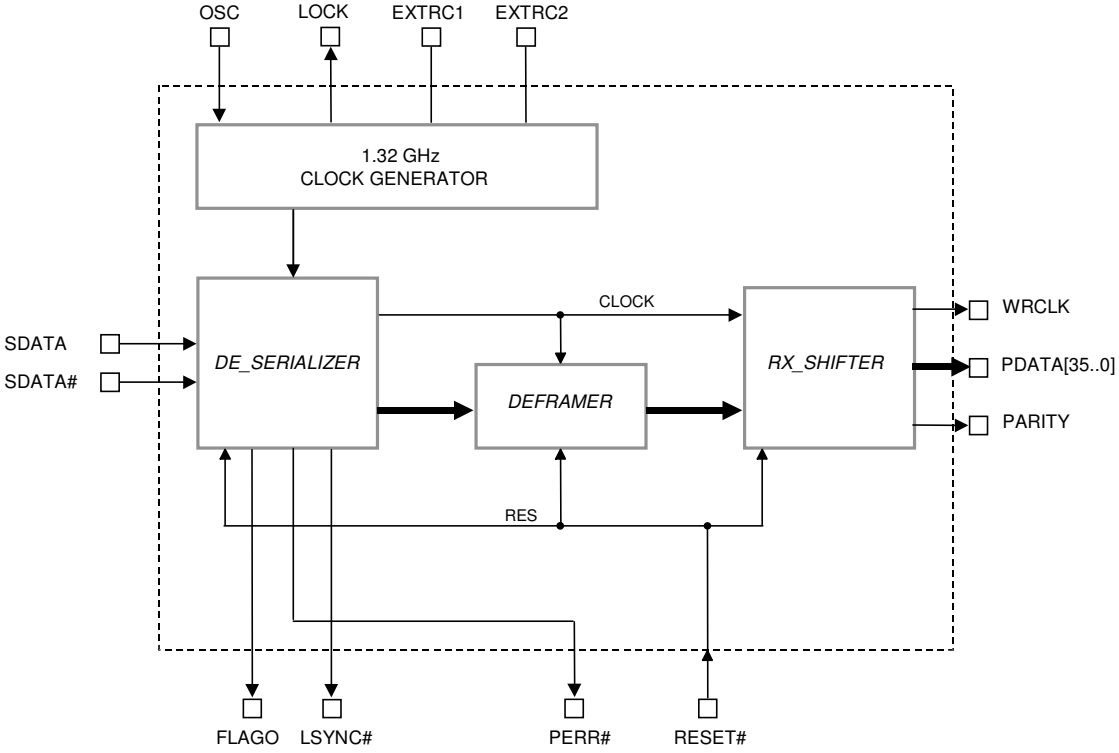


Figure 6: GigaSTaR® Receiver Block Diagram

3.2 INGR165B RECEIVER PARALLEL INTERFACE

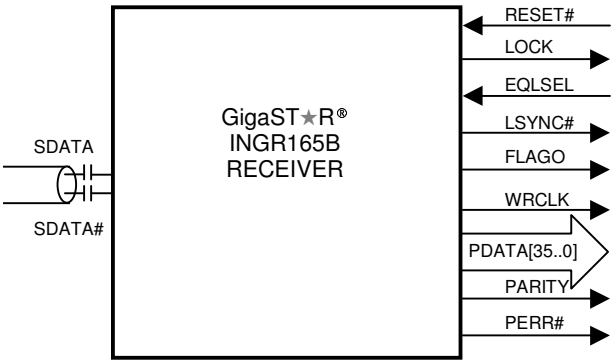


Figure 7: GigaSTaR® Receiver Parallel Interface

3.2.1 Control Signals

RESET# is an asynchronous active low reset signal. After a power-up sequence and activation of the reference clock, RESET# has to be kept low for at least 1 ms. The link is operational as soon as the LSYNC# signal is going low.

LOCK = ' 1' indicates that the internal PLL is locked. If LOCK is de-asserted, the Receiver is not ready.

EQLSEL activates the internal equalizer to support extended cable lengths above 10 meters.

FLAGO is the sideband signalling output flag, for timing details see 3.2.5.
The default state of FLAGO after reset is '0'.

The status bit LSYNC# is asserted if the GigaSTaR® Receiver is synchronized to the incoming bit-stream. If the Receiver is not synchronized correctly, LSYNC# is de-asserted.

The receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal PERR# is asserted for one data cycle. LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

3.2.2 Data Interface

The parallel interface is designed to support a variety of application interfaces.
It provides a sequence of write clock (WRCLK) pulses with a cycle time of 30.3 ns (corresponding to 33MHz) which is used to clock data into the remote application' s input buffer like a FIFO, memory devices or directly into an ASIC or PLD.

A data word at the parallel interface consists of 36 data bits. The data' s parity is always available synchronous to the data at the PARITY output. The application may use the parity bit for additional information about the data' s validity. As long as data with a wrong parity are transmitted, the Receiver is not synchronized with the Transmitter, and the LSYNC# signal is de-asserted.

3.2.3 Data Burst Transfers

The data burst timing is used to support the full data rate of 148.5 MByte/s.
PDATA[35..0] and PARITY are updated with each rising edge of WRCLK.

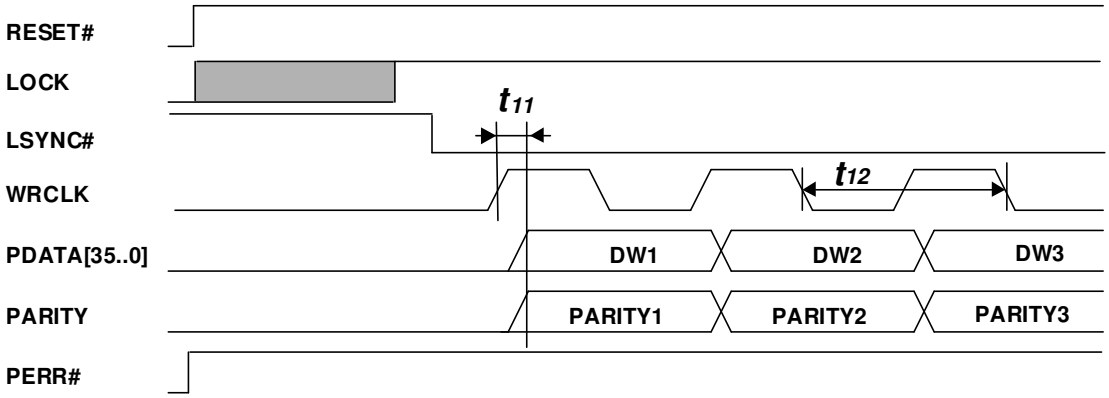


Figure 8: INGR165B Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_{11}	Rising edge WRCLK to PDATA and PARITY bit valid		1	4	ns
t_{12}	WRCLK cycle time (without assertion of FLAGI)		30.3		ns

Note: For timings with assertion of FLAGI, please see section 3.2.5

Table 3: INGR165B Data Burst Timing Parameters (Under recommended operating conditions)

3.2.4 Single Word Transfers

Single Word Transfers are used to support lower data rates. Every time a new data word is received the WRCLK signal generates one clock pulse.

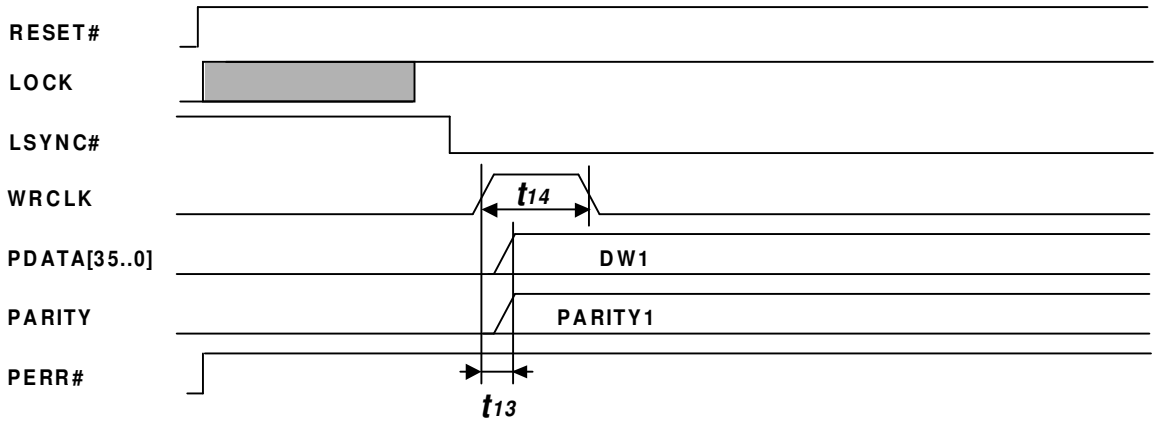


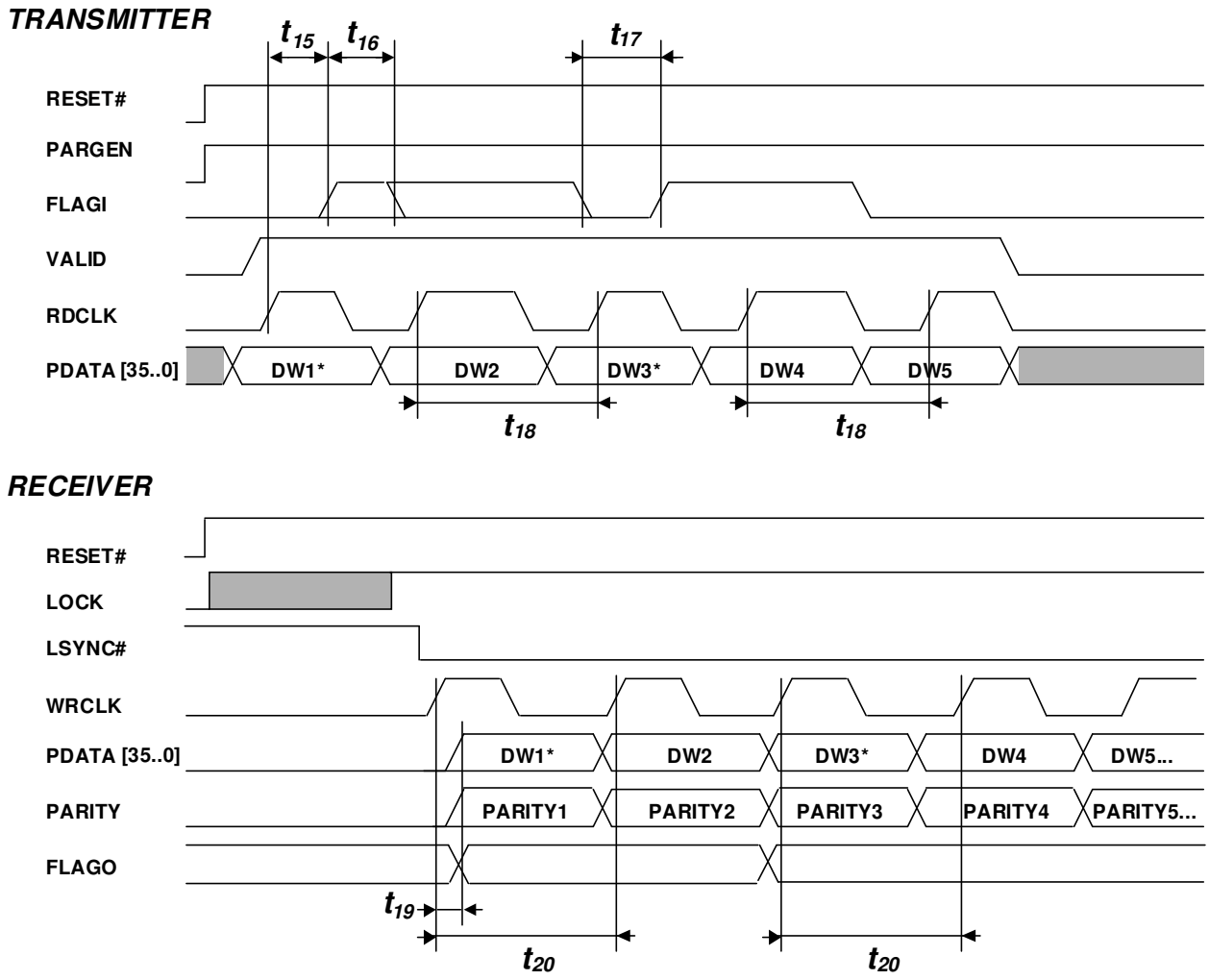
Figure 9: INGR165B Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_{13}	Rising edge WRCLK to PDATA and PARITY valid		1	4	ns
t_{14}	WRCLK high state	14	15	16	ns

Table 4: INGR165B Single Word Transfer Timing Parameters (under recommended operating conditions)

3.2.5 FLAGI / FLAGO Timing

With the FLAGI / FLAGO signals a mechanism is provided to implement a sideband signalling. Each rising edge at the Transmitter's input FLAGI toggles the FLAGO output of the Receiver. The timing diagram for the FLAGI/FLAGO signal is shown in combination with the Transmitter signals. Note that when the FLAGI signal is asserted, the following RDCLK high state time span is enlarged by app. 6 ns. At the Receiver, the WRCLK low state time span is enlarged by app. 6 ns when the FLAGO output toggles. In the diagrams below, the PARGEN is active at the Transmitter, therefore no external parity is provided.



Note : * indicates the data words [DW1, DW3] that are marked by the FLAGI signal.

Figure 10: INGT165B / INGR165B FLAGI and FLAGO Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_{15}	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t_{16}	FLAGI minimum high state		4	6	ns
t_{17}	FLAGI minimum low state		4	6	ns
t_{18}	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t_{19}	Rising edge of WRCLK to PDATA, PARITY and FLAGO valid		1	4	ns
t_{20}	WRCLK cycle time for data word marked by FLAGO toggle		36		ns

Table 5: INGT165B / INGR165B FLAGI and FLAGO Timing Parameters
(under recommended operating conditions)

3.2.6 Parity Error (Reporting) Timing

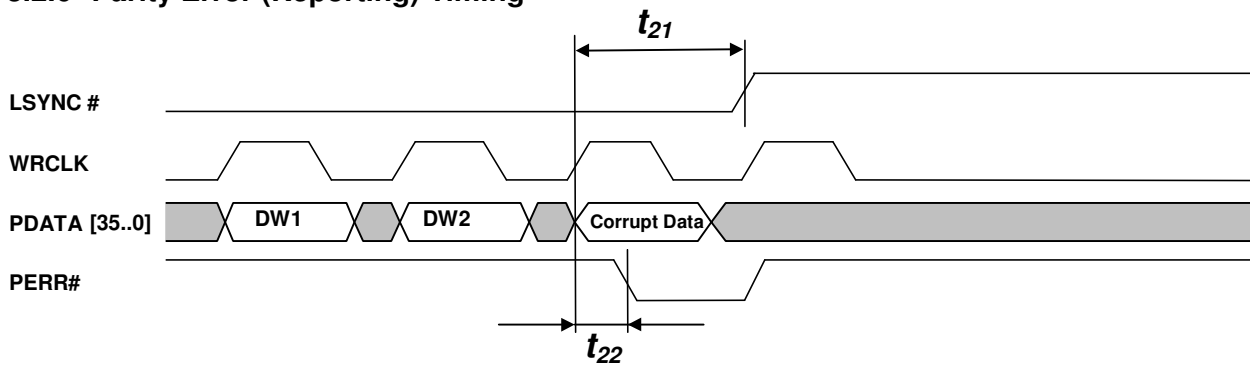


Figure 11: INGR165B Parity Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{21}	Rising edge of WRCLK marking the corrupt data word to rising edge of LSYNC#		30	40	ns
t_{22}	Rising edge of WRCLK marking the corrupt data word to falling edge of PERR#		3	6	ns

Table 6: INGR165B Parity Error (reporting) timing (under recommended operating conditions)

3.2.7 Header/Frame Error (Reporting) Timing

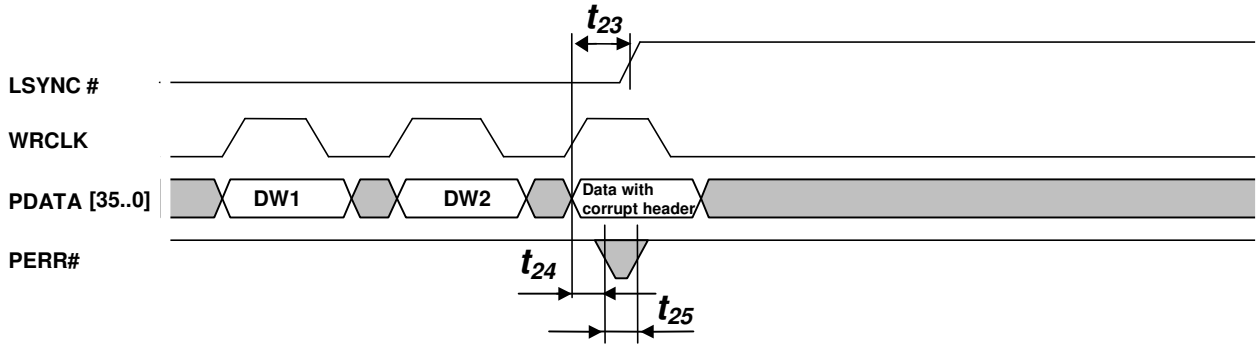


Figure 12: INGR165B Header/Frame Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{23}	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0	11	15	ns
t_{24}	Rising edge of WRCLK marking the corrupt data header to falling edge of PERR#		1,5		ns
t_{25}	PERR # low state		3		ns

Table 7: INGR165B Header/Frame Error (reporting) timing (under recommended operating conditions)

4. DEVICE SPECIFICATION

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	-0.5	+4.2	V	See handling precautions (6)
Input Voltage	V_{IN}	-0.5	V_{CC}+0.5	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	See handling precautions (6)
Junction Temperature (under bias)	T_j	-45	+140	° C	
Storage Temperature	T_{stg}	-55	+150	° C	
Soldering Temp./Time	T_{SLD} / t_{SLD}		220 / 10	° C / sec	
Static Discharge Voltage (CMOS dig. I/O versus respective GND & Supply rails)	V_{SDCMOS}		± 2000	V	Human Body Model
Static Discharge Voltage (all other pin combinations including CML I/O pins)	V_{SDCML}		± 800	V	Human Body Model

Table 8: Absolute Maximum Ratings

4.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	+3.15	+3.45	V	
Input Voltage	V_{IN}	0	Vcc	V	V_{CC} =3.3V ± 0.15V
CML Output Current	I_{OUTCML}	-10	+10	mA	
CMOS Output Current	$I_{OUTCMOS}$	-10	+10	mA	
Junction Temperature (under bias)	T_j	-40	+125	° C	
Ambient Temperature	T_a	-40	+85	° C	

Table 9: Recommended Operating Conditions

4.3 ELECTRICAL SPECIFICATION

4.3.1 AC – Characteristics

(under recommended operating conditions, Reference Clock Frequency = 66 MHz)

Parameter	Min.	Typ.	Max.	Units
Input capacitance, any pin (@ 66 MHz)		1.5	3	pF
Serial Transmission Data Rate		1.32		Gbit/s
Serial Payload Data Rate		1.188		Gbit/s
Parallel Interface Data Rate		148.5		MByte/s
Serial Bit Width		757.6		ps
CMOS Output Rise / Fall Time (C_L = 10 pF)		5	10	ns

Table 10: AC – Characteristics

4.3.2 DC – Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CMOS Input High Voltage	V_{IH}		2.6			V
CMOS Input Low Voltage	V_{IL}				0.7	V
CMOS Input High Current	I_{IH}	V_{IN} = Vcc	-1		1	µA
CMOS Input Low Current	I_{IL}	V_{IN} = 0 V	-1		1	µA
EQLSEL/OSC Pin High Current	I_{IH}	V_{IN} = Vcc	-10		40	µA
EQLSEL/OSC Pin Low Current	I_{IL}	V_{IN} = 0 V	-10		10	µA
CMOS Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0,95Vcc			V
CMOS Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA			0,05 Vcc	V
CMOS Output High Current	I_{OH}	V_{OH} = 0.9Vcc	-3	-5		mA
CMOS Output Low Current	I_{OL}	V_{OL} = 0.1Vcc	3.5	6		mA
LOCK Output High Current	I_{LH}	V_{OH} = 0.9Vcc	-1	-2.5		mA
LOCK Output Low Current	I_{LL}	V_{OL} = 0.1Vcc	1.5	3		mA
INGT165B Supply Current	I_{CCTX}	CMOS output load = 10 pF		340	430	mA
INGR165B Supply Current	I_{CCRX}	CMOS output load = 10 pF		300	360	mA
INGT165B Power Dissipation	P_{DTX}	Max. data transmission rate		1.1	1.5	W
INGR165B Power Dissipation	P_{DRX}	Max. data transmission rate		1	1.25	W

Table 11: DC – Characteristics (under recommended operating conditions)

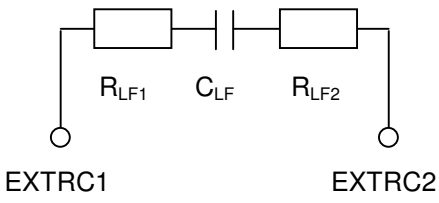
Note : *A floating CMOS input can result in heavy internal current draws. To achieve best performance for unused inputs an external pull-up should be added.*

4.3.3 Reference Clock Specification (Ta = -40 to 85° C; Vcc = 3.15 to 3.45 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Nominal Frequency	f_{OSC}		66		MHz	
Frequency Tolerance	F_{TOL}	-100		+100	ppm	
Duty Cycle		40		60	%	

Table 12: Reference Clock Specification

4.3.4 External Loop Filter Specification (Ta = -40 to 85° C)



The internal PLLs of the INGT165B and the INGR165B devices require an external RC loop filter.
It is not required to use dedicated RF R- and C-components, std components will perform correctly.

Parameter	Symbol	Value Tx	Value Rx	Note
Loop Filter Capacity	C_{LF}	1µF	1µF	Chip Capacitor (Ceramic)
Loop Filter Resistor 1	R_{LF1}	0 Ohm	47 Ohm	
Loop Filter Resistor 2	R_{LF2}	0 Ohm	47 Ohm	

Table 13: External Loop Filter Specification

4.3.5 Transmitter and Receiver Timing Parameters (under recommended operating conditions)

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t_2	VALID active to first rising RDCLK edge	9	12	14	ns
t_{2-1}	VALID high state	5	4		ns
t_{2-2}	LOCK# / RESET# high state before Tx operational	50			µs
t_3	PDATA and PARITY hold time	9	6		ns
t_4	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t_5	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns
t_6	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t_7	VALID active to rising RDCLK edge	9	12	14	ns
t_{7-1}	VALID high state	5	4		ns
t_{7-2}	LOCK# / RESET# high state before TX operational	50			µs
t_8	PDATA and PARITY hold time	9	6		ns
t_9	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t_{10}	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns
t_{11}	Rising edge WRCLK to PDATA and PARITY bit valid		1	4	ns
t_{12}	WRCLK cycle time (without assertion of FLAGI)		30.3		ns
t_{13}	Rising edge WRCLK to PDATA and PARITY valid		1	4	ns
t_{14}	WRCLK high state	14	15	16	ns
t_{15}	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t_{16}	FLAGI minimum high state		4	6	ns
t_{17}	FLAGI minimum low state		4	6	ns
t_{18}	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t_{19}	Rising edge of WRCLK to PDATA, PARITY and FLAGI valid		1	4	ns
t_{20}	WRCLK cycle time for data word marked by FLAGO toggle		36		ns
t_{21}	Rising edge of WRCLK after the corrupt data word to rising edge of LSYNC#		1	5	ns
t_{22}	Rising edge of WRCLK marking the corrupt data word to falling edge of PERR#		3	6	ns
t_{23}	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0		13	ns
t_{24}	Rising edge of WRCLK marking the corrupt data header to falling edge of PERR#		1,5		ns
t_{25}	PERR # low state		3		ns

Table 14: Transmitter and Receiver Timing Parameters (under recommended operating conditions)

INGT165B TRANSMITTER PIN DEFINITION

Pin Name	Pin #	Direction	Active	Description
PDATA[0]	A5	IN_{CMOS}	High	Parallel data input, Bit 0
PDATA[1]	B5	IN_{CMOS}	High	Parallel data input, Bit 1
PDATA[2]	A4	IN_{CMOS}	High	Parallel data input, Bit 2
PDATA[3]	B4	IN_{CMOS}	High	Parallel data input, Bit 3
PDATA[4]	A3	IN_{CMOS}	High	Parallel data input, Bit 4
PDATA[5]	B3	IN_{CMOS}	High	Parallel data input, Bit 5
PDATA[6]	A2	IN_{CMOS}	High	Parallel data input, Bit 6
PDATA[7]	B2	IN_{CMOS}	High	Parallel data input, Bit 7
PDATA[8]	B1	IN_{CMOS}	High	Parallel data input, Bit 8
PDATA[9]	C1	IN_{CMOS}	High	Parallel data input, Bit 9
PDATA[10]	D2	IN_{CMOS}	High	Parallel data input, Bit 10
PDATA[11]	E3	IN_{CMOS}	High	Parallel data input, Bit 11
PDATA[12]	D1	IN_{CMOS}	High	Parallel data input, Bit 12
PDATA[13]	E2	IN_{CMOS}	High	Parallel data input, Bit 13
PDATA[14]	E1	IN_{CMOS}	High	Parallel data input, Bit 14
PDATA[15]	F2	IN_{CMOS}	High	Parallel data input, Bit 15
PDATA[16]	G3	IN_{CMOS}	High	Parallel data input, Bit 16
PDATA[17]	G1	IN_{CMOS}	High	Parallel data input, Bit 17
PDATA[18]	H3	IN_{CMOS}	High	Parallel data input, Bit 18
PDATA[19]	H2	IN_{CMOS}	High	Parallel data input, Bit 19
PDATA[20]	J1	IN_{CMOS}	High	Parallel data input, Bit 20
PDATA[21]	J2	IN_{CMOS}	High	Parallel data input, Bit 21
PDATA[22]	L1	IN_{CMOS}	High	Parallel data input, Bit 22
PDATA[23]	K3	IN_{CMOS}	High	Parallel data input, Bit 23
PDATA[24]	K2	IN_{CMOS}	High	Parallel data input, Bit 24
PDATA[25]	M1	IN_{CMOS}	High	Parallel data input, Bit 25
PDATA[26]	L3	IN_{CMOS}	High	Parallel data input, Bit 26
PDATA[27]	M2	IN_{CMOS}	High	Parallel data input, Bit 27
PDATA[28]	N2	IN_{CMOS}	High	Parallel data input, Bit 28
PDATA[29]	P2	IN_{CMOS}	High	Parallel data input, Bit 29
PDATA[30]	N3	IN_{CMOS}	High	Parallel data input, Bit 30
PDATA[31]	P3	IN_{CMOS}	High	Parallel data input, Bit 31
PDATA[32]	N4	IN_{CMOS}	High	Parallel data input, Bit 32
PDATA[33]	P4	IN_{CMOS}	High	Parallel data input, Bit 33
PDATA[34]	N5	IN_{CMOS}	High	Parallel data input, Bit 34
PDATA[35]	P5	IN_{CMOS}	High	Parallel data input, Bit 35
PARITY	C6	IN_{CMOS}	High	Parity input
RDCLK	B6	OUT_{CMOS}	High	Read clock. PDATA[35..0] is registered at rising edge
VALID	N6	IN_{CMOS}	High	Data valid signal
RESET#	A6	IN_{CMOS}	Low	Asynchronous reset signal
FLAGI	M6	IN_{CMOS}	High	Set FLAG
PARGEN	N1	IN_{CMOS}	High	Generate parity internally
SYNGEN	D3	IN_{CMOS}	High	Reserved for future functionality, has to be set to '0'
PERR#	P6	OUT_{CMOS}	Low	Parity error
LOCK	C7	OUT_{CMOS}	High	PLL lock indication
OSC	A10	IN_{CMOS}		Reference clock input, 66MHz
SDATA	K12	OUT_{CML}		Differential serial high-speed CML output
SDATA#	J14	OUT_{CML}		Differential serial high-speed CML output
EXTRC1	H13			External loop filter pin1
EXTRC2	H12			External loop filter pin2
GND_D	C2, C5, F3, G2, J3, L2, M5	GND		Digital chip (CMOS) power supply GND
GND_ID	A7, P7	GND		Chip interface digital chip power supply GND
GND_IA	G6, G7, G8, G9, J6, J7, J8, J9, K7, K8	GND		Chip interface analog chip power supply GND
GND_A0	C9, C11, D10, D14, K14, L10	GND		Analog chip (Bipolar) power supply GND
GND_A1	G12, G13	GND		Analog chip (Bipolar) PLL circuit power supply ground
VCC_D	C4, F1, H1, K1, M4	VCC		Digital chip (CMOS) power supply VCC
VCC_ID	B7, N7	VCC		Chip interface digital chip power supply VCC
VCC_IA	E7, E8, E9, E10, F6, F7, F8, F9, F10, F11, H6, H7, H8, H9	VCC		Chip interface analog chip power supply VCC
VCC_A0	A11, D9, L9, L11, M9	VCC		Analog chip (Bipolar) power supply VCC
VCC_A1	H14, J11	VCC		Analog chip (Bipolar) PLL circuit power supply VCC

Table 15: GigaSTaR® INGT165B Pin Definition

INGT165B TRANSMITTER PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	N. C. ●	PDATA [6]	PDATA [4]	PDATA [2]	PDATA [0]	RESET#	GND_ID	N. C.	N. C.	OSC	VCC_A0	N. C.	N. C.	N. C.
B	PDATA [8]	PDATA [7]	PDATA [5]	PDATA [3]	PDATA [1]	RDCLK	VCC_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.
C	PDATA [9]	GND_D	N. C.	VCC_D	GND_D	PARITY	LOCK	N. C.	GND_A0	N. C.	GND_A0	N. C.	N. C.	N. C.
D	PDATA [12]	PDATA [10]	SYNGEN	N. C.	N. C.	N. C.	N. C.	N. C.	VCC_A0	GND_A0	N. C.	N. C.	N. C.	GND_A0
E	PDATA [14]	PDATA [13]	PDATA [11]	N. C.	N. C.	N. C.	VCC_IA	VCC_IA	VCC_IA	VCC_IA	N. C.	N. C.	N. C.	N. C.
F	VCC_D	PDATA [15]	GND_D	N. C.	N. C.	VCC_IA	VCC_ IA	VCC_ IA	VCC_ IA	VCC_IA	VCC_IA	N. C.	N. C.	N. C.
G	PDATA [17]	GND_D	PDATA [16]	N. C.	N. C.	GND_IA	GND_IA	GND_IA	GND_IA	N. C.	N. C.	GND_A1	GND_A1	N. C.
H	VCC_D	PDATA [19]	PDATA [18]	N. C.	N. C.	VCC_IA	VCC_ IA	VCC_ IA	VCC_ IA	N. C.	N. C.	EXTRC2	EXTRC1	VCC_A1
J	PDATA [20]	PDATA [21]	GND_D	N. C.	N. C.	GND_IA	GND_IA	GND_IA	GND_IA	N. C.	VCC_A1	N. C.	N. C.	SDATA#
K	VCC_D	PDATA [24]	PDATA [23]	N. C.	N. C.	N. C.	GND_IA	GND_IA	N. C.	N. C.	N. C.	SDATA	N. C.	GND_A0
L	PDATA [22]	GND_D	PDATA [26]	N. C.	N. C.	N. C.	N. C.	N. C.	VCC_A0	GND_A0	VCC_A0	N. C.	N. C.	N. C.
M	PDATA [25]	PDATA [27]	N.C.	VCC_D	GND_D	FLAGI	N. C.	N. C.	VCC_A0	N. C.	N. C.	N. C.	N. C.	N. C.
N	PARGEN	PDATA [28]	PDATA [30]	PDATA [32]	PDATA [34]	VALID	VCC_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.
P	N. C.	PDATA [29]	PDATA [31]	PDATA [33]	PDATA [35]	PERR#	GND_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.

Note: N.C. marked pins are not electrically connected to the dice. However, for improved thermal performance, the pins are electrically connected to each other. It is recommended to tie all N.C. pins to that supply plane with the best heat sink capability.

● Pin 1 Identifier

Figure 13: GigaSTaR® INGT165B Pin Assignments (Top View)

INGR165B RECEIVER PIN DEFINITION

Pin Name	Pin #	Direction	Active	Description
PDATA[0]	A5	OUT_{CMOS}	High	Parallel data output, Bit 0
PDATA[1]	B5	OUT_{CMOS}	High	Parallel data output, Bit 1
PDATA[2]	A4	OUT_{CMOS}	High	Parallel data output, Bit 2
PDATA[3]	B4	OUT_{CMOS}	High	Parallel data output, Bit 3
PDATA[4]	A3	OUT_{CMOS}	High	Parallel data output, Bit 4
PDATA[5]	B3	OUT_{CMOS}	High	Parallel data output, Bit 5
PDATA[6]	A2	OUT_{CMOS}	High	Parallel data output, Bit 6
PDATA[7]	B2	OUT_{CMOS}	High	Parallel data output, Bit 7
PDATA[8]	B1	OUT_{CMOS}	High	Parallel data output, Bit 8
PDATA[9]	C1	OUT_{CMOS}	High	Parallel data output, Bit 9
PDATA[10]	D2	OUT_{CMOS}	High	Parallel data output, Bit 10
PDATA[11]	E3	OUT_{CMOS}	High	Parallel data output, Bit 11
PDATA[12]	D1	OUT_{CMOS}	High	Parallel data output, Bit 12
PDATA[13]	E2	OUT_{CMOS}	High	Parallel data output, Bit 13
PDATA[14]	E1	OUT_{CMOS}	High	Parallel data output, Bit 14
PDATA[15]	F2	OUT_{CMOS}	High	Parallel data output, Bit 15
PDATA[16]	G3	OUT_{CMOS}	High	Parallel data output, Bit 16
PDATA[17]	G1	OUT_{CMOS}	High	Parallel data output, Bit 17
PDATA[18]	H3	OUT_{CMOS}	High	Parallel data output, Bit 18
PDATA[19]	H2	OUT_{CMOS}	High	Parallel data output, Bit 19
PDATA[20]	J1	OUT_{CMOS}	High	Parallel data output, Bit 20
PDATA[21]	J2	OUT_{CMOS}	High	Parallel data output, Bit 21
PDATA[22]	L1	OUT_{CMOS}	High	Parallel data output, Bit 22
PDATA[23]	K3	OUT_{CMOS}	High	Parallel data output, Bit 23
PDATA[24]	K2	OUT_{CMOS}	High	Parallel data output, Bit 24
PDATA[25]	M1	OUT_{CMOS}	High	Parallel data output, Bit 25
PDATA[26]	L3	OUT_{CMOS}	High	Parallel data output, Bit 26
PDATA[27]	M2	OUT_{CMOS}	High	Parallel data output, Bit 27
PDATA[28]	N2	OUT_{CMOS}	High	Parallel data output, Bit 28
PDATA[29]	P2	OUT_{CMOS}	High	Parallel data output, Bit 29
PDATA[30]	N3	OUT_{CMOS}	High	Parallel data output, Bit 30
PDATA[31]	P3	OUT_{CMOS}	High	Parallel data output, Bit 31
PDATA[32]	N4	OUT_{CMOS}	High	Parallel data output, Bit 32
PDATA[33]	P4	OUT_{CMOS}	High	Parallel data output, Bit 33
PDATA[34]	N5	OUT_{CMOS}	High	Parallel data output, Bit 34
PDATA[35]	P5	OUT_{CMOS}	High	Parallel data output, Bit 35
PARITY	C6	OUT_{CMOS}	High	Parity output
WRCLK	B6	OUT_{CMOS}	High	Write clock
LSYNC#	N6	OUT_{CMOS}	Low	Receiver is synchronous, link is established
RESET#	A6	IN_{CMOS}	Low	Asynchronous reset signal
FLAGO	M6	OUT_{CMOS}	High	FLAG output
PERR#	P6	OUT_{CMOS}	Low	Parity error
EQLSEL	C10	IN_{CMOS}	High	Equalizer select
LOCK	C7	OUT_{CMOS}	High	PLL lock indication
OSC	A10	IN_{CMOS}	High	Reference clock input, 66MHz
SDATA	E12	IN_{CML}		Differential serial high-speed CML input
SDATA#	E14	IN_{CML}		Differential serial high-speed CML input
EXTRC1	H13			External loop filter pin1
EXTRC2	H12			External loop filter pin2
GND_D	C2, C5, F3, G2, J3, L2, M5	GND		Digital chip (CMOS) power supply GND
GND_ID	A7, P7	GND		Chip interface digital chip power supply GND
GND_IA	G6, G7, G8, G9, J6, J7, J8, J9, K7, K8	GND		Chip interface analog chip power supply GND
GND_A0	C9, C11, D10, D14, K14, L10	GND		Analog chip (Bipolar) power supply GND
GND_A1	G12, G13	GND		Analog chip (Bipolar) PLL circuit power supply ground
VCC_D	C4, D3, F1, H1, K1, M4, N1	VCC		Digital chip (CMOS) power supply VCC
VCC_ID	B7, N7	VCC		Chip interface digital chip power supply VCC
VCC_IA	E7, E8, E9, E10, F6, F7, F8, F9, F10,F11, H6, H7, H8, H9	VCC		Chip interface analog chip power supply VCC
VCC_A0	A11, D9, L9, L11, M9	VCC		Analog chip (Bipolar) power supply VCC
VCC_A1	H14, J11	VCC		Analog chip (Bipolar) PLL circuit power supply VCC

Table 16: GigaSTaR® INGR165B Pin Definition

INGR165B RECEIVER PIN ASSIGNMENT (TOP VIEW)

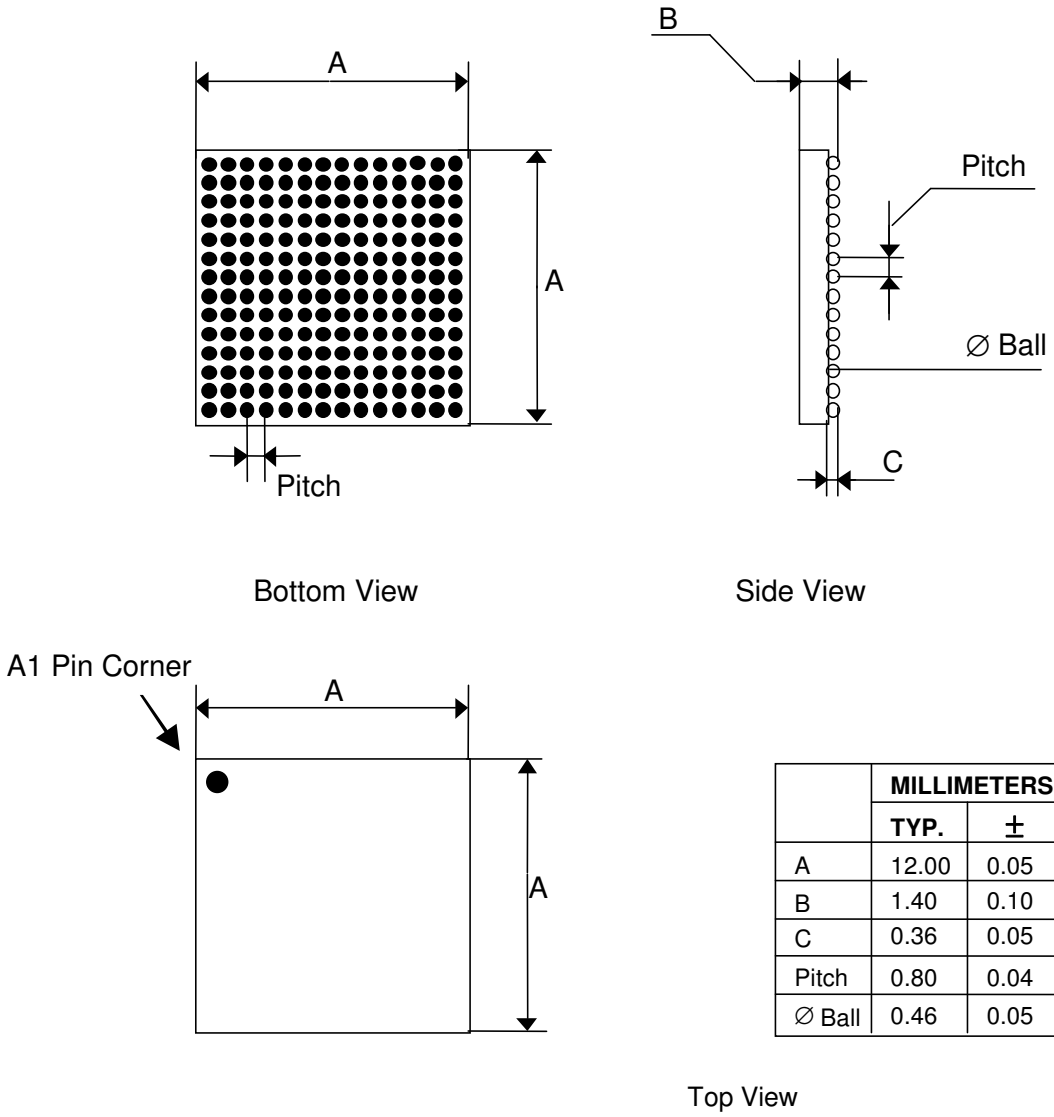
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	N. C. ●	PDATA [6]	PDATA [4]	PDATA [2]	PDATA [0]	RESET#	GND_ID	N. C.	N. C.	OSC	VCC_A0	N. C.	N. C.	N. C.
B	PDATA [8]	PDATA [7]	PDATA [5]	PDATA [3]	PDATA [1]	WRCLK	VCC_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.
C	PDATA [9]	GND_D	N. C.	VCC_D	GND_D	PARITY	LOCK	N. C.	GND_A0	EQLSEL	GND_A0	N. C.	N. C.	N. C.
D	PDATA [12]	PDATA [10]	VCC_D	N. C.	N. C.	N. C.	N. C.	N. C.	VCC_A0	GND_A0	N. C.	N. C.	N. C.	GND_A0
E	PDATA [14]	PDATA [13]	PDATA [11]	N. C.	N. C.	N. C.	VCC_IA	VCC_IA	VCC_IA	VCC_IA	N. C.	SDATA	N. C.	SDATA#
F	VCC_D	PDATA [15]	GND_D	N. C.	N. C.	VCC_IA	VCC_IA	VCC_IA	VCC_IA	VCC_IA	VCC_IA	N. C.	N. C.	N. C.
G	PDATA [17]	GND_D	PDATA [16]	N. C.	N. C.	GND_IA	GND_IA	GND_IA	GND_IA	N. C.	N. C.	GND_A1	GND_A1	N. C.
H	VCC_D	PDATA [19]	PDATA [18]	N. C.	N. C.	VCC_IA	VCC_IA	VCC_IA	VCC_IA	N. C.	N. C.	EXTRC2	EXTRC1	VCC_A1
J	PDATA [20]	PDATA [21]	GND_D	N. C.	N. C.	GND_IA	GND_IA	GND_IA	GND_IA	N. C.	VCC_A1	N. C.	N. C.	N. C.
K	VCC_D	PDATA [24]	PDATA [23]	N. C.	N. C.	N. C.	GND_IA	GND_IA	N. C.	N. C.	N. C.	N. C.	N. C.	GND_A0
L	PDATA [22]	GND_D	PDATA [26]	N. C.	N. C.	N. C.	N. C.	N. C.	VCC_A0	GND_A0	VCC_A0	N. C.	N. C.	N. C.
M	PDATA [25]	PDATA [27]	N.C.	VCC_D	GND_D	FLAGO	N. C.	N. C.	VCC_A0	N. C.	N. C.	N. C.	N. C.	N. C.
N	VCC_D	PDATA [28]	PDATA [30]	PDATA [32]	PDATA [34]	LSYNC#	VCC_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.
P	N. C.	PDATA [29]	PDATA [31]	PDATA [33]	PDATA [35]	PERR#	GND_ID	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.	N. C.

Note: N.C. marked pins are not electrically connected to the dice. However, for improved thermal performance, the pins are electrically connected to each other. It is recommended to tie all N.C. pins to that supply plane with the best heat sink capability.

● Pin 1 Identifier

Figure 14: GigaSTaR® INGR165B Pin Assignments (Top View)

4.4 PACKAGE DIMENSIONS (12MM X 12MM PBGA)



	MILLIMETERS	
	TYP.	±
A	12.00	0.05
B	1.40	0.10
C	0.36	0.05
Pitch	0.80	0.04
∅ Ball	0.46	0.05

Figure 15: Package Dimensions

4.5 PACKAGE HANDLING PRECAUTIONS

BGA packages are moisture-sensitive and are delivered in sealed dry packs.
The devices presented in this datasheet meet JEDEC standard 22A113B, Level 3.

Handling precautions are:

1. Shelf life in sealed dry pack : 12 months at < 40° C and < 90% RH
2. After the dry pack is opened, devices that will undergo infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220° C, maximum peak temperature package exposure time 10 sec) must be:
   a) mounted within 168 hrs at factory conditions of <=30° C / 60% RH, or
   b) stored at <= 20% RH or
   c) be baked less than 168 hrs before undergoing infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220° C)
3. If baking is required, devices may be baked for :
   a) 192 hours at 40° C + 5° C / -0° C and < 5% RH
   b) 24 hours at 125° C + 5° C / -5° C (for baking above 130° C, high-temperature trays are required)
4. Precautions have to be taken against exposure of the device terminals to electrostatic discharge stress
5. The maximum ratings may not be exceeded at any time
6. At power-up and power-down sequences, all supply voltage nodes have to be ramped up and down with identical voltage ramping, otherwise the maximum rating of I_D (I/O Current DC or transient per pin) can be exceeded and damage to the device may occur.

4.6 ORDERING CODE AND PRODUCTION STATUS INFORMATION

Ordering Code	Delivery package, minimum packing quantity (MPQ)	Production Status
INGT165B	Tray (in sealed dry pack); MPQ = 189 units	full production
INGR165B	Tray (in sealed dry pack); MPQ = 189 units	full production
INGSK	Sample Kit (in sealed dry pack); Box containing 2 x INGT165B and 2 x INGR165B	full production
ING_TRC	Piggyback Board w/ INGT165B and INGR165B, SUB D9 connector for cable data transmission Box; MPQ = 10 units	full production
ING_TRF	Piggyback Board w/ INGT165B and INGR165B with fiber optic module Box; MPQ = 10 units	full production
ING_TTC	Piggyback Board with two INGT165B, SUB D9 connector for cable data transmission Box; MPQ = 10 units	full production
ING_RRC	Piggyback Board with two INGR165B, SUB D9 connector for cable data transmission Box; MPQ = 10 units	full production

Table 17: Product Availability

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