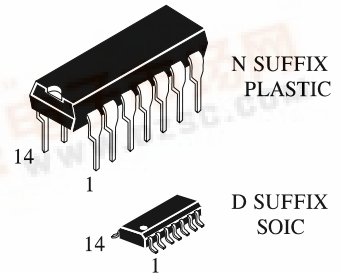


# IN74HC10

## TRIPLE 3-INPUT NAND GATE High-Performance Silicon-Gate CMOS

The IN74HC10 is identical in pinout to the LS/ALS10. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



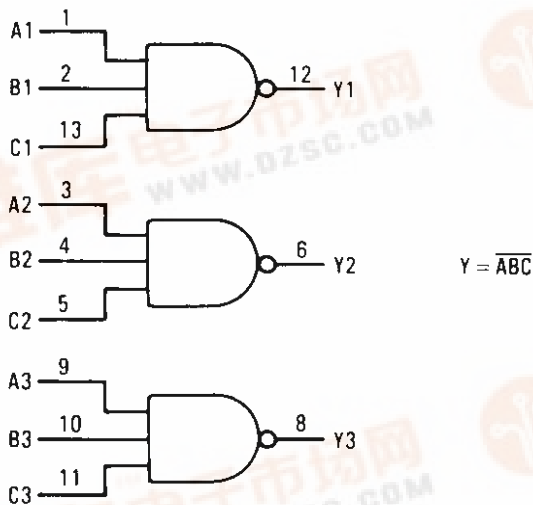
### ORDERING INFORMATION

IN74HC10N Plastic

IN74HC10D SOIC

$T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



$$Y = \overline{ABC}$$

PIN 14 =  $V_{CC}$   
PIN 7 = GND

### PIN ASSIGNMENT

A1	1	14	$V_{CC}$
B1	2	13	C1
A2	3	12	Y1
B2	4	11	C3
C2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

### FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

X = don't care

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### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 4.5$ V	0	1000	
	$V_{CC} = 2.0$ V	0	500	
	$V_{CC} = 6.0$ V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

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### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> =V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	2.0	20	40	μA

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## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125° C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A,B or C to Output Y (Figures 1 and 2)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{IN}$	Maximum Input Capacitance	-	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate)	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	25			

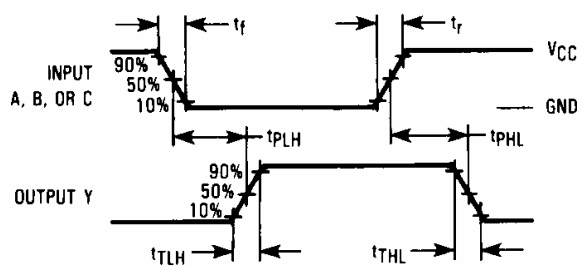
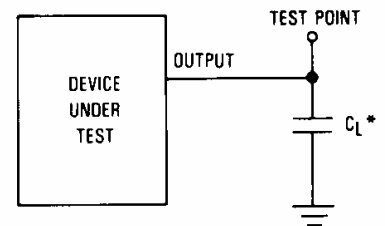


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/3 of the Device)

