



IPB80N08S2L-07

IPP80N08S2L-07

**OptiMOS® Power-Transistor**

**Features**

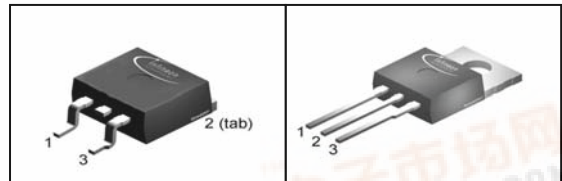
- N-channel Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

**Product Summary**

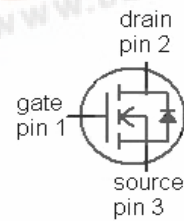
$V_{DS}$	75	V
$R_{DS(on),max}$ (SMD version)	6.8	mΩ
$I_D$	80	A

PG-TO263-3-2

PG-TO220-3-1



Type	Package	Ordering Code	Marking
IPB80N08S2L-07	PG-TO263-3-2	SP0002-19051	2N08L07
IPP80N08S2L-07	PG-TO220-3-1	SP0002-19050	2N08L07



**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$	80	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{2)}$	80	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	320	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=80\text{ A}$	810	mJ
Gate source voltage <sup>4)</sup>	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... +175	°C



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics<sup>2)</sup>**

Thermal resistance, junction - case	$R_{thJC}$		-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$		-	-	62	
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>5)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	75	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=80\text{ A},$ SMD version	-	6.6	9	m $\Omega$
		$V_{GS}=4.5\text{ V}, I_D=80\text{ A},$ SMD version	-	6.3	8.7	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=80\text{ A},$	-	5.1	7.1	m $\Omega$
		$V_{GS}=10\text{ V}, I_D=80\text{ A},$ SMD version	-	4.8	6.8	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	5400	-	pF
Output capacitance	$C_{oss}$		-	1300	-	
Reverse transfer capacitance	$C_{rss}$		-	590	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=1.1\ \Omega$	-	19	-	ns
Rise time	$t_r$		-	55	-	
Turn-off delay time	$t_{d(off)}$		-	85	-	
Fall time	$t_f$		-	21	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=60\text{ V}, I_D=80\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	18	23	nC
Gate to drain charge	$Q_{gd}$		-	69	83	
Gate charge total	$Q_g$		-	183	233	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	80	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	320	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	95	120	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	240	300	nC

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 0.5\text{K/W}$  the chip is able to carry 135A at 25°C. For detailed information see Application Note ANPS071E at [www.infineon.com/optimos](http://www.infineon.com/optimos)

<sup>2)</sup> Defined by design. Not subject to production test.

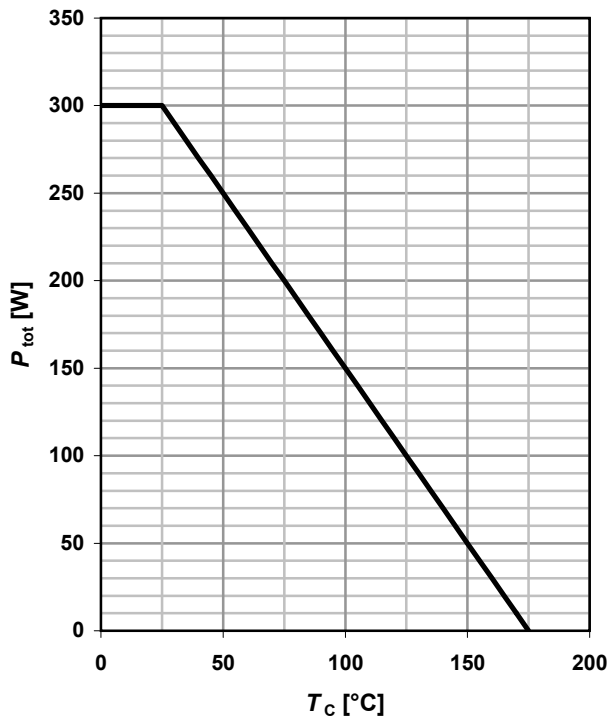
<sup>3)</sup> See diagram 13

<sup>4)</sup> Qualified at -20V and +20V.

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

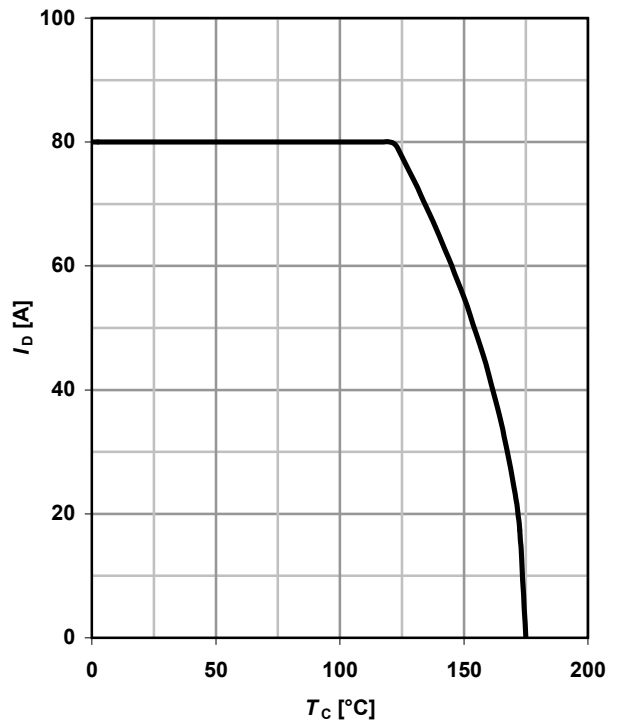
**1 Power dissipation**

$P_{tot} = f(T_C); V_{GS} \geq 4 \text{ V}$



**2 Drain current**

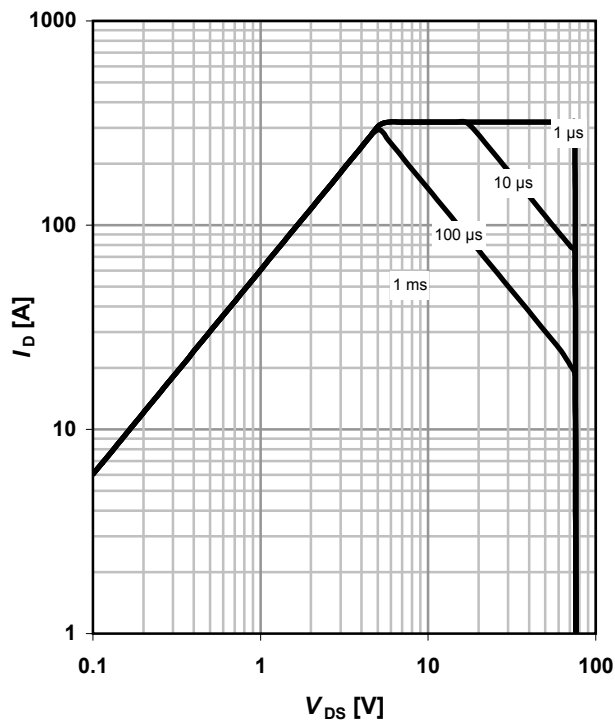
$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$



**3 Safe operating area**

$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$

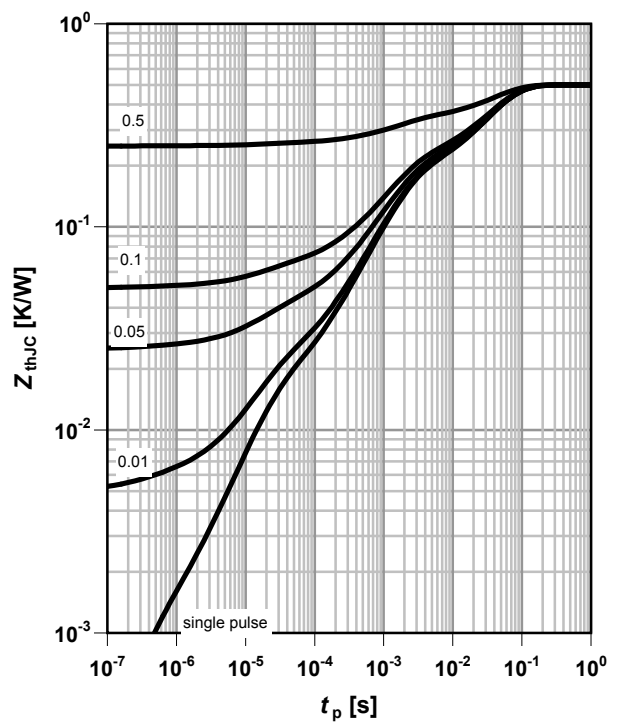
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC} = f(t_p)$

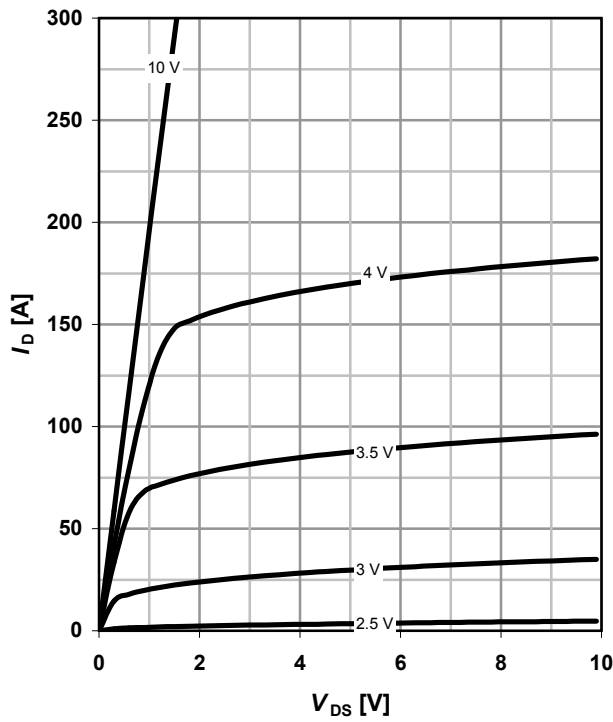
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

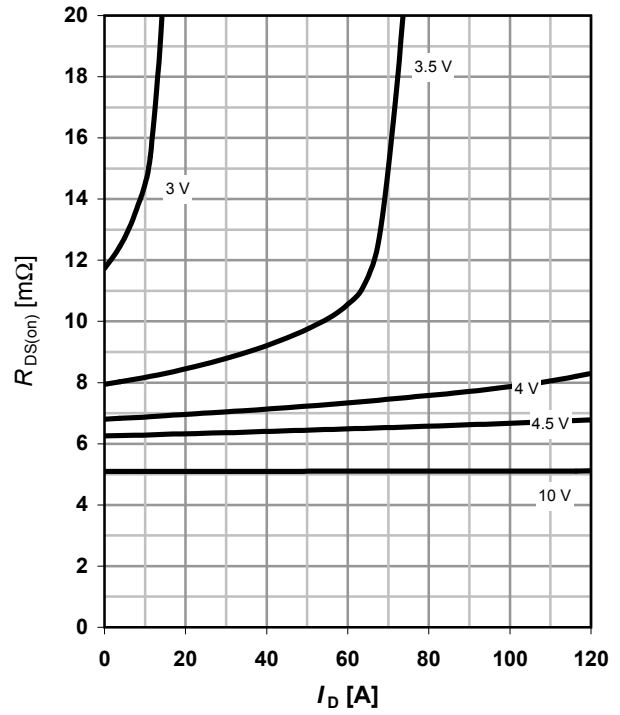
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

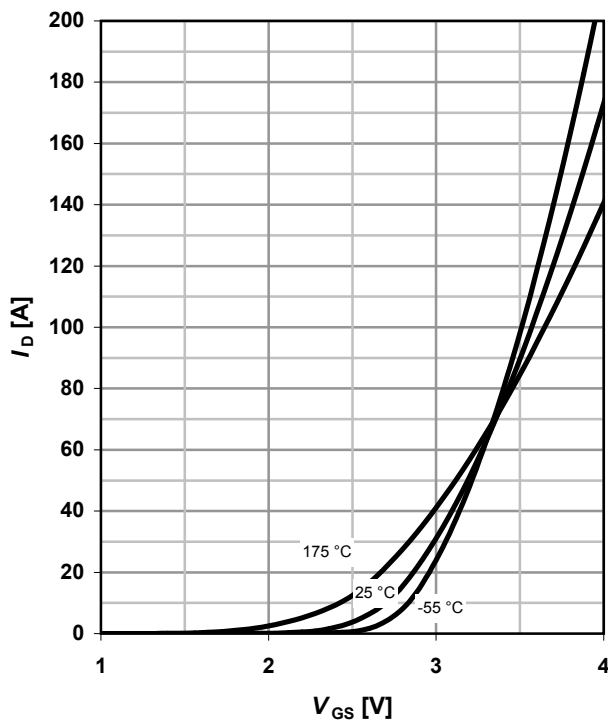
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

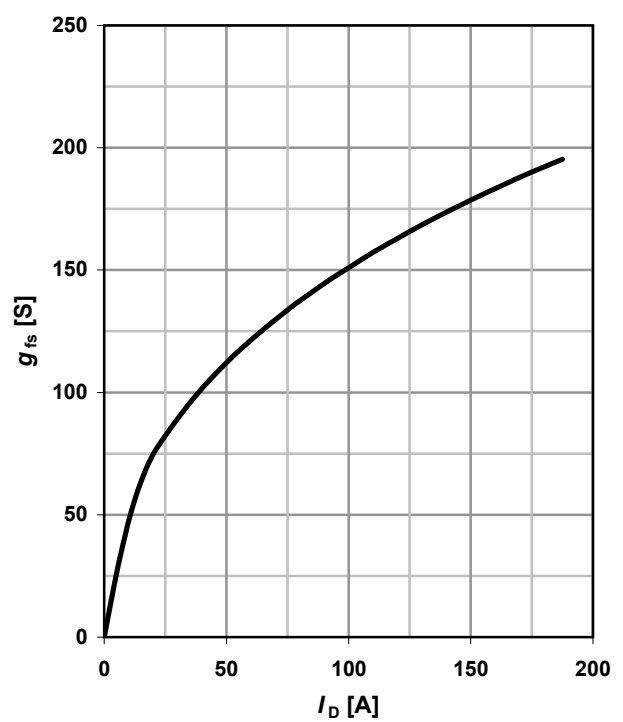
parameter:  $T_j$



**8 Typ. Forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

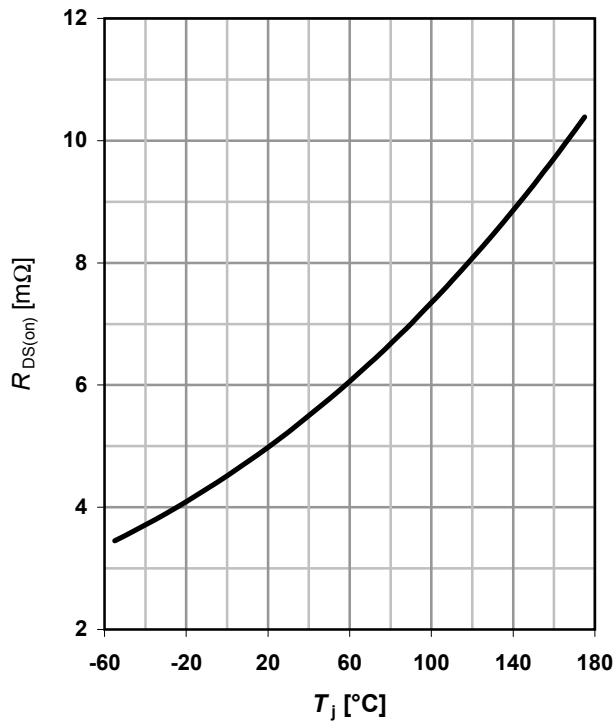
parameter:  $g_{fs}$



**9 Typ. Drain-source on-state resistance**

$$R_{DS(ON)} = f(T_j)$$

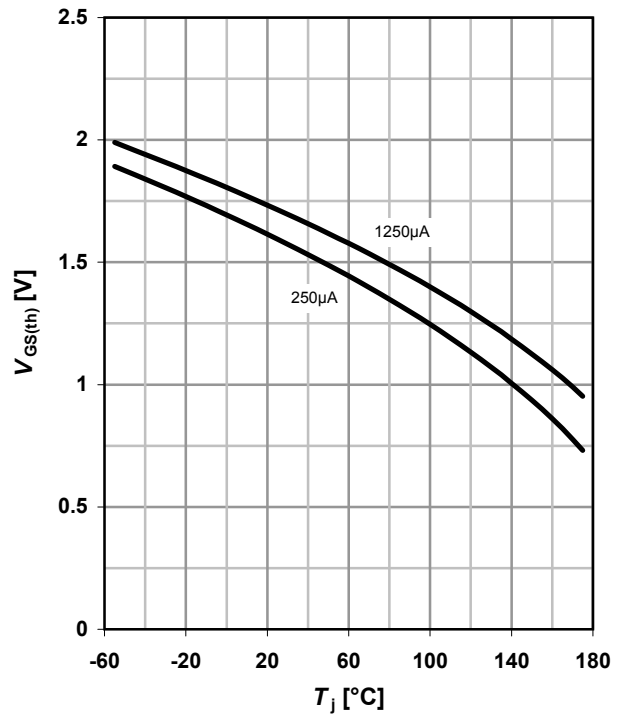
parameter:  $I_D = 80\text{ A}$ ;  $V_{GS} = 10\text{ V}$



**10 Typ. gate threshold voltage**

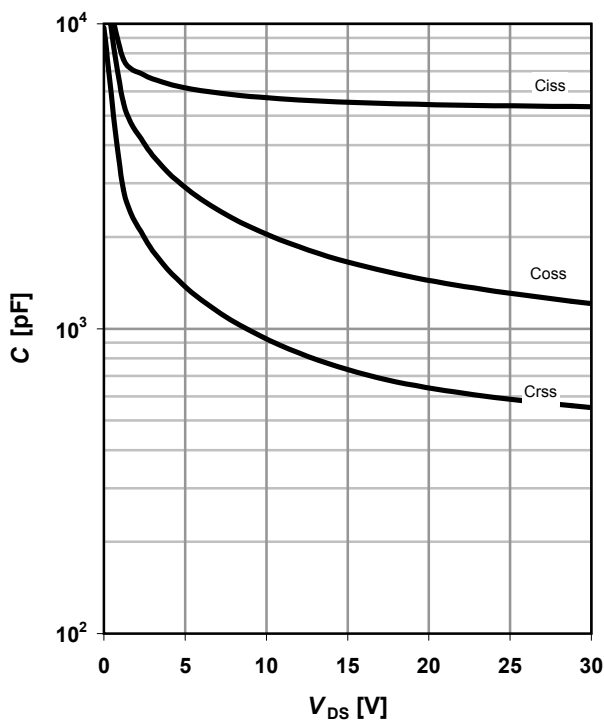
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$



**11 Typ. capacitances**

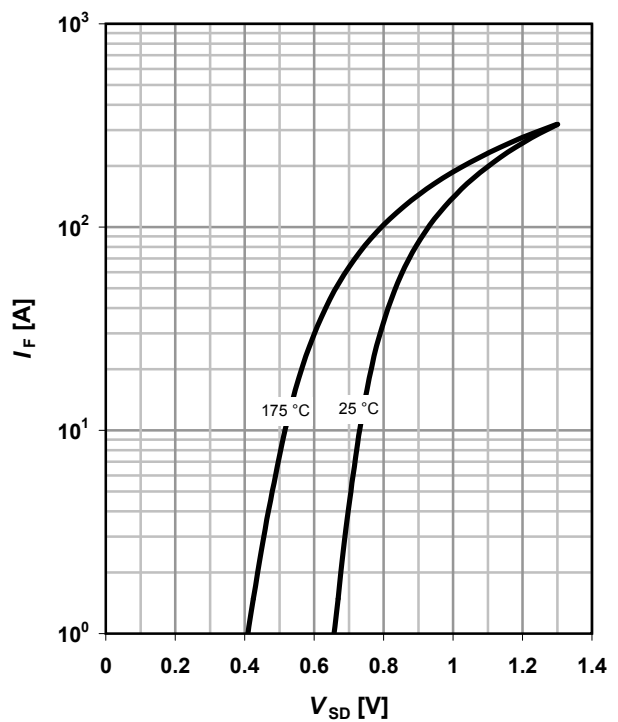
$$C = f(V_{DS}); V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$



**12 Typical forward diode characteristics**

$$I_F = f(V_{SD})$$

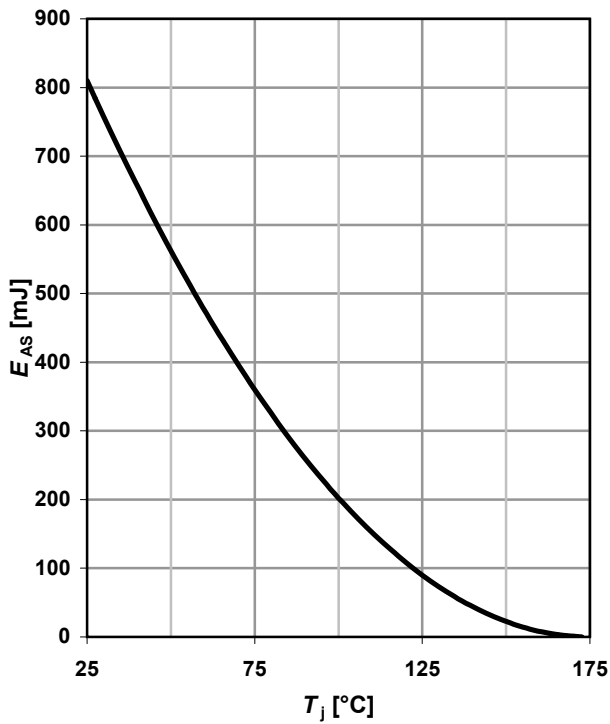
parameter:  $T_j$



**13 Typical avalanche energy**

$$E_{AS} = f(T_j)$$

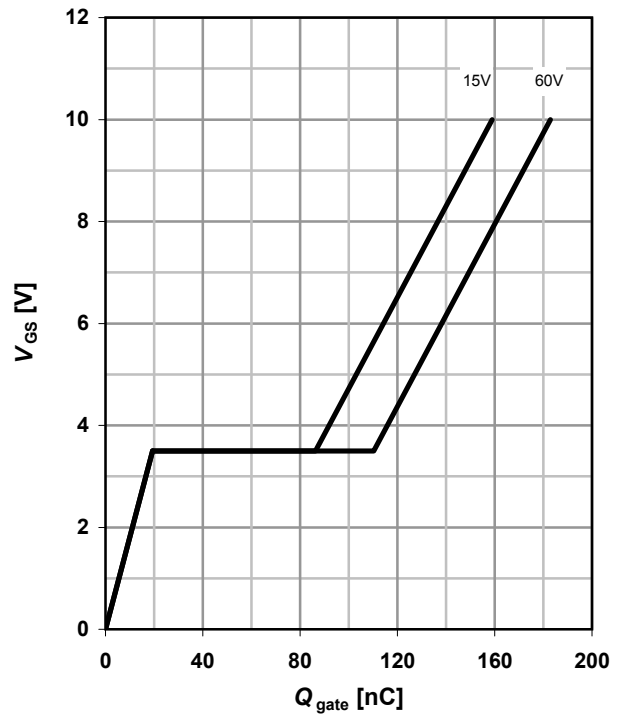
parameter:  $I_D = 80A$



**14 Typ. gate charge**

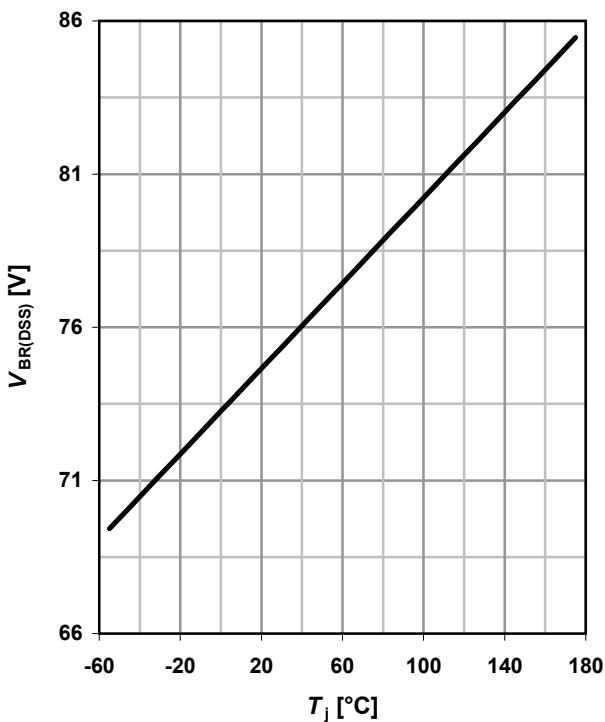
$$V_{GS} = f(Q_{gate}); I_D = 80 A \text{ pulsed}$$

parameter:  $V_{DD}$

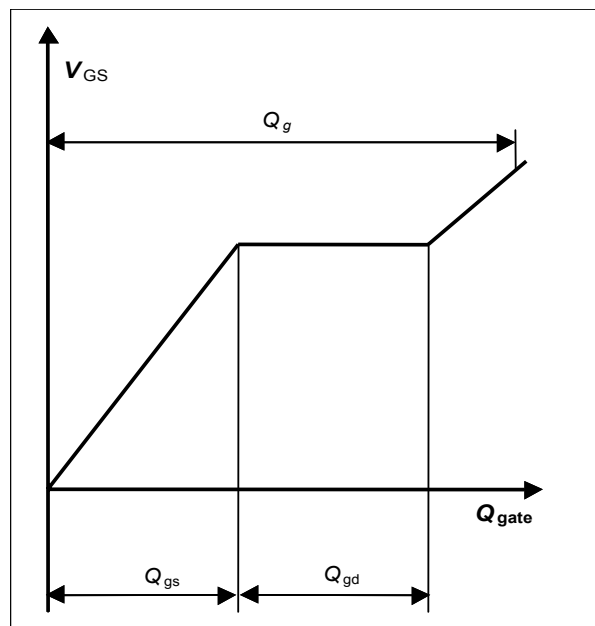


**15 Typ. drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_D = 1 mA$$



**16 Gate charge waveforms**





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