PD-97270 RevA

International
IOR Rectifier

Integrated Power Hybrid IC for
Low Voltage Motor Applications

IRAM136-3023B
iMOTION™ Series
30A, 150V
with Internal Shunt Resistor

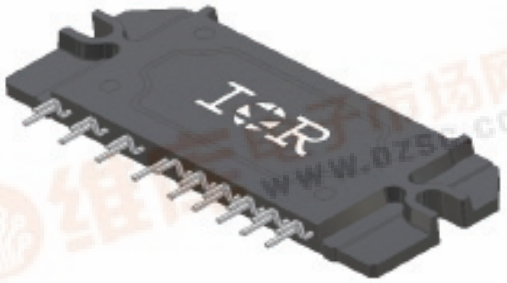
Description

International Rectifier's IRAM136-3023B is a 30A, 150V Integrated Power Hybrid IC with Internal Shunt Resistor for low voltage Motor Drives applications such as electric vehicles, portable power tools and light industrial applications. IR's technology offers an extremely compact, high performance AC motor-driver in a single isolated package to simplify design.

This advanced HIC is a combination of IR's low $R_{DS(on)}$ Advance Planar MOSFET Super Rugged technology and the industry benchmark 3-Phase high voltage, high speed driver in a fully isolated thermally enhanced package. A built-in temperature monitor and over-current and over-temperature protections and integrated under-voltage lockout function, deliver high level of protection and fail-safe operation. Using a new developed single in line package (SiP3) with heat spreader for the power die along with full transfer mold structure minimizes PCB space and resolves isolation problems to heatsink.

Features

- Integrated Gate Drivers
- Temperature Monitor and Protection
- Overcurrent shutdown
- Low R_{DS}(on) Advance Planar Super Rugged Technology
- Undervoltage lockout for all channels
- Matched propagation delay for all channels
- 5V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Lower di/dt gate driver for better noise immunity
- Motor Power up to 4.0kW / 48~100 Vdc
- Fully Isolated Package, Isolation 2000V_{RMS} min

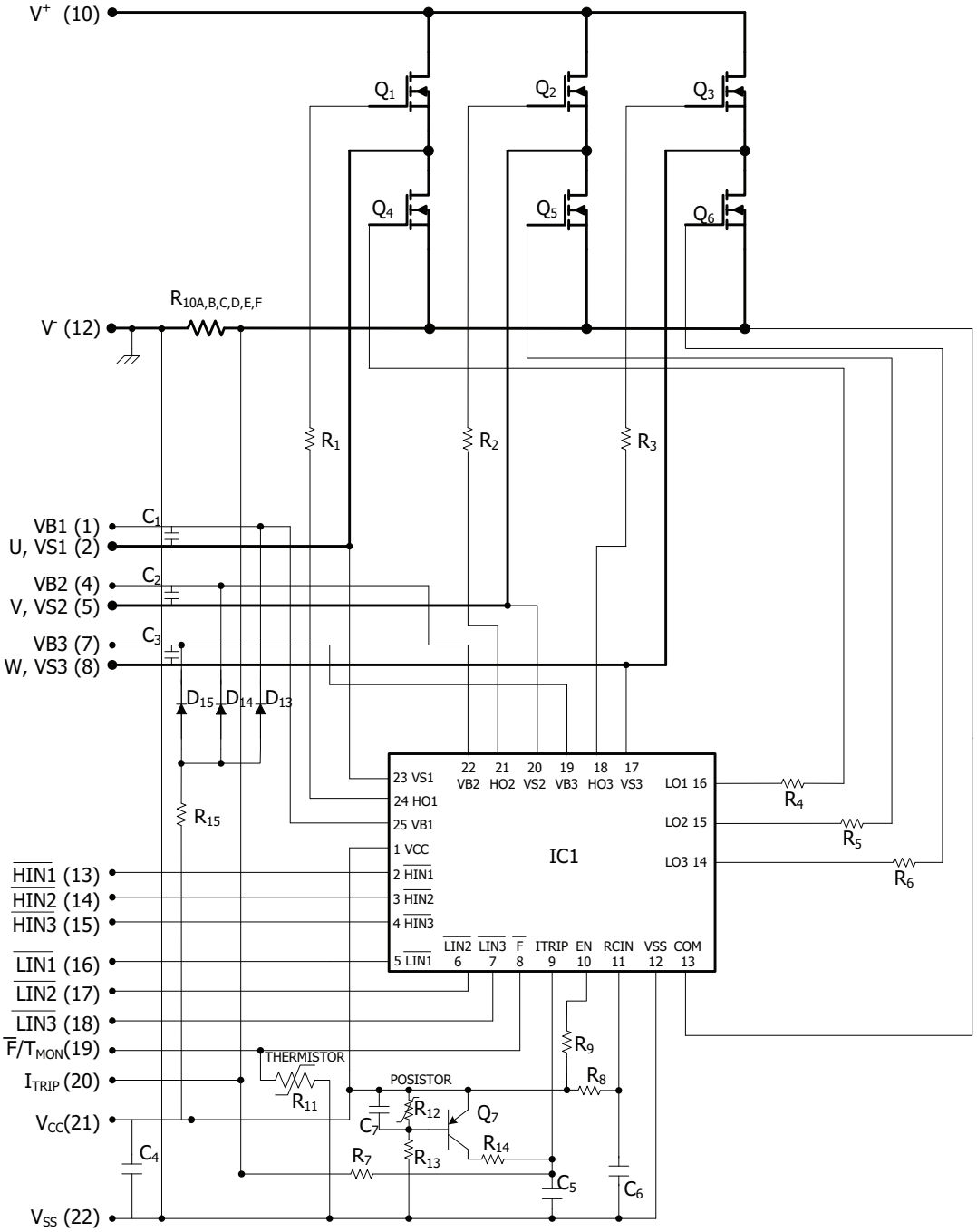


Absolute Maximum Ratings

Parameter	Description	Value	Units
$V_{BR(DSS)}$	MOSFET Blocking Voltage	150	V
V^+	Positive Bus Input Voltage	100	
I_O @ T_C=25°C	RMS Phase Current (Note 1)	30	A
I_O @ T_C=100°C	RMS Phase Current (Note 1)	15	
I_O	Pulsed RMS Phase Current (Note 1 and 2)	56	
F_{PWM}	PWM Carrier Frequency	20	kHz
P_D	Power Dissipation per MOSFET @ T_C =25°C	89	W
V_{ISO}	Isolation Voltage (1min)	2000	V_{RMS}
T_J (MOSFET & IC)	Maximum Operating Junction Temperature	+150	°C
T_C	Operating Case Temperature Range	-20 to +100	
T_{STG}	Storage Temperature Range	-40 to +125	
T	Mounting Torque (M4 screw)	0.7 to 1.17	Nm

Note 1: Sinusoidal modulation at V^+=100V, T_J=150°C, F_{PWM}=20kHz, modulation depth=0.8, pf=0.6, see Figure 3
Note 2: t_P<100ms; T_C=25°C; F_{PWM}=20kHz, limited by $I_{BUS-TRIP}$, see Table "Inverter Section Electrical Characteristics"

Internal Electrical Schematic – IRAM136-3023B



Absolute Maximum Ratings (Continued)

Symbol	Parameter	Min	Max	Units	Conditions
I_{BDF}	Bootstrap Diode Peak Forward Current	---	4.5	A	t_P= 10ms, T_J = 150°C, T_C=100°C
$P_{BR\ Peak}$	Bootstrap Resistor Peak Power (Single Pulse)	---	25.0	W	t_P=100µs, T_C =100°C
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ +0.3	V	
$V_{B1,2,3}$	High side floating supply voltage	-0.3	150	V	
V_{CC}	Low Side and logic fixed supply voltage	-0.3	20	V	
V_{IN}	Input voltage LIN, HIN, I_{Trip}	-0.3	Lower of (V_{SS}+15V) or V_{CC}+0.3V	V	

Inverter Section Electrical Characteristics @T_J= 25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	---	---	V	V_{IN}=5V, I_D=250µA
$\Delta V_{(BR)DSS}$ / ΔT	Temperature Coeff. Of Breakdown Voltage	---	0.16	---	V/°C	V_{IN}=5V, I_D=1.0mA (25°C - 150°C)
$R_{DS(ON)}$	Drain-to-Source On Resistance	---	38	80	mΩ	I_D=15A, V_{CC}=15V
		---	65	122		I_D=15A, V_{CC}=15V, T_J=125°C
I_{DSS}	Zero Gate Voltage Drain Current	---	3	80	µA	V_{IN}=5V, V^+=150V
		---	8	---		V_{IN}=5V, V^+=150V, T_J=125°C
V_{SD}	Body Diode Forward Voltage Drop	---	1.2	1.9	V	I_D=15A
		---	1.0	1.8		I_D=15A, T_J=125°C
V_{BDFM}	Bootstrap Diode Forward Voltage Drop	--	--	1.25	V	I_F=1A
		---	---	1.10		I_F=1A, T_J=125°C
R_{BR}	Bootstrap Resistor Value	---	22	---	Ω	T_J=25°C
$\Delta R_{BR}/R_{BR}$	Bootstrap Resistor Tolerance	---	---	±5	%	T_J=25°C
I_{BUS_TRIP}	Current Protection Threshold (positive going)	56	---	68	A	See Figure 2

Inverter Section Switching Characteristics @ T_J= 25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
E_{ON}	Turn-On Switching Loss[1/]	---	395	1100	µJ	I_D=15A, V^+=100V V_{CC}=15V, L=2mH Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-Off Switching Loss[1/]	---	135	250		
E_{TOT}	Total Switching Loss[1/]	---	530	1350		
E_{REC}	Diode Reverse Recovery energy[1/]	---	210	1000		
t_{RR}	Diode Reverse Recovery time[1/]	---	240	---	ns	
E_{ON}	Turn-on Swtiching Loss[1/]	---	360	970	µJ	I_D=15A, V^+=100V V_{CC}=15V, L=2mH, T_J=125°C Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-off Switching Loss[1/]	---	115	210		
E_{TOT}	Total Switching Loss[1/]	---	475	1180		
E_{REC}	Diode Reverse Recovery energy[1/]	---	230	1000		
t_{RR}	Diode Reverse Recovery time[1/]	---	270	---	ns	
Q_G	Turn-On FET Gate Charge[1/]	---	60	89	nC	I_D=36A, V^+=75V, V_{GS}=10V
E_{AS}	Single Pulse Avalanche Energy	---	---	470	mJ	Note 3, 4
I_{AR}	Avalanche Current	---	---	36	A	Repetitive rating; pulse width limited by max. junction temperature. (Note 4)
E_{AR}	Repetitive Avalanche Energy	---	---	32	mJ	

Note 3: Starting T_J = 25°C, L = 0.72mH, R_G = 25Ω, I_{AS} = 36A

Note 4: This is only applied to TO-220AB package

[1/] Based on Characterization Data only. Not subject to production test.

Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM/I_{TRIP}. The V_S offset is tested with all supplies biased at 15V differential (Note 5).

Symbol	Definition	Min	Max	Units
$V_{B1,2,3}$	High side floating supply voltage	V_S+10	V_S+20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 6	150	
V_{CC}	Low side and logic fixed supply voltage	12	20	V
V_{IN}	Logic input voltage LIN, HIN	V_{SS}	V_{SS}+5	V

Note 5: For more details, see IR2136 data sheet

Note 6: Logic operational for V_s from COM-5V to COM+150V. Logic state held for V_s from COM-5V to COM-V_{BS}. (please refer to DT97-3 for more details)

Static Electrical Characteristics Driver Function @ T_J= 25°C

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$)=15V, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (Static Electrical Characteristics are Based on Driver IC Data Sheet, Note 5).

Symbol	Definition	Min	Typ	Max	Units
V_{IH}	Logic "0" input voltage	3.0	---	---	V
V_{IL}	Logic "1" input voltage	---	---	0.8	V
V_{CCUV+}, V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V
V_{CCUV-}, V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V
V_{CCUVH}, V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lock-out hysteresis	0.3	0.7	---	V
$V_{IN,Clamp}$	Input Clamp Voltage (HIN, LIN, T/I_{TRIP}) I_{IN}=10µA	4.9	5.2	5.5	V
I_{QBS}	Quiescent V_{BS} supply current V_{IN}=0V	---	---	165	µA
I_{QCC}	Quiescent V_{CC} supply current V_{IN}=0V	---	---	3.35	mA
I_{LK}	Offset Supply Leakage Current	---	---	60	µA
I_{IN+}	Input bias current V_{IN}=5V	---	200	300	µA
I_{IN-}	Input bias current V_{IN}=0V	---	100	220	µA
I_{TRIP+}	I_{TRIP} bias current V_{ITRIP}=5V	---	30	100	µA
I_{TRIP-}	I_{TRIP} bias current V_{ITRIP}=0V	---	0	1	µA
V(I_{TRIP})	I_{TRIP} threshold Voltage	440	490	540	mV
V(I_{TRIP},HYS)	I_{TRIP} Input Hysteresis	---	70	---	mV

Dynamic Electrical Characteristics @ T_J= 25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output propagation turn-on delay time (see fig.11)[2/]	---	0.83	---	µs	V_{CC}=V_{BS}= 15V, I_D=30A, V^+=100V
T_{OFF}	Input to Output propagation turn-off delay time (see fig. 11)[2/]	---	1.08	---	µs	
T_{FLIN}	Input Filter time (HIN, LIN)[3/]	100	200	---	ns	V_{IN}=0 & V_{IN}=5V
$T_{BLT-Trip}$	I_{TRIP} Blancking Time[3/]	100	150	---	ns	V_{IN}=0 & V_{IN}=5V
D_T	Dead Time (V_{BS}=V_{DD}=15V)[3/]	220	290	360	ns	V_{BS}=V_{CC}=15V
M_T	Matching Propagation Delay Time (On & Off)[3/]	---	40	75	ns	V_{CC}= V_{BS}= 15V, external dead time> 400ns
T_{ITrip}	I_{Trip} to six switch to turn-off propagation delay (see fig. 2)[4/]	---	3.2	---	µs	V_{CC}=V_{BS}= 15V, I_D=30A, V^+=100V
$T_{FLT-CLR}$	Post I_{Trip} to six switch to turn-off clear time (see fig. 2)[4/]	---	7.7	---	ms	T_C = 25°C
		---	6.7	---		T_C = 100°C

[2/] Based on Characterization Data only. Not subject to production test.

[3/] Based on Driver IC Data Sheet.

[4/] Verified by Design. Not subject to production test.

Thermal and Mechanical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{th(J-C)}$	Thermal resistance, FET[5/]	---	1.2	1.4	°C/W	Flat, greased surface. Heatsink compound thermal conductivity 1W/m°K
$R_{th(C-S)}$	Thermal resistance, C-S[5/]	---	0.1	---		
C_D	Creepage Distance	3.5	---	---	mm	See outline Drawings

[5/] Based on Characterization Data only. Not subject to production test.

Internal Current Sensing Resistor - Shunt Characteristics

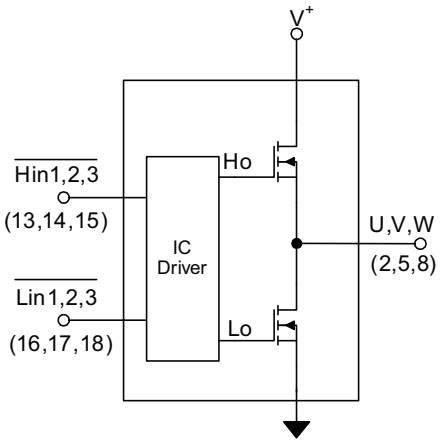
Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{Shunt}	Resistance	8.1	8.3	8.5	mΩ	T_C = 25°C
T_{Coeff}	Temperature Coefficient	0	---	200	ppm/°C	
P_{Shunt}	Power Dissipation	---	---	4.5	W	-40°C< T_C <100°C
T_{Range}	Temperature Range	-20	---	125	°C	

Internal NTC - Thermistor Characteristics

Parameter	Definition	Min	Typ	Max	Units	Conditions
R_{25}	Resistance	97	100	103	kΩ	T_C = 25°C
R_{125}	Resistance[6/]	2.25	2.52	2.80	kΩ	T_C = 125°C
B	B-constant (25-50°C)[6/]	4165	4250	4335	k	$R_2 = R_1 e^{[B(1/T2 - 1/T1)]}$
Temperature Range		-20	---	125	°C	
Typ. Dissipation constant		---	1	---	mW/°C	T_C = 25°C

[6/] Verified by Design. Not subject to production test.

Input-Output Logic Level Table



I_{TRIP}	$\overline{HIN1,2,3}$	$\overline{LIN1,2,3}$	U,V,W
0	0	1	V^+
0	1	0	0
0	1	1	X
1	X	X	X

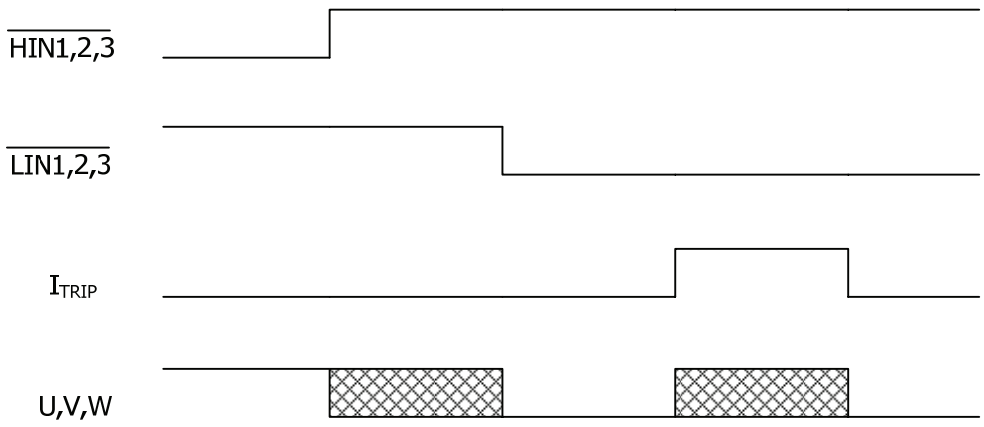


Figure 1. Input/Output Timing Diagram

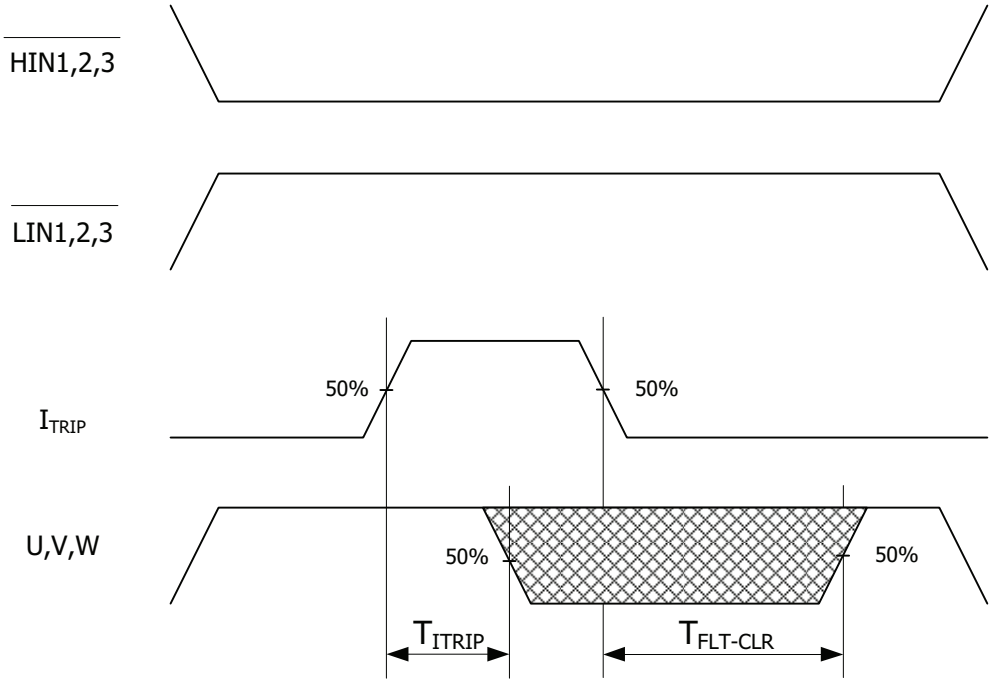
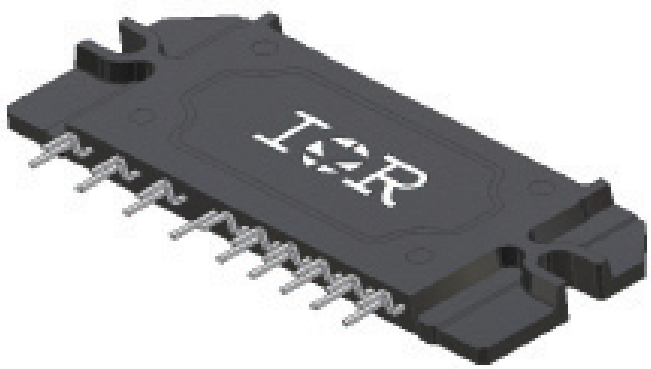


Figure 2. I_{TRIP} Timing Waveform

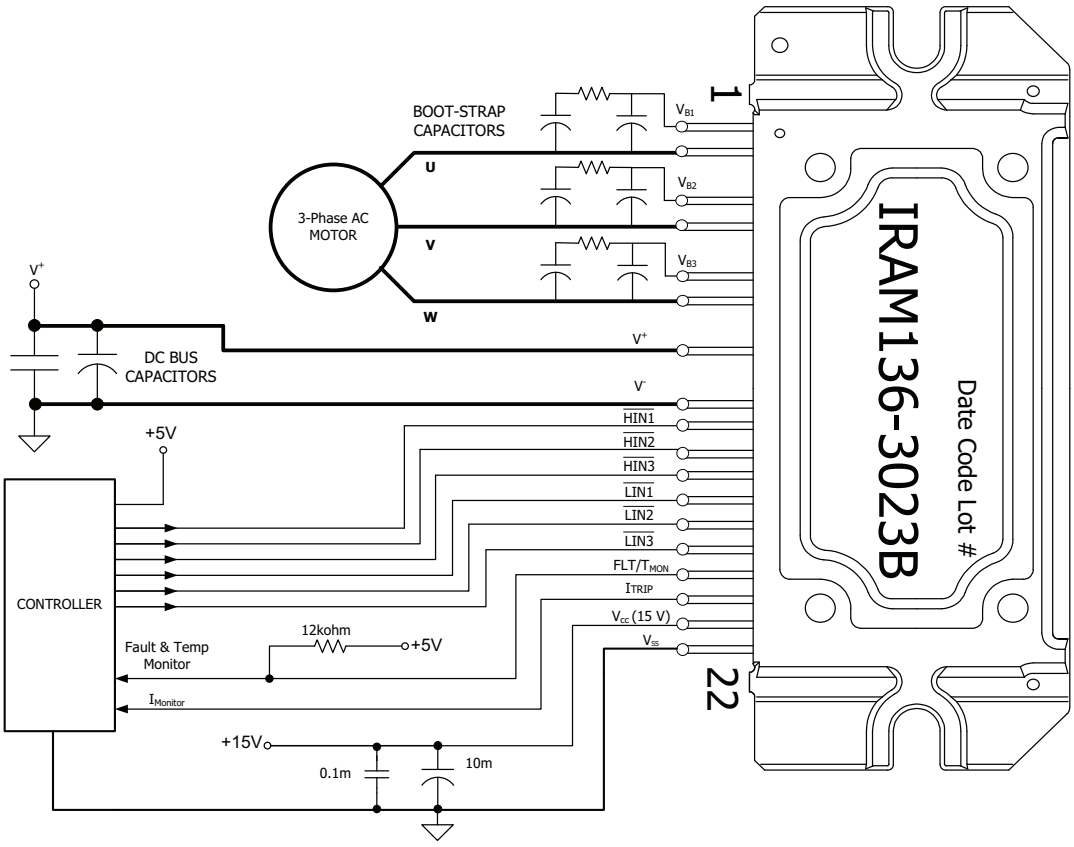
Note 7: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

Module Pin-Out Description

Pin	Name	Description
1	V_{B1}	High Side Floating Supply Voltage 1
2	U, V_{S1}	Output 1 - High Side Floating Supply Offset Voltage
3	NA	none
4	V_{B2}	High Side Floating Supply voltage 2
5	V,V_{S2}	Output 2 - High Side Floating Supply Offset Voltage
6	NA	none
7	V_{B3}	High Side Floating Supply voltage 3
8	W,V_{S3}	Output 3 - High Side Floating Supply Offset Voltage
9	NA	none
10	V^+	Positive Bus Input Voltage
11	NA	none
12	V-	Negative Bus Input Voltage
13	$\overline{H_{IN1}}$	Logic Input High Side Gate Driver - Phase 1
14	$\overline{H_{IN2}}$	Logic Input High Side Gate Driver - Phase 2
15	$\overline{H_{IN3}}$	Logic Input High Side Gate Driver - Phase 3
16	$\overline{L_{IN1}}$	Logic Input Low Side Gate Driver - Phase 1
17	$\overline{L_{IN2}}$	Logic Input Low Side Gate Driver - Phase 2
18	$\overline{L_{IN3}}$	Logic Input Low Side Gate Driver - Phase 3
19	$\overline{Fault}/T_{MON}$	Temperature Monitor and Fault Function
20	I_{Sense}	Current Monitor
21	V_{CC}	+15V Main Supply
22	V_{SS}	Negative Main Supply



Typical Application Connection IRAM136-3023B



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide good decoupling between VCC-VSS and VB1,2,3-VS1,2,3 terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are strongly recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9. Bootstrap capacitor value must be selected to limit the power dissipation of the internal resistor in series with the VCC. (see maximum ratings Table on page 3).
4. After approx. 8ms the FAULT is reset. (see Dynamic Characteristics Table on page 5).
5. PWM generator must be disabled within Fault duration to guarantee shutdown of the system, overcurrent condition must be cleared before resuming operation.
6. Fault/T_{MON} Monitor pin must be pulled-up to +5V.

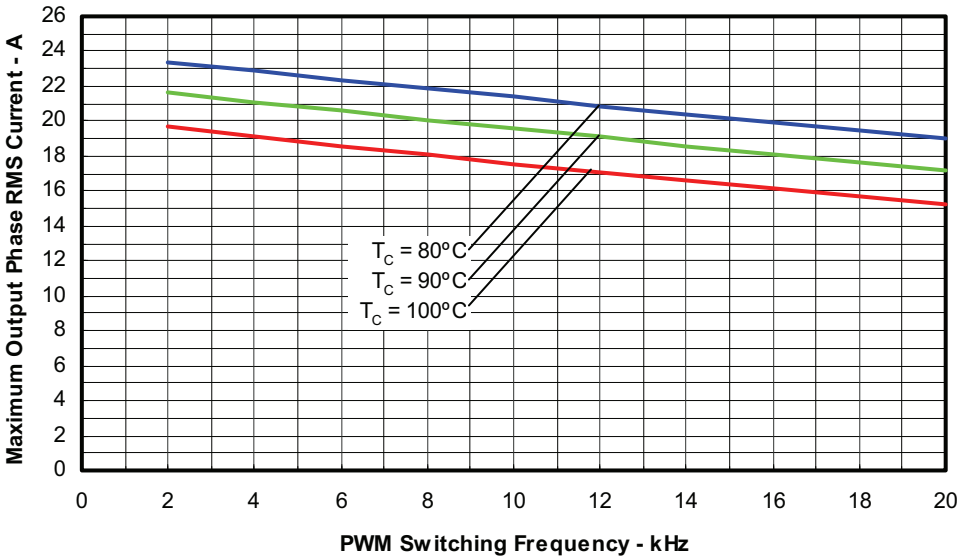


Figure 3. Maximum Sinusoidal Phase Current vs. PWM Switching Frequency
Sinusoidal Modulation, V^+=100V, T_J=150°C, Modulation Depth=0.8, PF=0.6

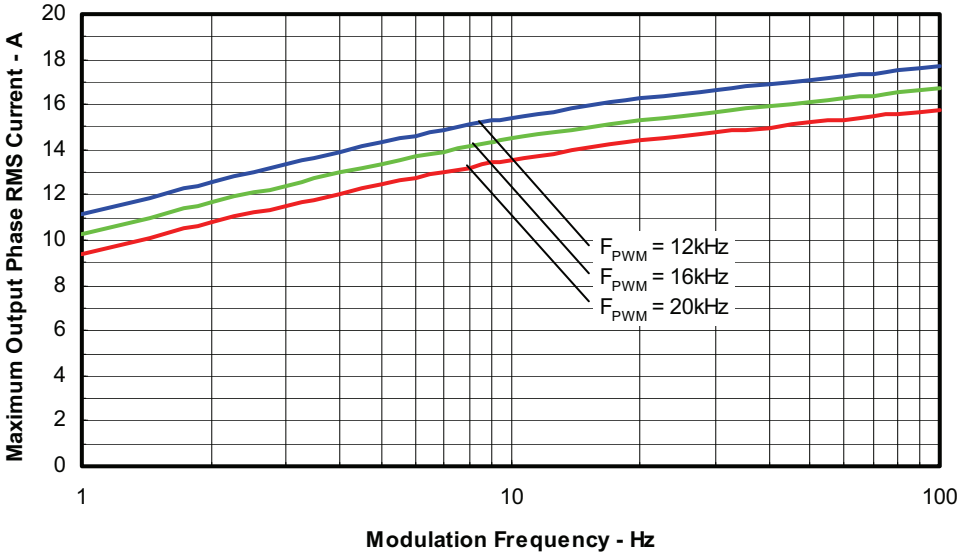


Figure 4. Maximum Sinusoidal Phase Current vs. Modulation Frequency
Sinusoidal Modulation, V^+=100V, T_J=100°C, Modulation Depth=0.8, PF=0.6

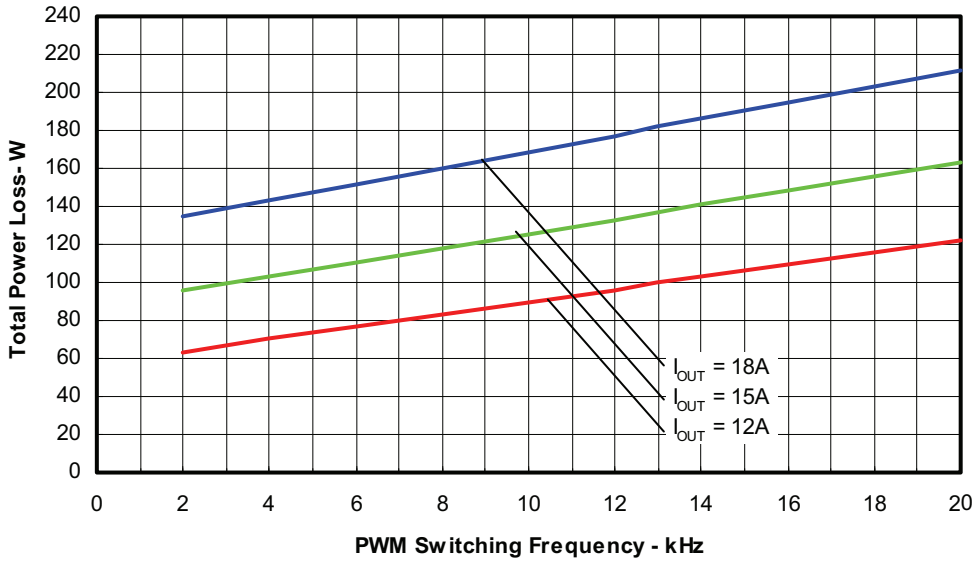


Figure 5. Total Power Losses vs. PWM Switching Frequency
Sinusoidal Modulation, V^+=100V, T_J=150°C, Modulation Depth=0.8, PF=0.6

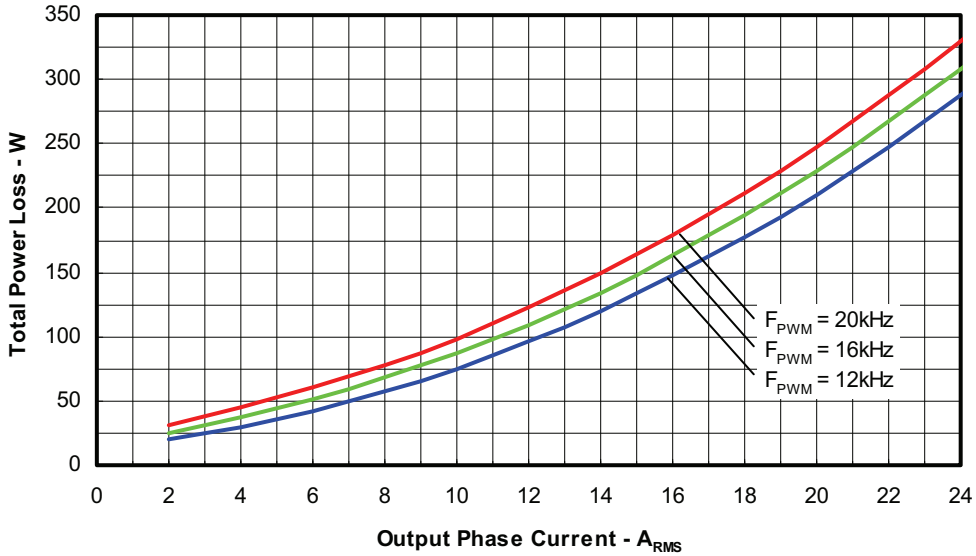


Figure 6. Total Power Losses vs. Output Phase Current
Sinusoidal Modulation, V^+=100V, T_J=150°C, Modulation Depth=0.8, PF=0.6

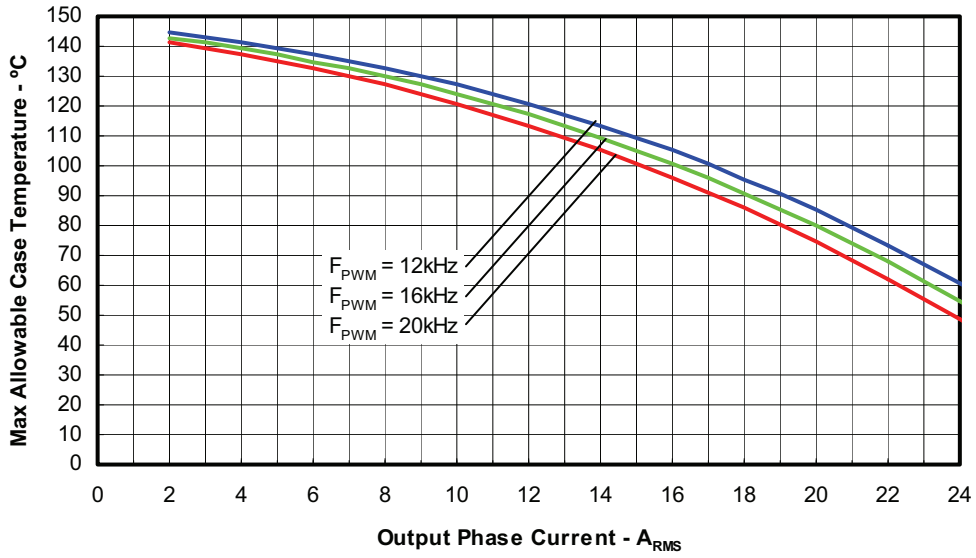


Figure 7. Maximum Allowable Case Temperature vs. Output RMS Current per Phase Sinusoidal Modulation, V^+=100V, T_J=150°C, Modulation Depth=0.8, PF=0.6

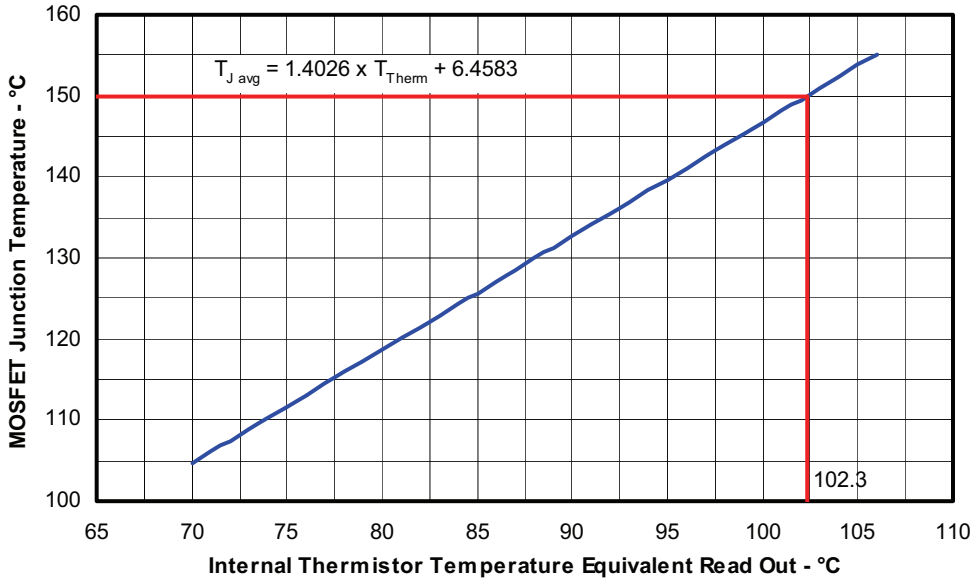
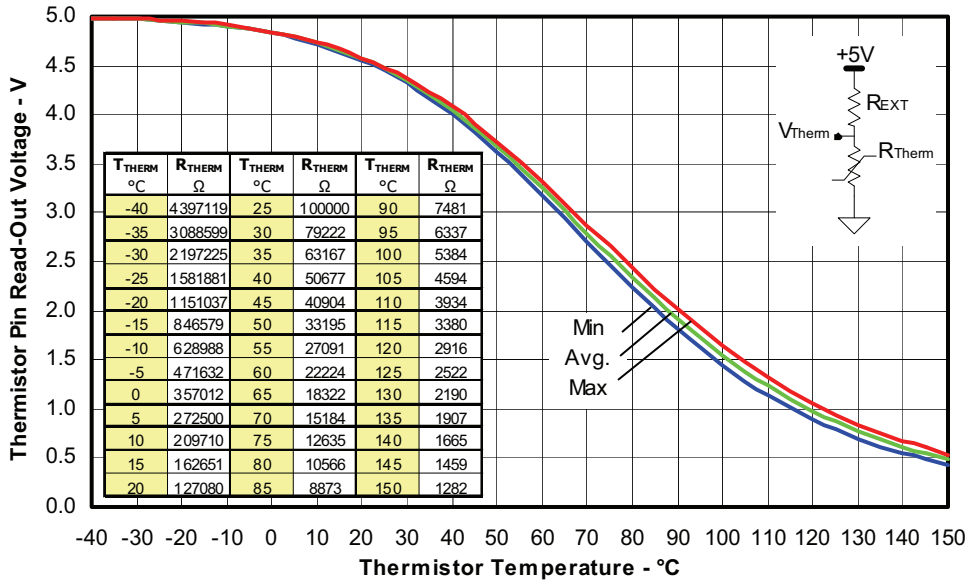


Figure 8. Estimated Maximum MOSFET Junction Temperature vs. Thermistor Temperature



T_{THERM} °C	R_{THERM} Ω	T_{THERM} °C	R_{THERM} Ω	T_{THERM} °C	R_{THERM} Ω
-40	4397119	25	100000	90	7481
-35	3088599	30	79222	95	6337
-30	2197225	35	63167	100	5384
-25	1581881	40	50677	105	4594
-20	1151037	45	40904	110	3934
-15	846579	50	33195	115	3380
-10	628988	55	27091	120	2916
-5	471632	60	22224	125	2522
0	357012	65	18322	130	2190
5	272500	70	15184	135	1907
10	209710	75	12635	140	1665
15	162651	80	10566	145	1459
20	127080	85	8873	150	1282

Figure 9. Thermistor Readout vs. Temperature (12Kohm pull-up resistor, 5V) and Normal Thermistor Resistance values vs. Temperature Table.

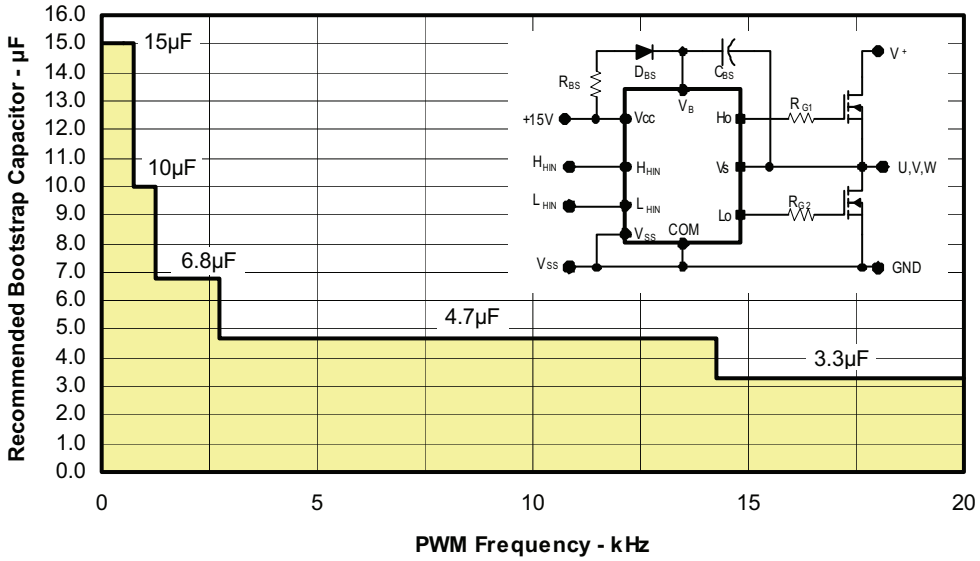


Figure 10. Recommended Bootstrap Capacitor Value vs. Switching Frequency

Figure 11. Switching Parameter Definitions

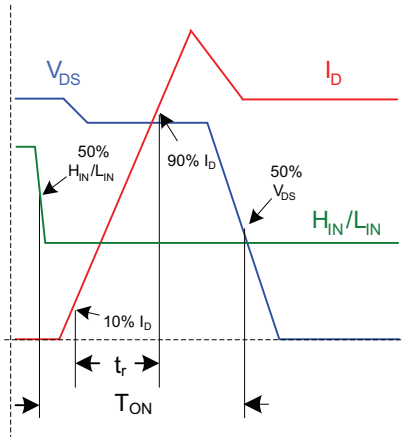


Figure 11a. Input to Output propagation turn-on delay time.

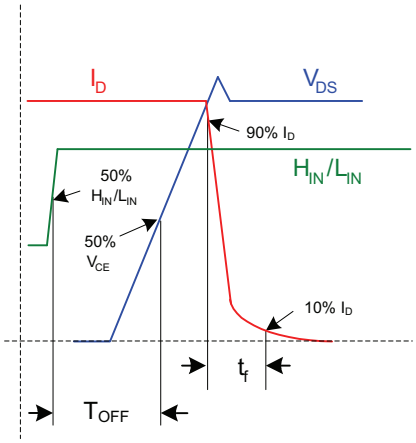


Figure 11b. Input to Output propagation turn-off delay time.

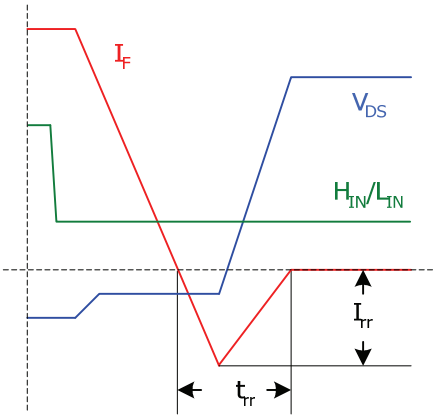


Figure 11c. Diode Reverse Recovery.

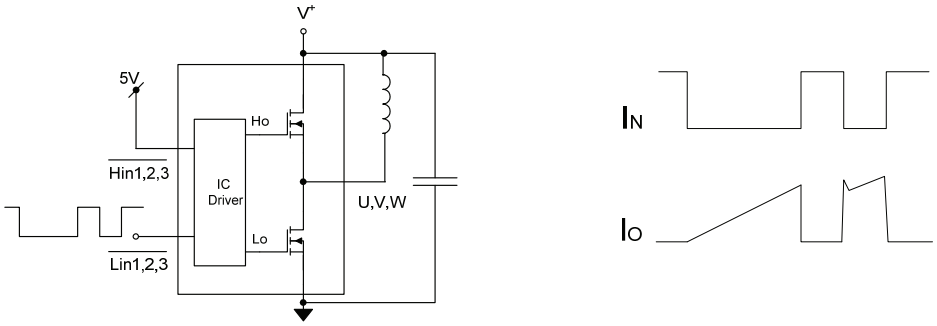


Figure CT1. Switching Loss Circuit

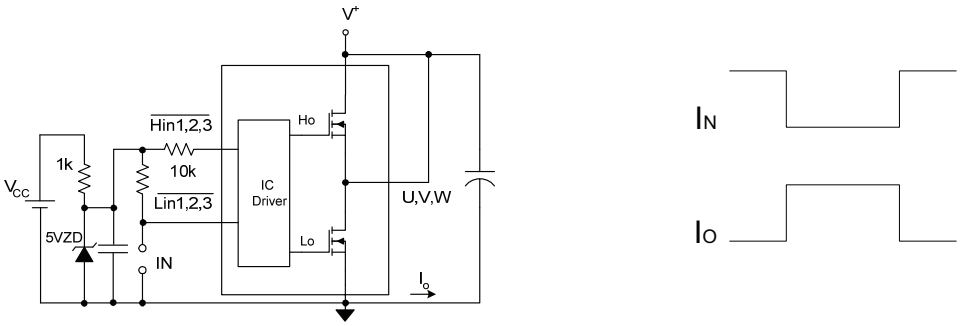


Figure CT2. S.C.SOA Circuit

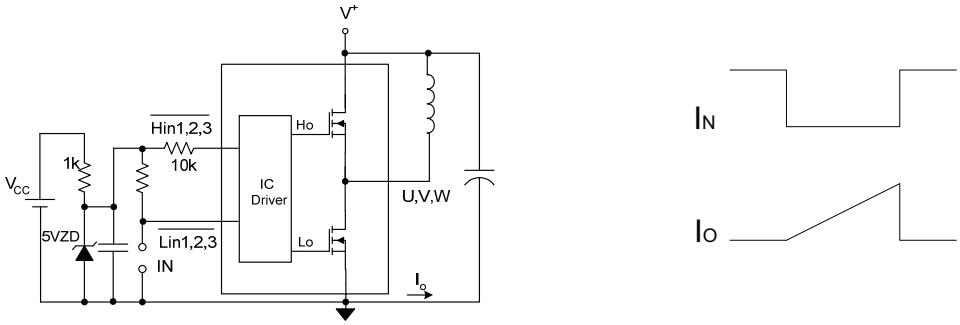
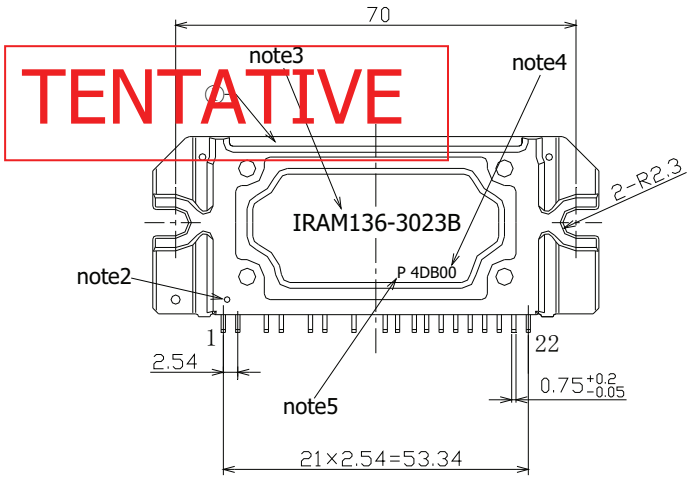


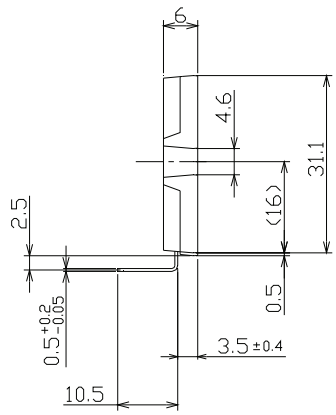
Figure CT3. R.B.SOA Circuit

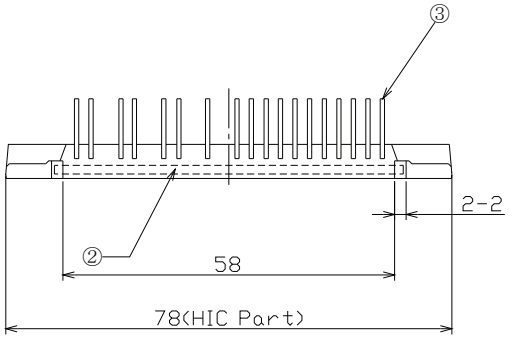
Package Outline

Missing pins: 3, 6, 9, 11

Missing Pin : 3,6,9,11







note1: Unit Tolerance is ±0.5mm,
Unless Otherwise Specified.

note2: Mirror Surface Mark indicates Pin1 Identification.

note3: Part Number Marking.
Characters Font in this drawing differs from Font shown on Module.

note4: Lot Code Marking.
Characters Font in this drawing differs from Font shown on Module.

note5: "P" Character denotes Lead Free.
Characters Font in this drawing differs from Font shown on Module.

For mounting instruction see AN-1049

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