



查询IRFB11N50APbF供应商

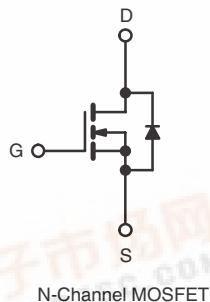
捷多邦，专业PCB打样工厂，24小时加急出货

IRFB11N50A, SiHFB11N50A

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 0.52
Q_g (Max.) (nC)	52
Q_{gs} (nC)	13
Q_{gd} (nC)	18
Configuration	Single



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and current
- Lead (Pb)-free Available

RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

APPLICABLE OFF LINE SMPS TOPOLOGIES

- Two Transistor Forward
- Half and Full Bridge
- Power Factor Correction Boost

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFB11N50APbF SiHFB11N50A-E3
SnPb	IRFB11N50A SiHFB11N50A

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	11	A
		7.0	
Pulsed Drain Current ^a	I_{DM}	44	
Linear Derating Factor		1.3	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	275	mJ
Repetitive Avalanche Current ^a	I_{AR}	11	A
Repetitive Avalanche Energy ^a	E_{AR}	17	mJ
Maximum Power Dissipation	P_D	170	W
Peak Diode Recovery dV/dt ^c	dV/dt	6.9	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 4.5$ mH, $R_G = 25$ Ω, $I_{AS} = 11$ A (see fig. 12).
- $I_{SD} \leq 11$ A, $dI/dt \leq 140$ A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- ± 0.1 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply



IRFB11N50A, SiHFB11N50A

Vishay Siliconix



THERMAL RESISTANCE

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.75	

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

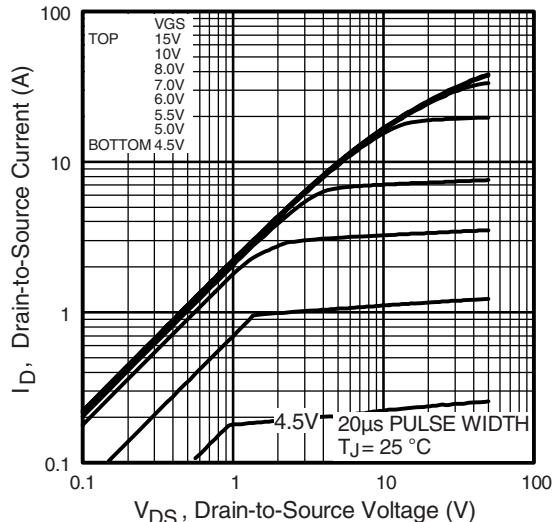
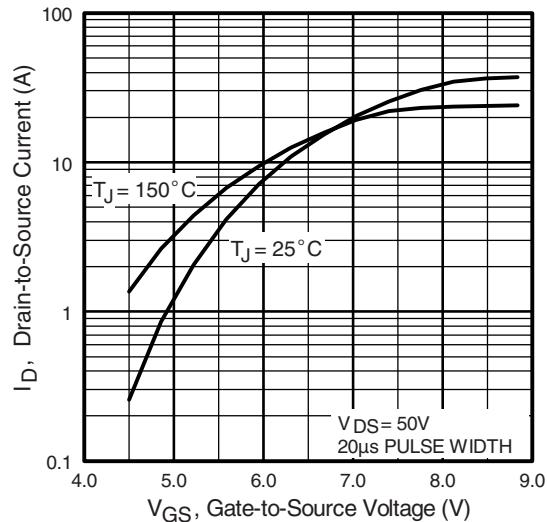
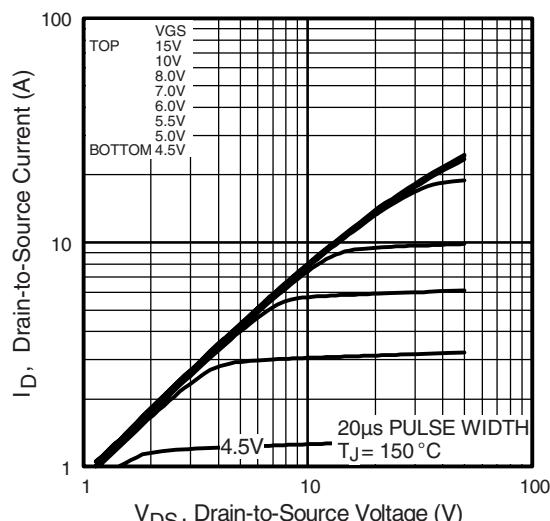
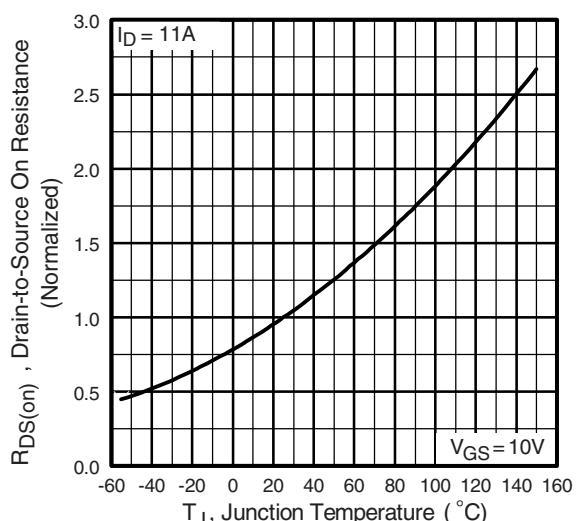
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30 \text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	25	μA
		$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 150^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$ $I_D = 6.6 \text{ A}^b$	-	-	0.52	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}, I_D = 6.6 \text{ A}$	6.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz, see fig. 5}$	-	1423	-	pF
Output Capacitance	C_{oss}		-	208	-	
Reverse Transfer Capacitance	C_{rss}		-	8.1	-	
Output Capacitance	C_{oss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 1.0 \text{ V}, f = 1.0 \text{ MHz}$	-	2000	
			$V_{DS} = 400 \text{ V}, f = 1.0 \text{ MHz}$	-	55	
			$V_{DS} = 0 \text{ V to } 400 \text{ V}$	-	97	
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}, V_{DS} = 400 \text{ V}$ see fig. 6 and 13 ^b	-	-	52
Gate-Source Charge	Q_{gs}			-	-	13
Gate-Drain Charge	Q_{gd}			-	-	18
Turn-On Delay Time	$t_{d(on)}$			-	14	-
Rise Time	t_r	$V_{DD} = 250 \text{ V}, I_D = 11 \text{ A}$ $R_G = 9.1 \Omega, R_D = 22 \Omega, \text{ see fig. 10}^b$		-	35	-
Turn-Off Delay Time	$t_{d(off)}$			-	32	-
Fall Time	t_f			-	28	-
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	11	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	44	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_S = 11 \text{ A}, V_{GS} = 0 \text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 11 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}^b$	-	510	770	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.4	5.1	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.

c. C_{oss} effective is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

IRFB11N50A, SiHFB11N50A

Vishay Siliconix

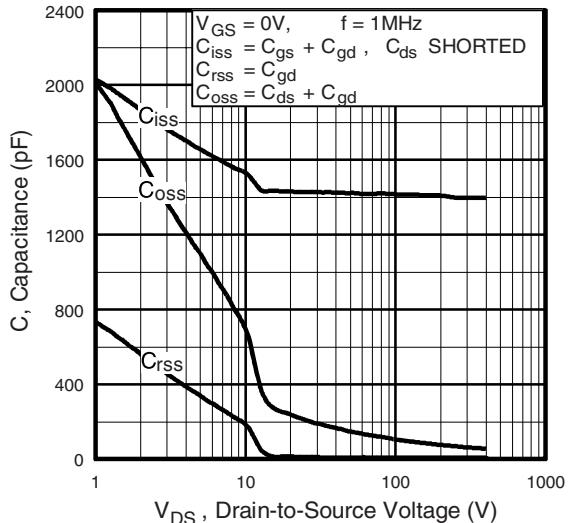


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

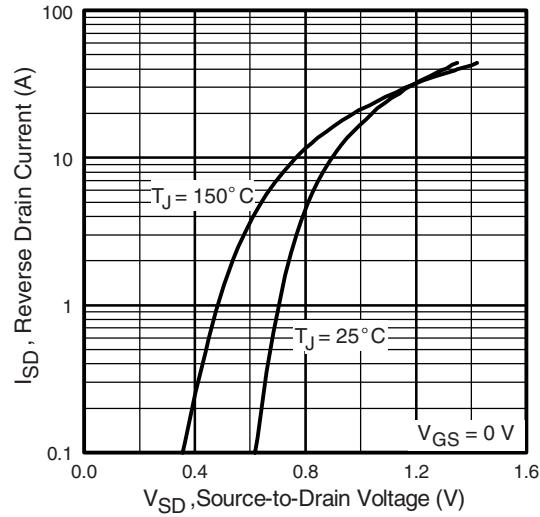


Fig. 7 - Typical Source-Drain Diode Forward Voltage

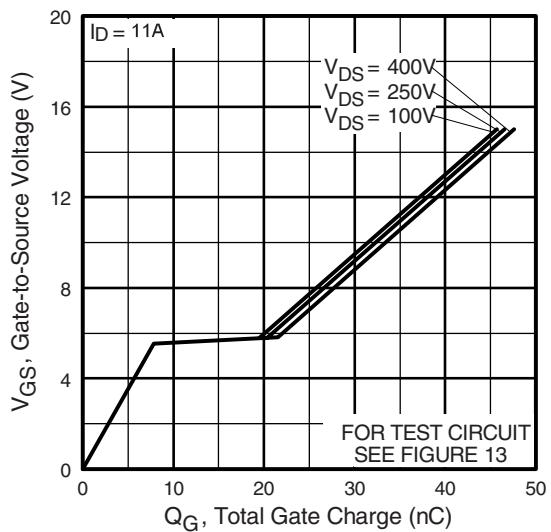


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

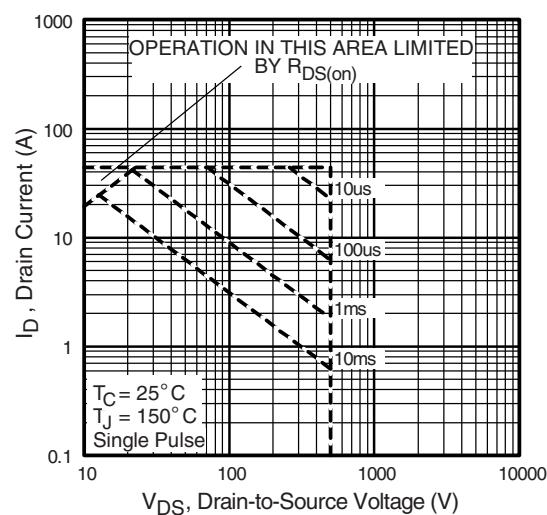


Fig. 8 - Maximum Safe Operating Area

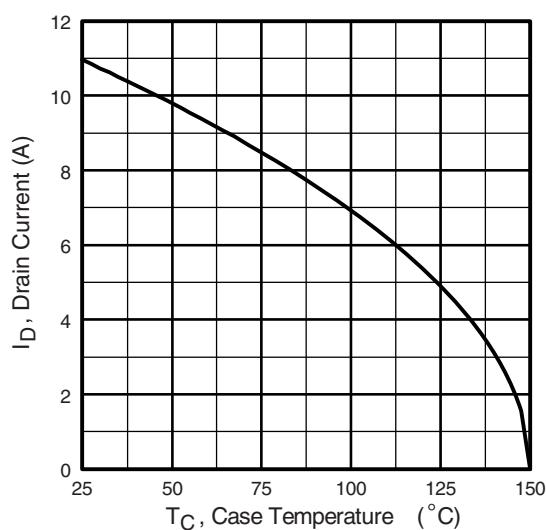


Fig. 9 - Maximum Drain Current vs. Case Temperature

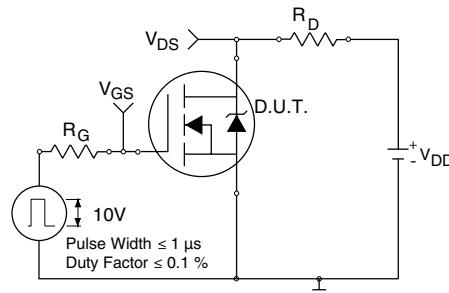


Fig. 10a - Switching Time Test Circuit

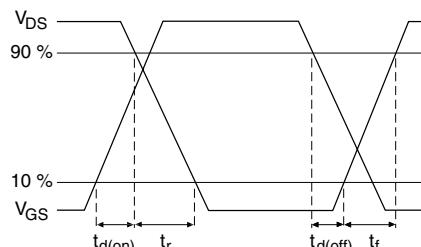


Fig. 10b - Switching Time Waveforms

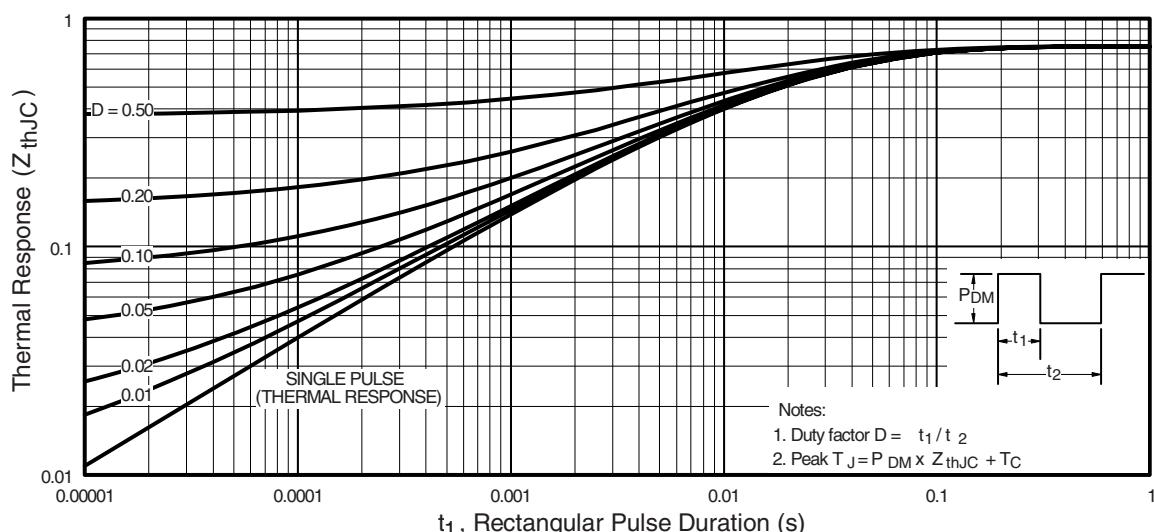


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

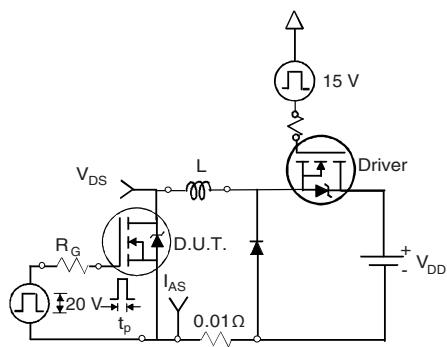


Fig. 12a - Unclamped Inductive Test Circuit

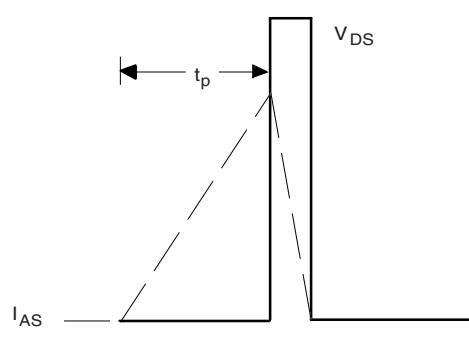


Fig. 12b - Unclamped Inductive Waveforms

IRFB11N50A, SiHFB11N50A

Vishay Siliconix

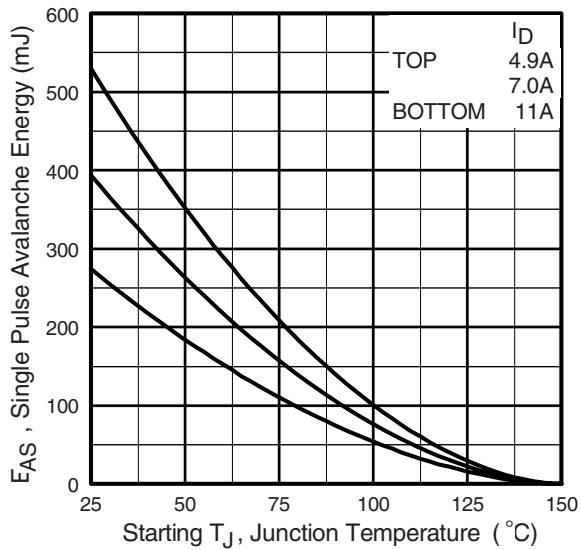


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

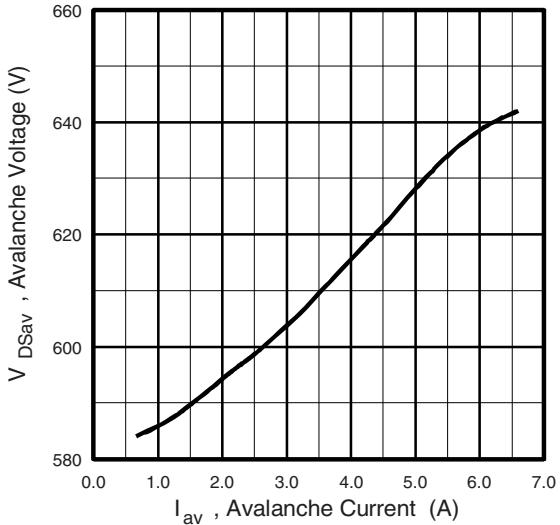


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

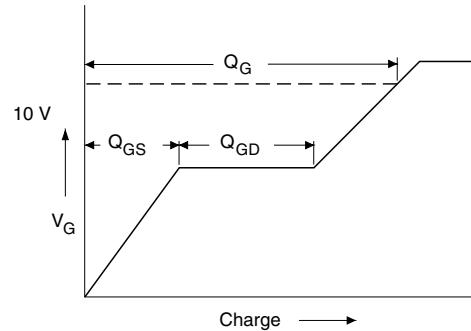


Fig. 13a - Basic Gate Charge Waveform

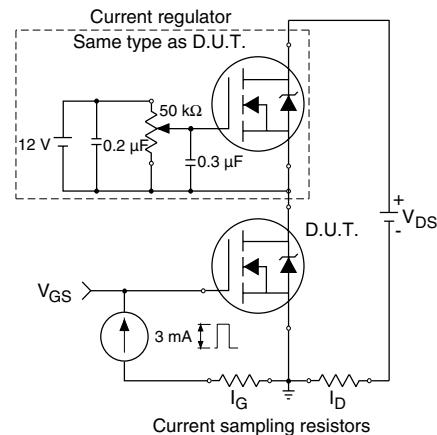
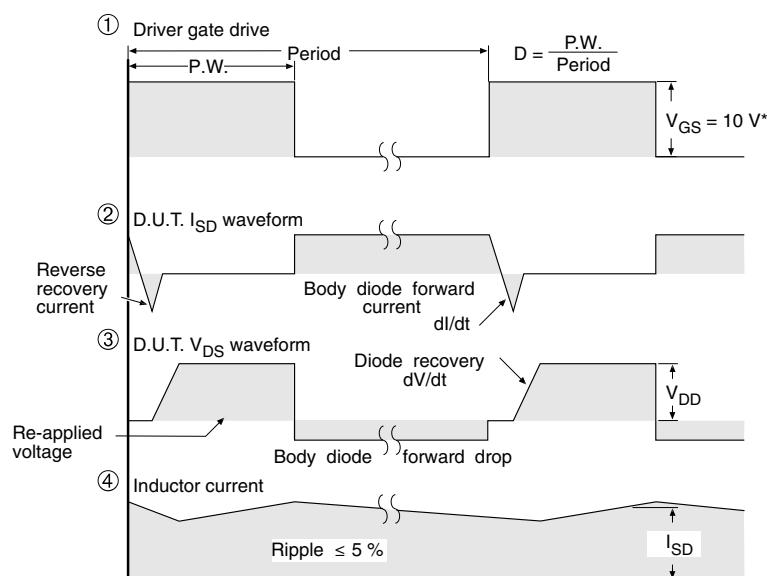
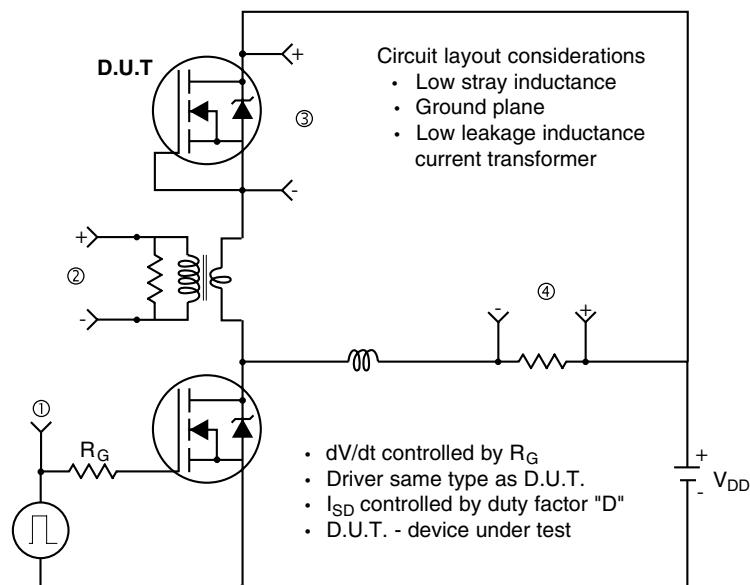


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel



Legal Disclaimer Notice

Vishay

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.