

International
IR Rectifier

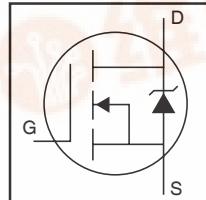
IRFB3077PbF

Applications

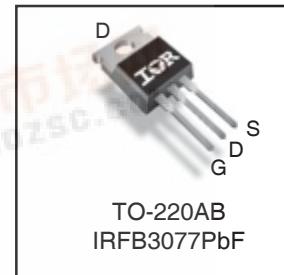
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Worldwide Best $R_{DS(on)}$ in TO-220
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and di/dt Capability



V_{DSS}	75V
$R_{DS(on)}$ typ.	2.8mΩ
max.	3.3mΩ
I_D	210A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	210①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	150 ①	
I_{DM}	Pulsed Drain Current ②	850	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	
V_{GS}	Gate-to-Source Voltage	± 20	V
dV/dt	Peak Diode Recovery ④	2.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	240	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R_{JC}	Junction-to-Case ⑨	—	0.402	°C/W
R_{FC}	Case-to-Sink, Flat Greased Surface	0.50	—	
R_{JA}	Junction-to-Ambient ⑩⑪	—	62	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.091	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	2.8	3.3	m Ω	$V_{GS} = 10V, I_D = 75\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250	—	$V_{DS} = 75V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	—	$V_{GS} = -20V$
R_G	Gate Input Resistance	—	1.2	—	Ω	$f = 1\text{MHz}$, open drain

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	160	—	—	S	$V_{DS} = 50V, I_D = 75\text{A}$
Q_g	Total Gate Charge	—	160	220	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	37	—	—	$V_{DS} = 38V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	42	—	—	$V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 38V$
t_r	Rise Time	—	87	—	—	$I_D = 75\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	69	—	—	$R_G = 2.1\Omega$
t_f	Fall Time	—	95	—	—	$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	9400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	820	—	—	$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	350	—	—	$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)⑦	—	1090	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑧, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	1260	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑨, See Fig. 5

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	210①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②⑦	—	—	850	—	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_s = 75\text{A}, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	42	63	ns	$T_J = 25^\circ\text{C} \quad V_R = 64V,$
		—	50	75	—	$T_J = 125^\circ\text{C} \quad I_F = 75\text{A}$
Q_{rr}	Reverse Recovery Charge	—	59	89	nC	$T_J = 25^\circ\text{C} \quad \text{di/dt} = 100\text{A}/\mu\text{s}$ ⑤
		—	86	130	—	$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by $T_{J\max}$, starting $T_J = 25^\circ\text{C}$, $L = 0.08\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 75\text{A}$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 75\text{A}$, $\text{di/dt} \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\text{us}$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .

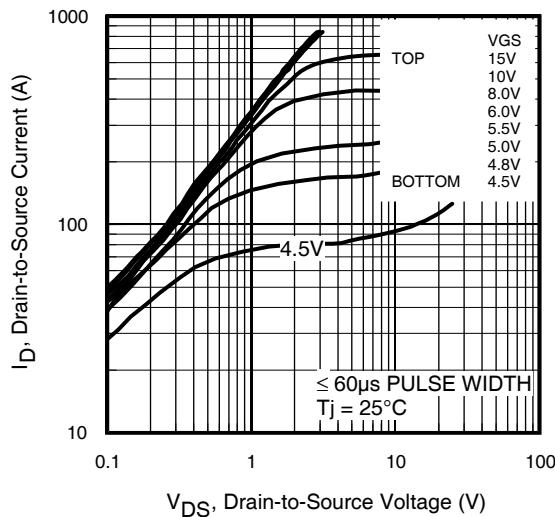


Fig 1. Typical Output Characteristics

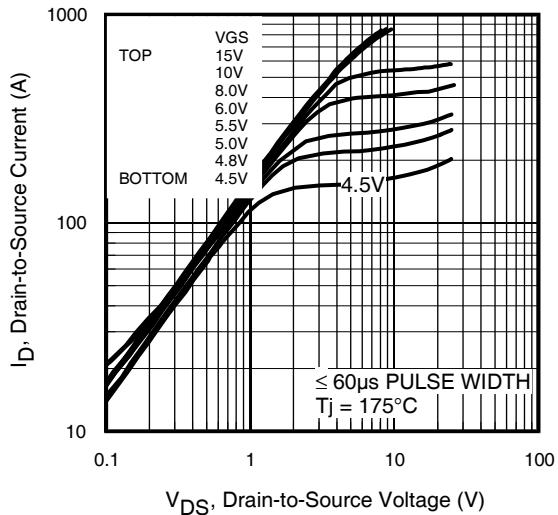


Fig 2. Typical Output Characteristics

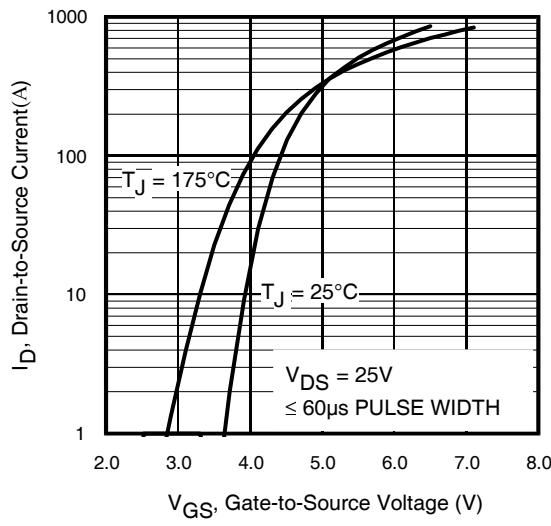


Fig 3. Typical Transfer Characteristics

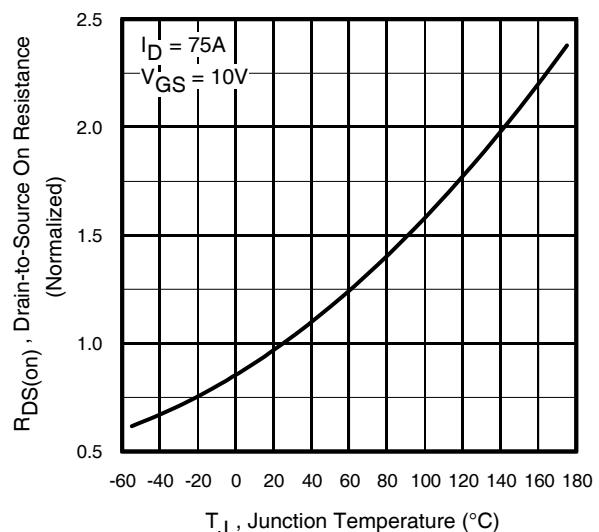


Fig 4. Normalized On-Resistance vs. Temperature

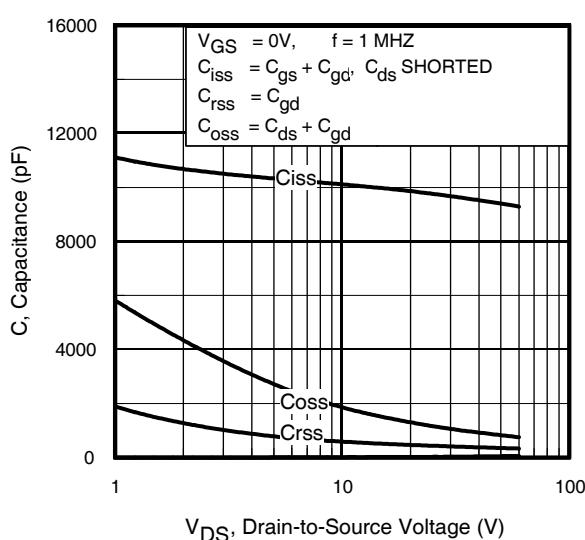


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

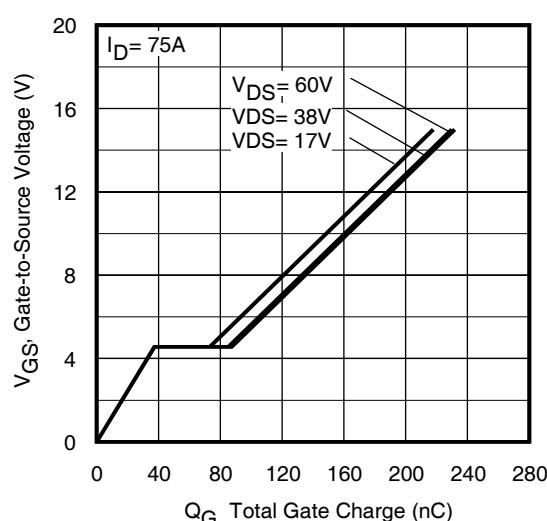


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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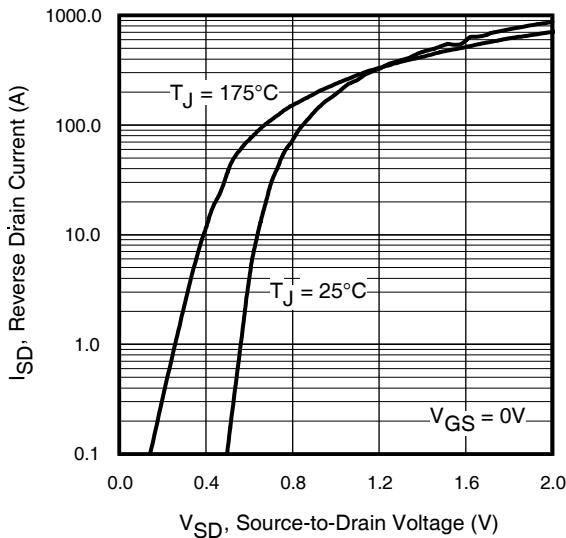


Fig 7. Typical Source-Drain Diode Forward Voltage

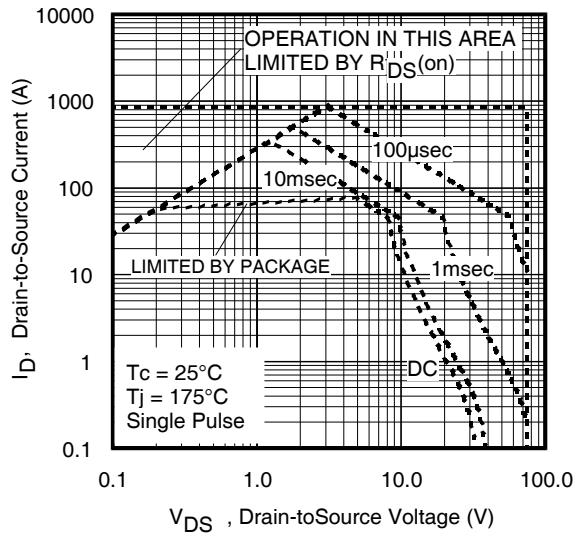


Fig 8. Maximum Safe Operating Area

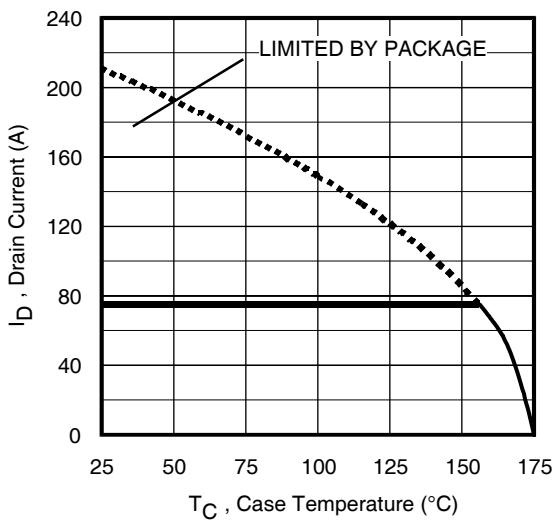


Fig 9. Maximum Drain Current vs. Case Temperature

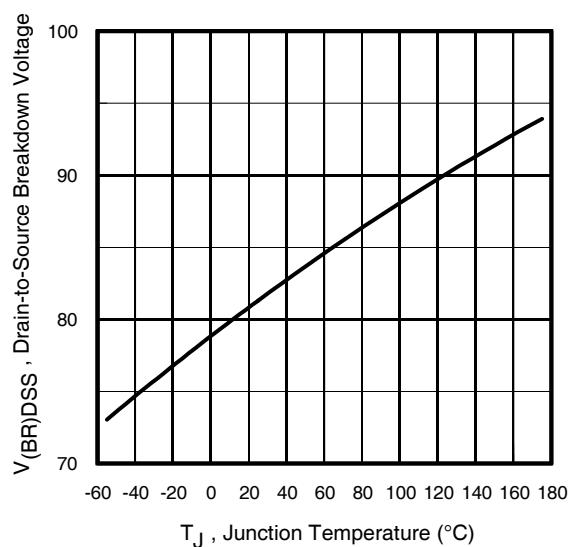


Fig 10. Drain-to-Source Breakdown Voltage

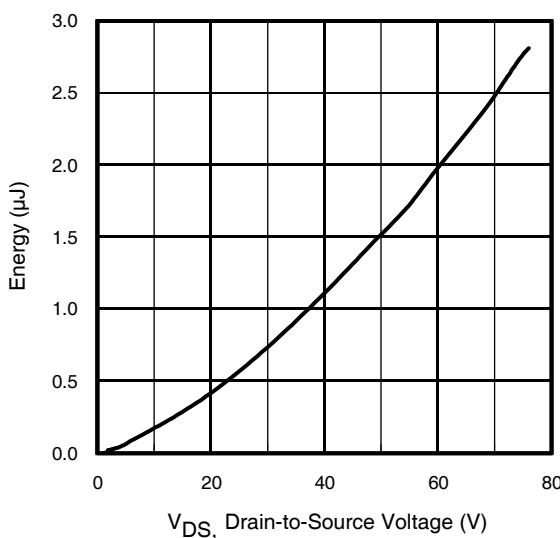


Fig 11. Typical Coss Stored Energy

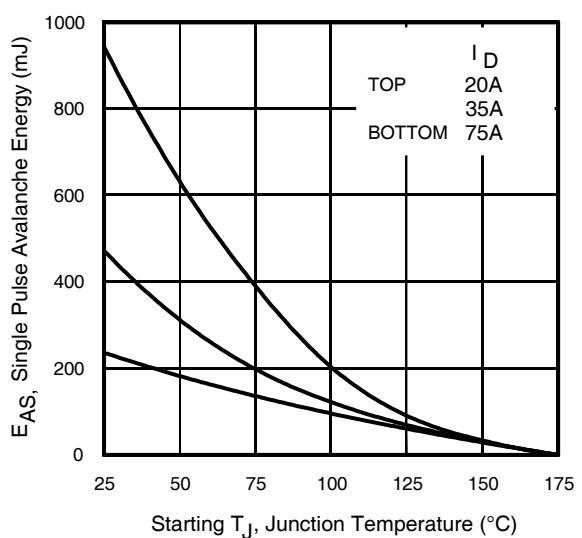


Fig 12. Maximum Avalanche Energy Vs. Drain Current

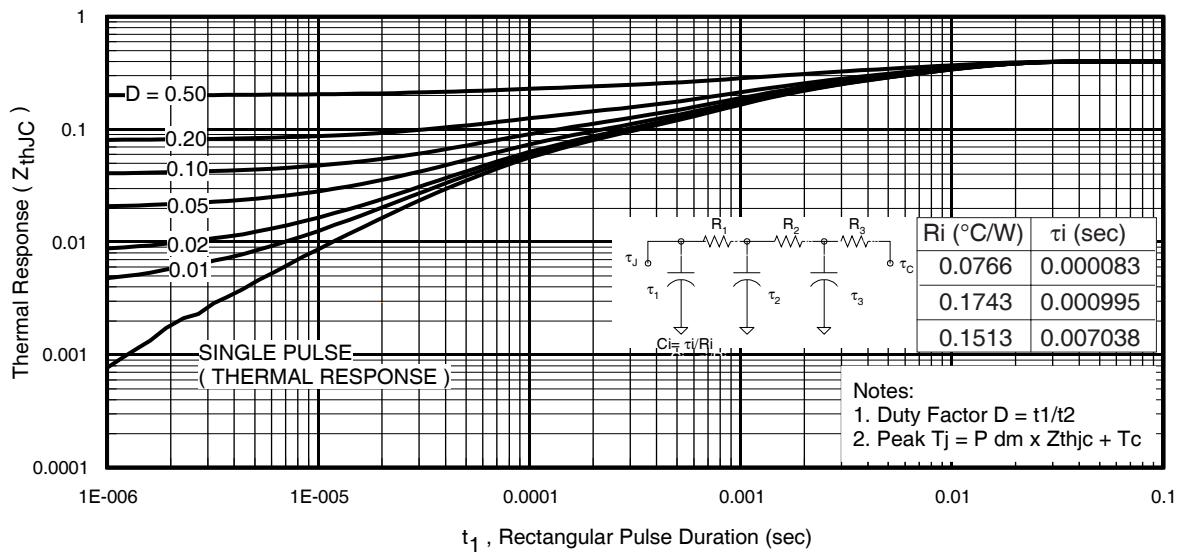


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

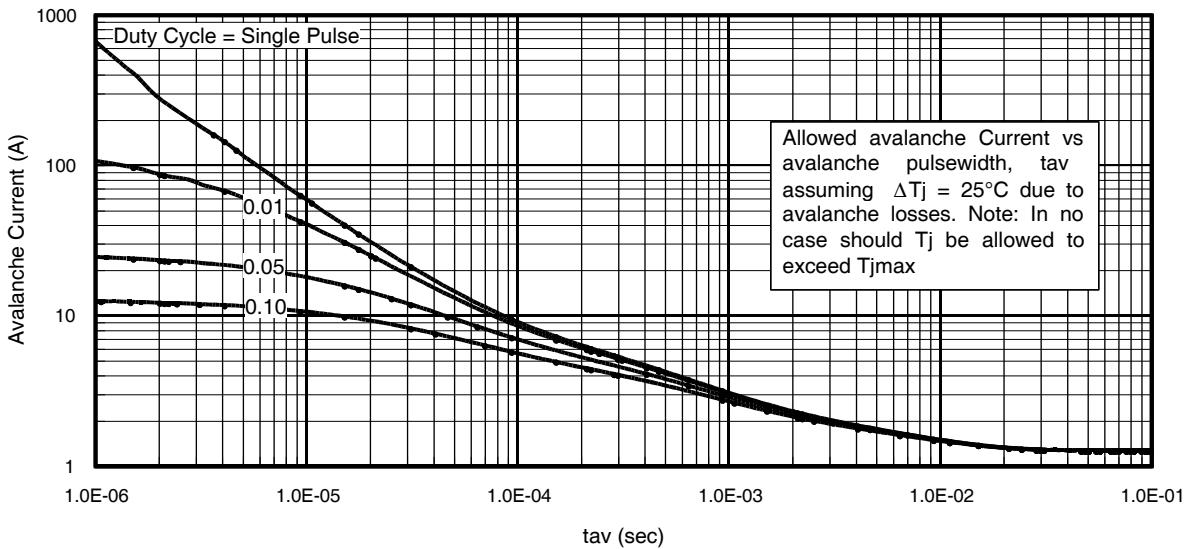
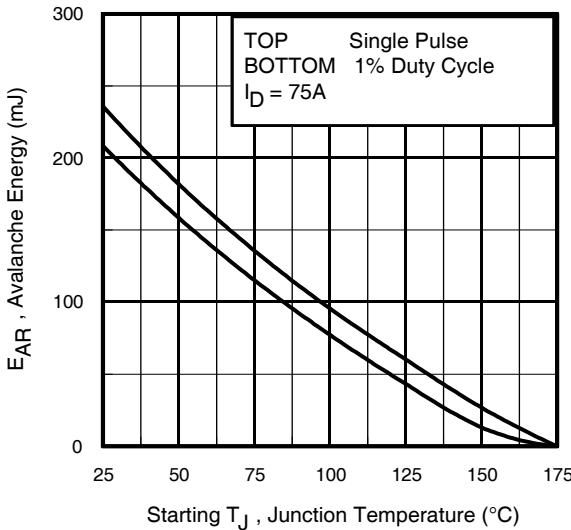


Fig 14. Typical Avalanche Current vs.Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 15:
 (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
 3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
 4. $P_D(\text{ave})$ = Average power dissipation per single avalanche pulse.
 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
 6. I_{av} = Allowable avalanche current.
 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
- t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_D(\text{ave}) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_D(\text{ave}) \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

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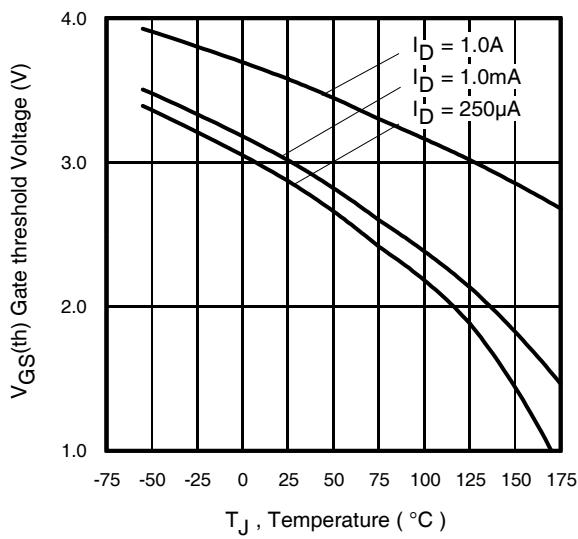


Fig. 16. Threshold Voltage Vs. Temperature

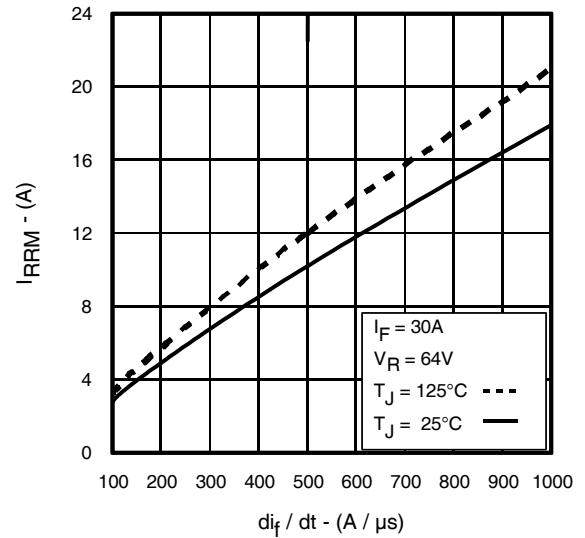


Fig. 17 - Typical Recovery Current vs. di_f/dt

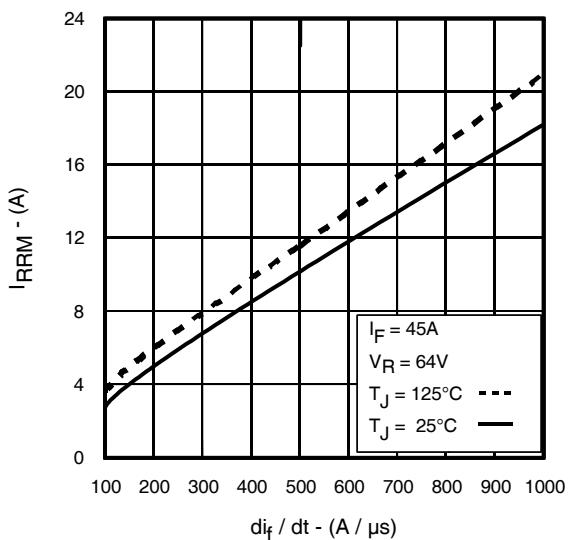


Fig. 18 - Typical Recovery Current vs. di_f/dt

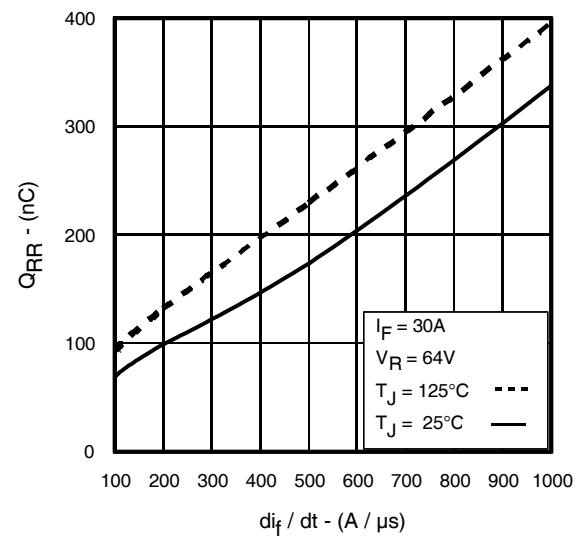


Fig. 19 - Typical Stored Charge vs. di_f/dt

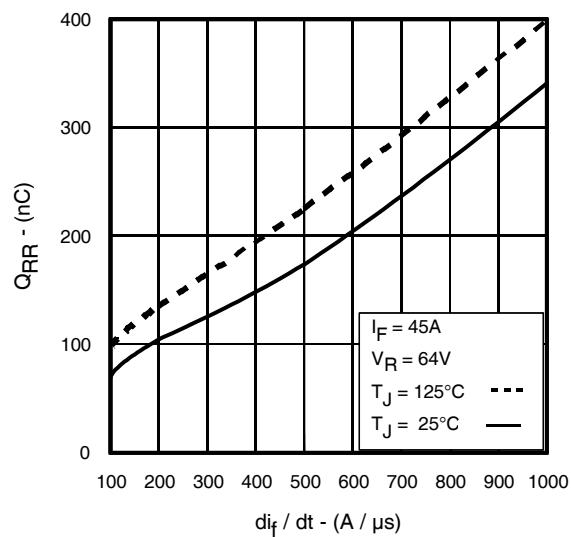


Fig. 20 - Typical Stored Charge vs. di_f/dt

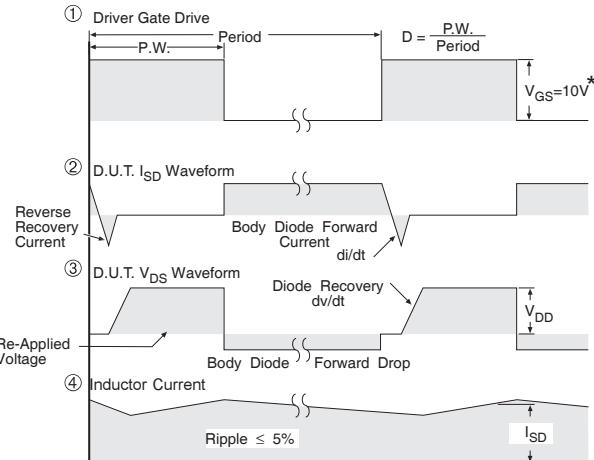
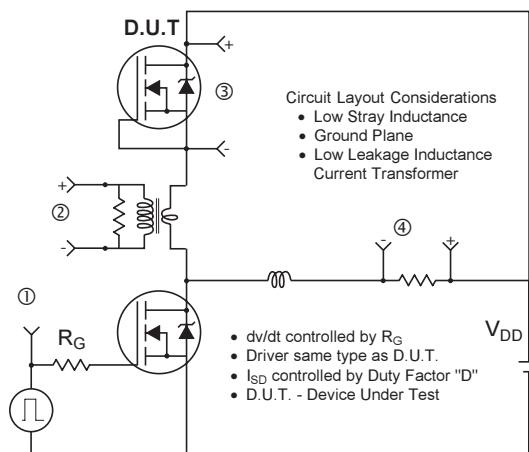


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

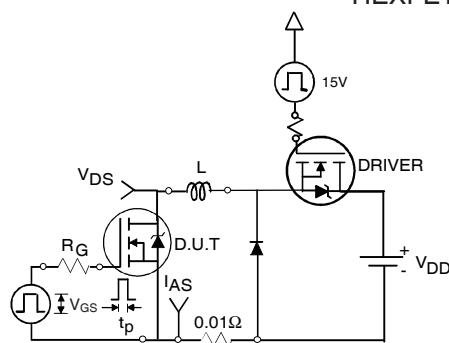


Fig 22a. Unclamped Inductive Test Circuit

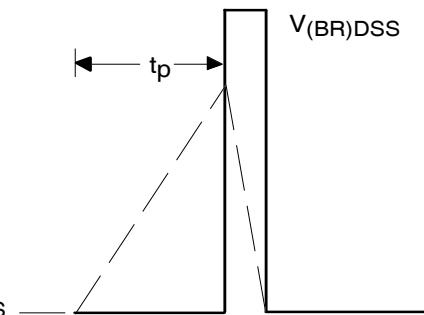


Fig 22b. Unclamped Inductive Waveforms

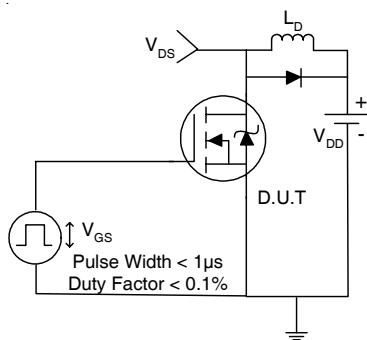


Fig 23a. Switching Time Test Circuit

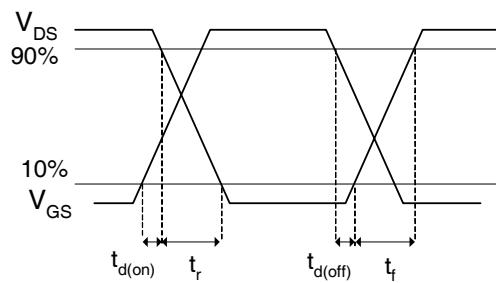


Fig 23b. Switching Time Waveforms

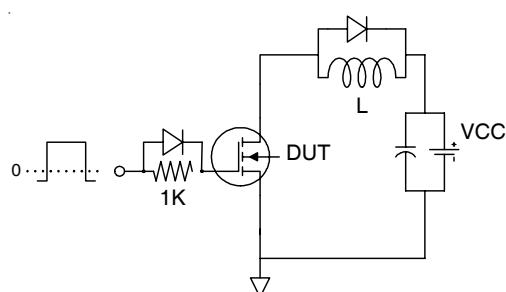


Fig 24a. Gate Charge Test Circuit

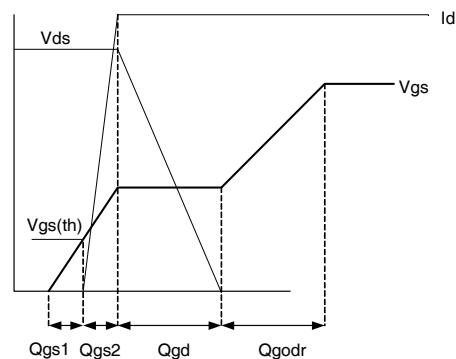
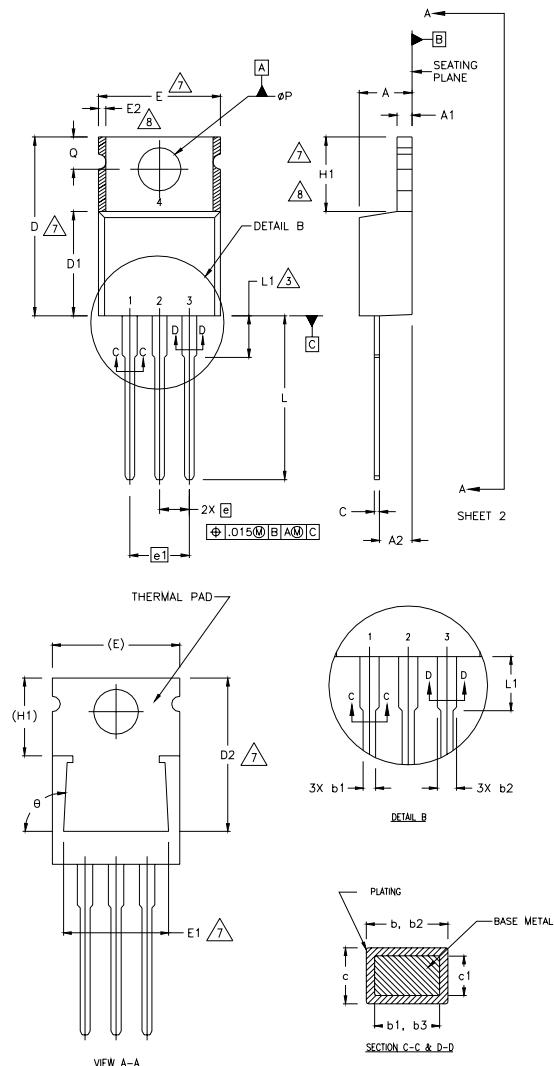


Fig 24b. Gate Charge Waveform

IRFB3077PbF

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



VIEW A-A

NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
- 6 CONTROLLING DIMENSION : INCHES.
- 7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter

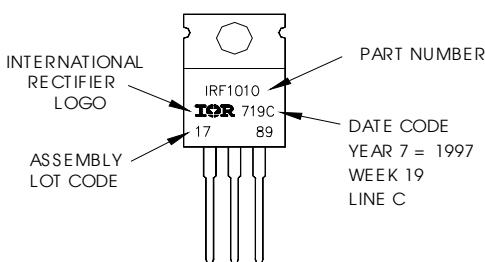
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.82	.140	.190		
A1	0.51	1.40	.020	.055		
A2	2.04	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.96	.015	.038	5	
b2	1.15	1.77	.045	.070		
b3	1.15	1.73	.045	.068		
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650	4	
D1	8.38	9.02	.330	.355		
D2	12.19	12.88	.480	.507	7	
E	9.66	10.66	.380	.420	4,7	
E1	8.38	8.89	.330	.350	7	
e	2.54	BSC	.100	BSC		
e1	5.08		.200	BSC		
H1	5.85	6.55	.230	.270	7,8	
L	12.70	14.73	.500	.580		
L1	-	6.35	-	.250	3	
ØP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		
Ø	90°-93°		90°-93°			

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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