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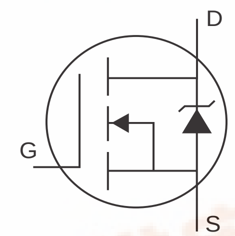
International
IOR Rectifier

PD - 94694

IRFBE30S
IRFBE30L

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



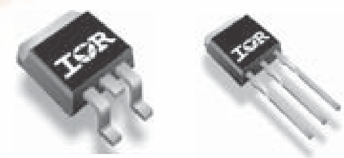
V_{DSS} = 800V

$R_{DS(on)}$ = 3.0Ω

I_D = 4.1A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



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TO-262
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Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	4.1	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	2.6	
I_{DM}	Pulsed Drain Current ①	16	
P_D @T_C = 25°C	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	260	mJ
I_{AR}	Avalanche Current ①	4.1	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	——	——	1.0	°C/W
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	——	0.50	——	
$R_{θJA}$	Junction-to-Ambient	——	——	62	

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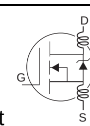
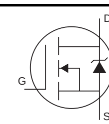
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	800	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.90	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V_{GS} = 10V, I_D = 2.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μA
gfs	Forward Transconductance	2.5	—	—	S	V_{DS} = 100V, I_D = 2.5A
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS} = 800V, V_{GS} = 0V
		—	—	500		V_{DS} = 640V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	78	nC	I_D = 4.1A
Q_{gs}	Gate-to-Source Charge	—	—	9.6		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	45		V_{GS} = 10V, See Fig. 6 & 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 400V
t_r	Rise Time	—	33	—		I_D = 4.1A
$t_{d(off)}$	Turn-Off Delay Time	—	82	—		R_G = 12Ω
t_f	Fall Time	—	30	—		R_D = 95Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact  D G S
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	310	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	190	—		f = 1.0MHz, See Fig. 5

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.1	A	MOSFET symbol showing the integral reverse p-n junction diode.  D G S
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	16		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_J = 25°C, I_S = 4.1A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	480	720	ns	T_J = 25°C, I_F = 4.1A
Q_{rr}	Reverse Recovery Charge	—	1.8	2.7	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② V_{DD}=50V, starting T_J = 25°C, L=29mH, R_G=25Ω, I_{AS} = 4.1A. (See Figure 12).

③ $I_{SD} \leq$ 4.1A, di/dt ≤ 100A/μs, $V_{DD} \leq$ 600, $T_J \leq$ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

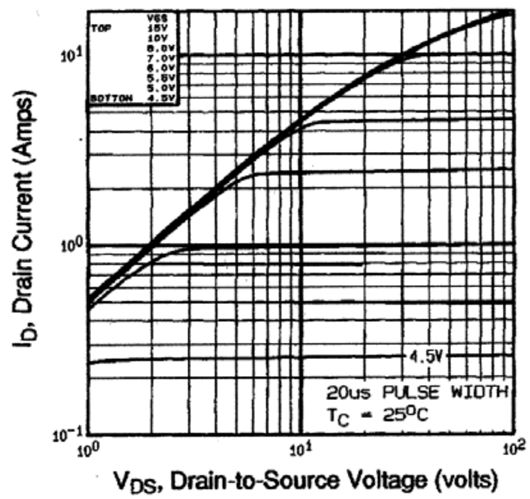


Fig 1. Typical Output Characteristics, T_C=25°C

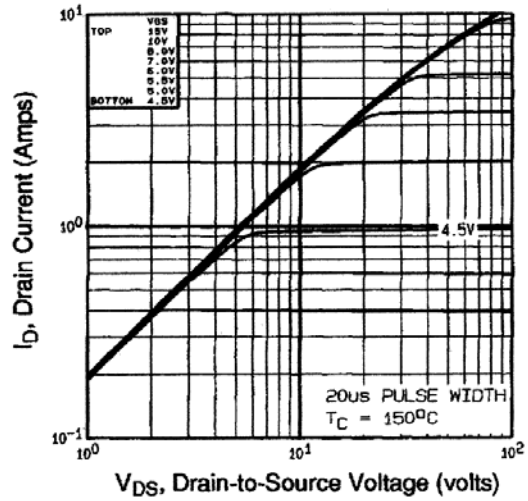


Fig 2. Typical Output Characteristics, T_C=150°C

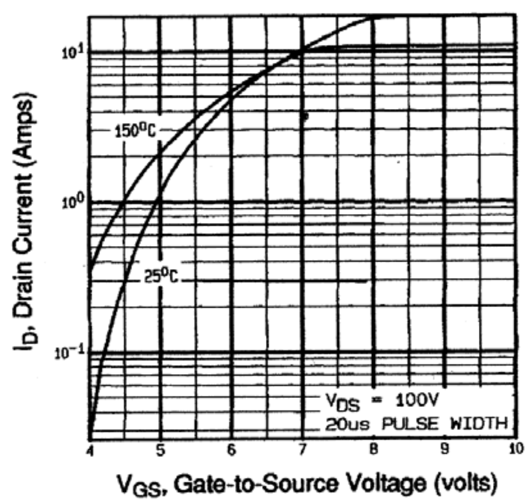


Fig 3. Typical Transfer Characteristics

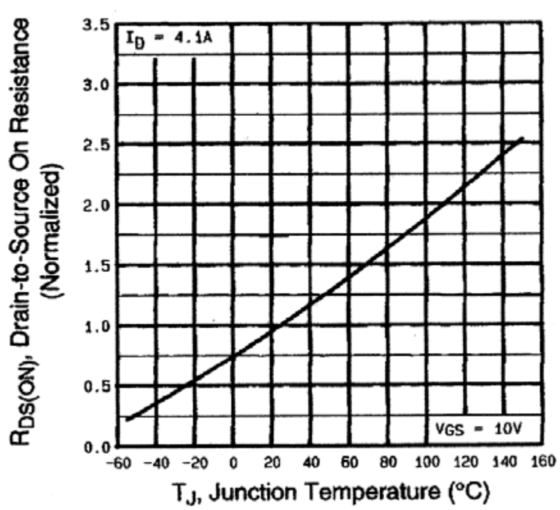


Fig 4. Normalized On-Resistance Vs. Temperature

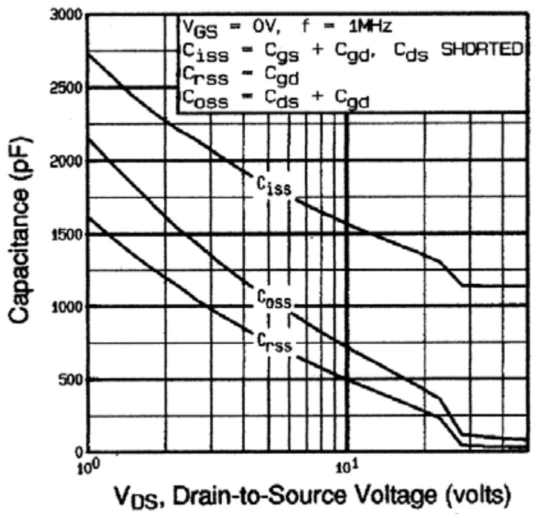


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

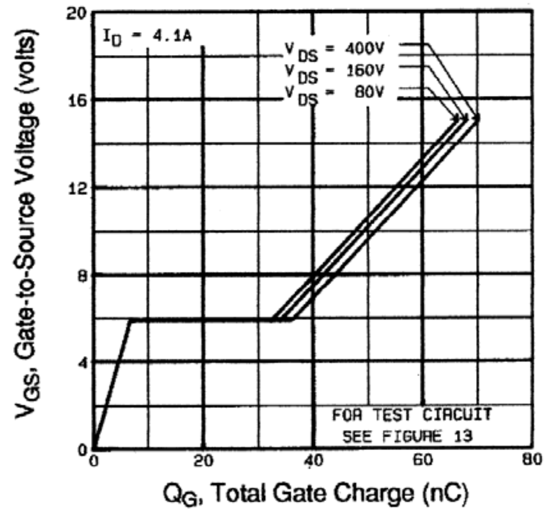


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

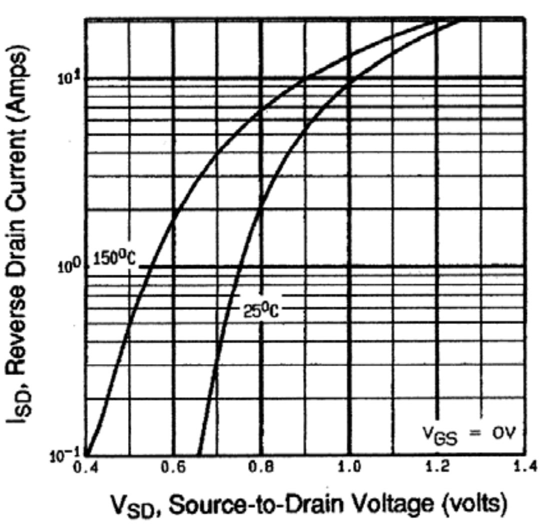


Fig 7. Typical Source-Drain Diode Forward Voltage

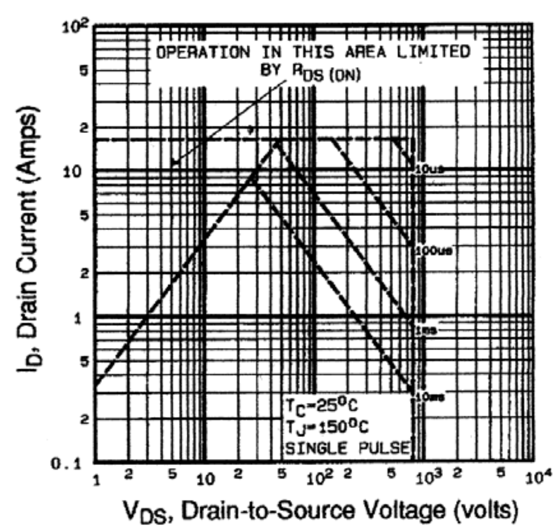


Fig 8. Maximum Safe Operating Area

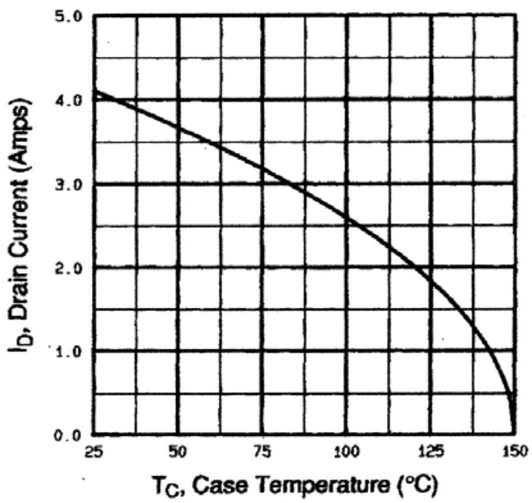


Fig 9. Maximum Drain Current Vs. Case Temperature

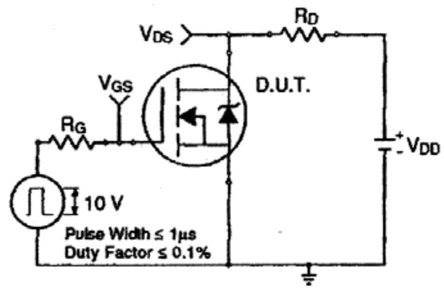


Fig 10a. Switching Time Test Circuit

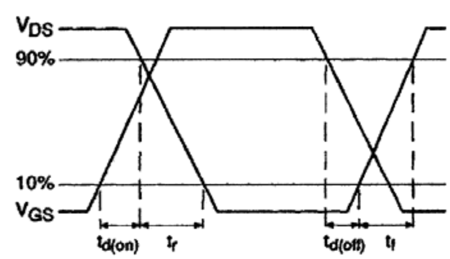


Fig 10b. Switching Time Waveforms

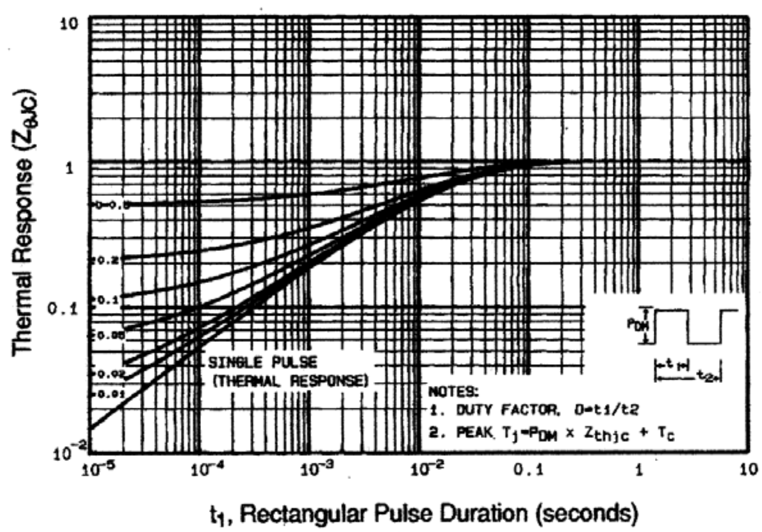


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

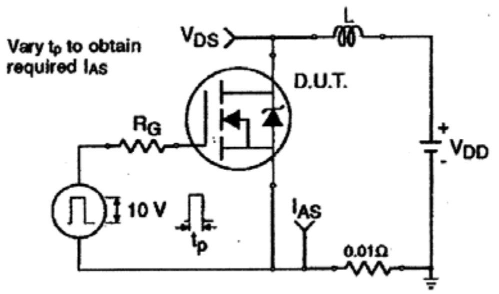


Fig 12a. Unclamped Inductive Test Circuit

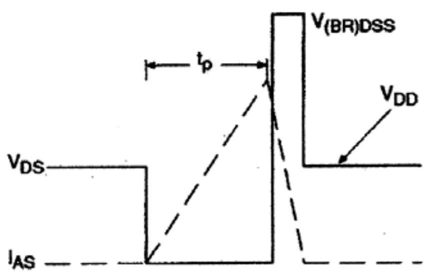


Fig 12b. Unclamped Inductive Waveforms

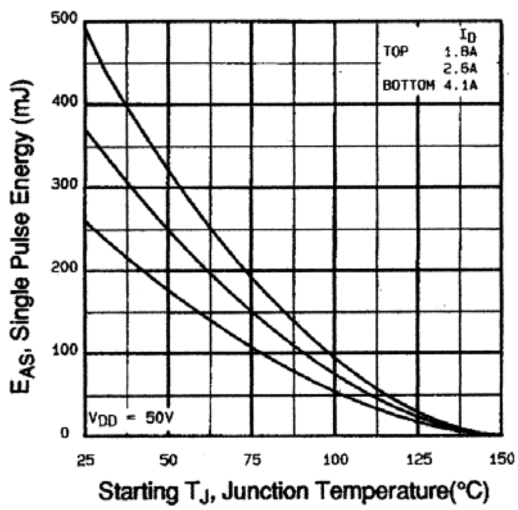


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

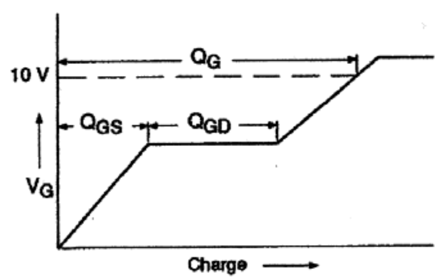


Fig 13a. Basic Gate Charge Waveform

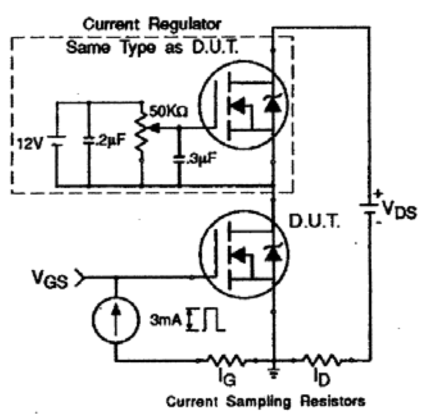


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

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