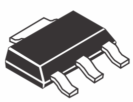
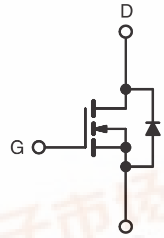
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	2.0
Q_g (Max.) (nC)	8.2	
Q_{gs} (nC)	1.8	
Q_{gd} (nC)	4.5	
Configuration	Single	

SOT-223





N-Channel MOSFET

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performace due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION		
Package	SOT-223	SOT-223
Lead (Pb)-free	IRFL214PbF	IRFL214TRPbF[a]
	SiHFL214-E3	SiHFL214T-E3[a]
SnPb	IRFL214	IRFL214TR[a]
	SiHFL214	SiHFL214T[a]

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	250	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	0.79	A
		T_C = 100 °C		0.50	
Pulsed Drain Current[a]			I_{DM}	6.3	
Linear Derating Factor				0.025	W/°C
Linear Derating Factor (PCB Mount)[e]				0.017	
Single Pulse Avalanche Energy[b]			E_{AS}	50	mJ
Repetitive Avalanche Current[a]			I_{AR}	0.79	A
Repetitive Avalanche Energy[a]			E_{AR}	0.31	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	3.1	W
Maximum Power Dissipation (PCB Mount)[e]	T_A = 25 °C			2.0	

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS $T_C = 25\ °C$, unless otherwise noted

PARAMETER		SYMBOL	LIMIT	UNIT
Peak Diode Recovery dV/dt[c]		dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 128 mH, $R_G = 25\ \Omega$, $I_{AS} = 0.79$ A (see fig. 12).
c. $I_{SD} \leq 2.7$ A, dI/dt ≤ 65 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

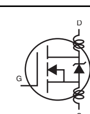
THERMAL RESISTANCE RATINGS

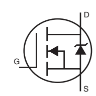
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\ °C$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μA		250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.39	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$ V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250$ V, $V_{GS} = 0$ V		-	-	25	μA
		$V_{DS} = 200$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 0.47$ A[b]	-	-	2.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50$ V, $I_D = 0.47$ A		0.50	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, f = 1.0 MHz, see fig. 5		-	140	-	pF
Output Capacitance	C_{oss}			-	42	-	
Reverse Transfer Capacitance	C_{rss}			-	9.6	-	
Total Gate Charge	Q_g	$V_{GS} = 10$ V	$I_D = 2.7$ A, $V_{DS} = 200$ V, see fig. 6 and 13[b]	-	-	8.2	nC
Gate-Source Charge	Q_{gs}			-	-	1.8	
Gate-Drain Charge	Q_{gd}			-	-	4.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125$ V, $I_D = 2.7$ A, $R_G = 24\ \Omega$, $R_D = 45\ \Omega$, see fig. 10[b]		-	7.0	-	ns
Rise Time	t_r			-	7.6	-	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-	
Fall Time	t_f			-	7.0	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	0.79	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	6.3	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 0.79 A, V_{GS} = 0 V[b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 2.7 A, dI/dt = 100 A/μs[b]	-	190	390	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.64	1.3	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

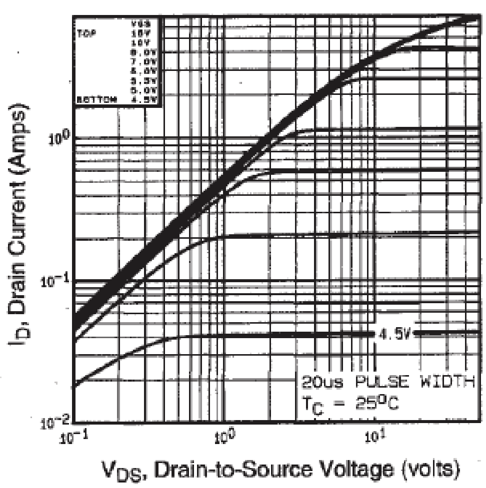


Fig. 1 - Typical Output Characteristics

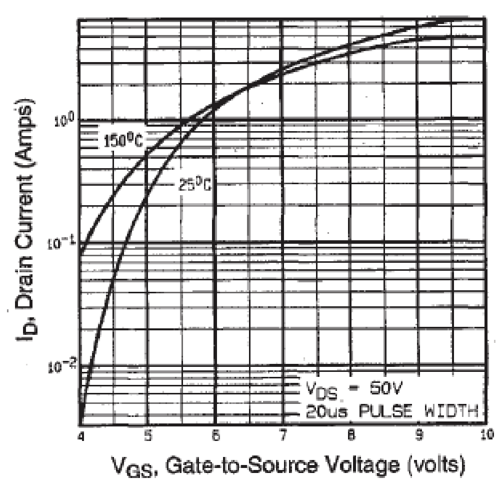


Fig. 3 - Typical Transfer Characteristics

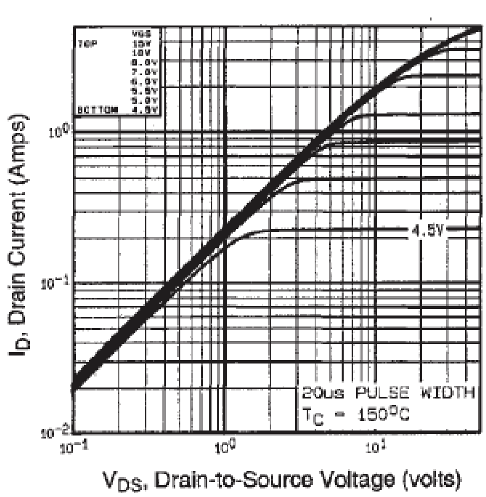


Fig. 2 - Typical Output Characteristics

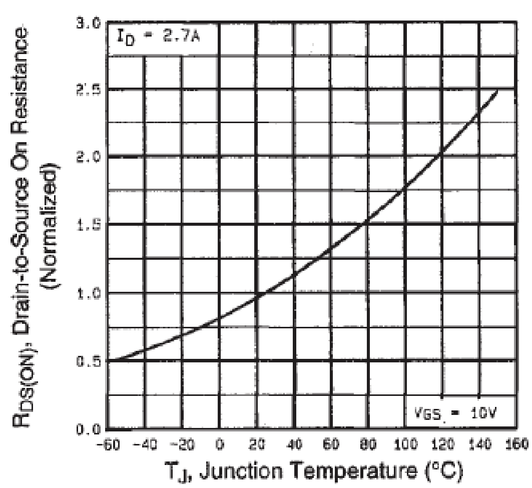


Fig. 4 - Normalized On-Resistance vs. Temperature

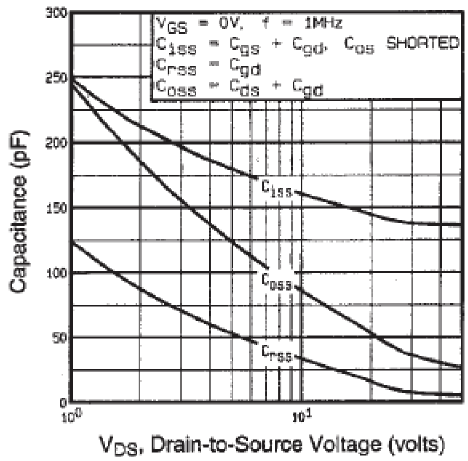


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

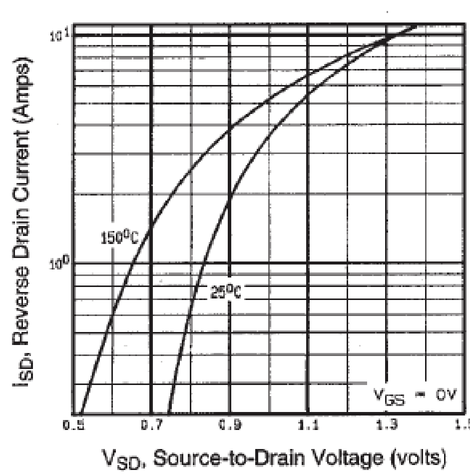


Fig. 7 - Typical Source-Drain Diode Forward Voltage

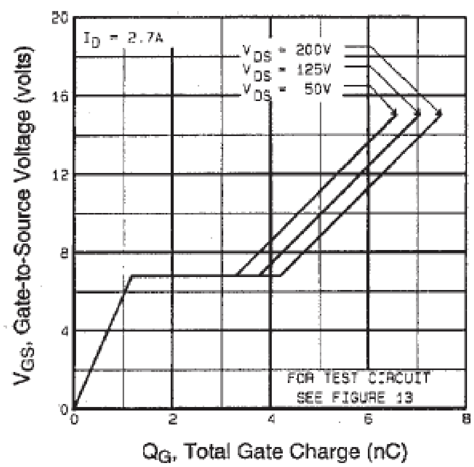


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

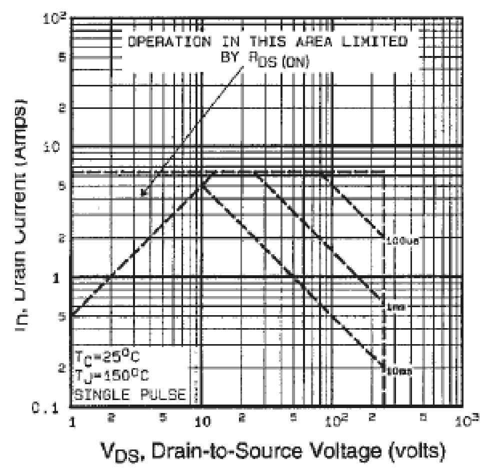


Fig. 8 - Maximum Safe Operating Area

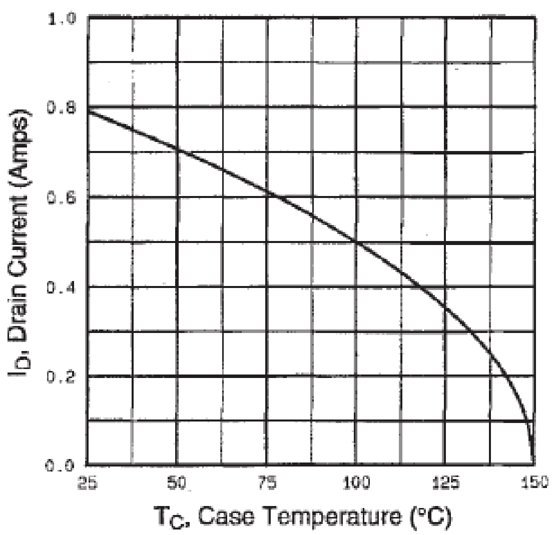


Fig. 9 - Maximum Drain Current vs. Case Temperature

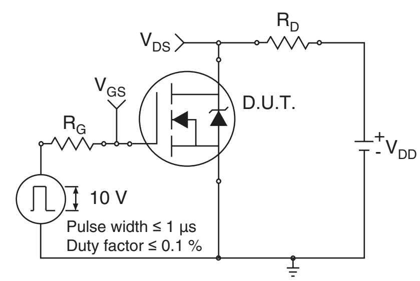


Fig. 10a - Switching Time Test Circuit

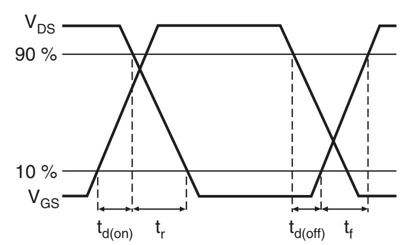


Fig. 10b - Switching Time Waveforms

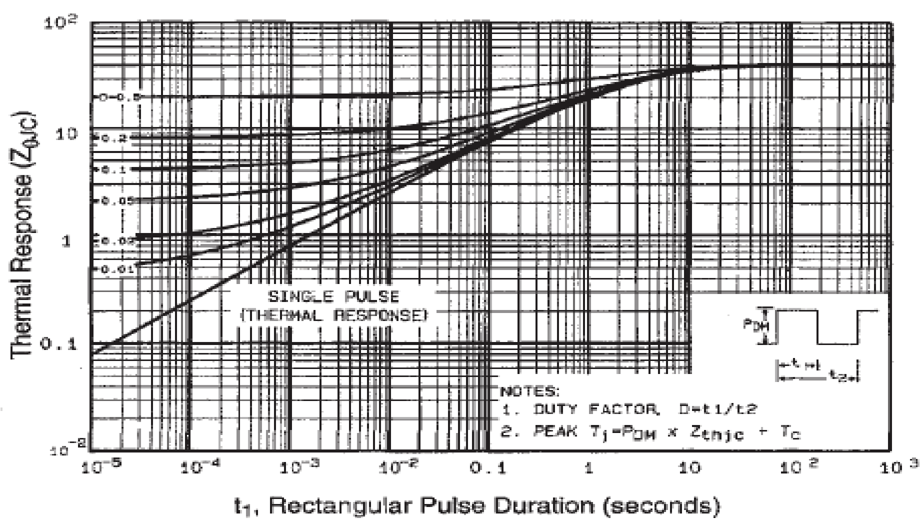


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

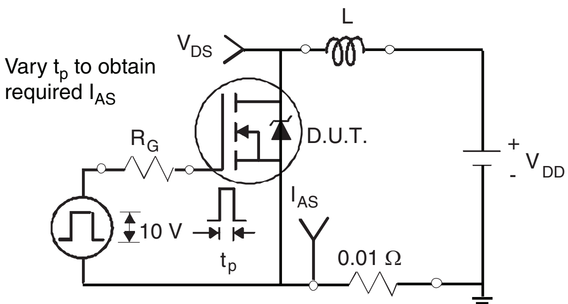


Fig. 12a - Unclamped Inductive Test Circuit

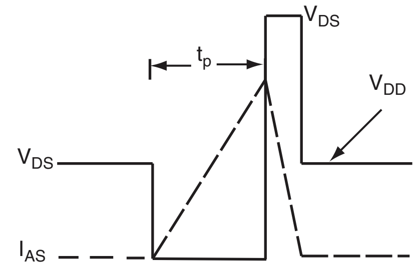


Fig. 12b - Unclamped Inductive Waveforms

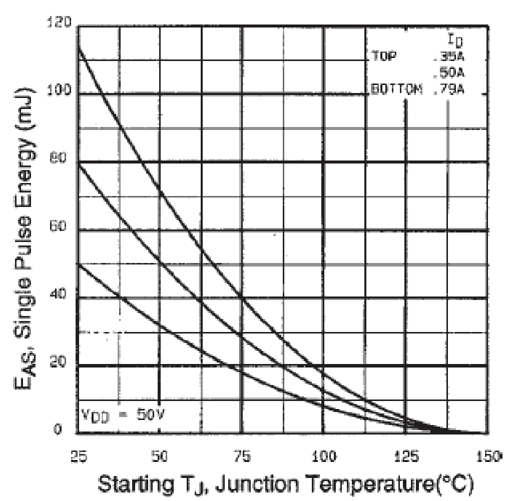


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

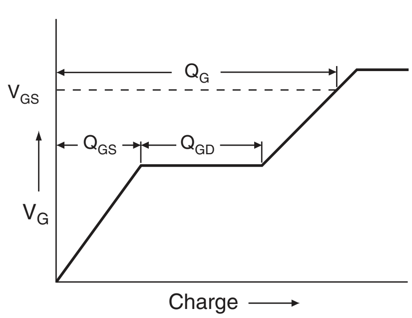


Fig. 13a - Basic Gate Charge Waveform

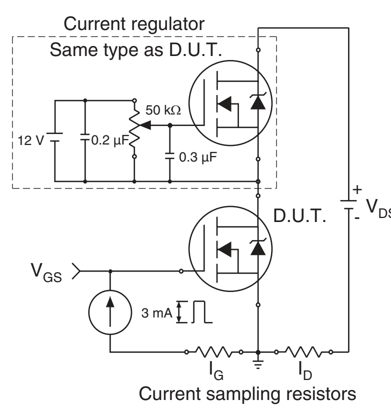


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

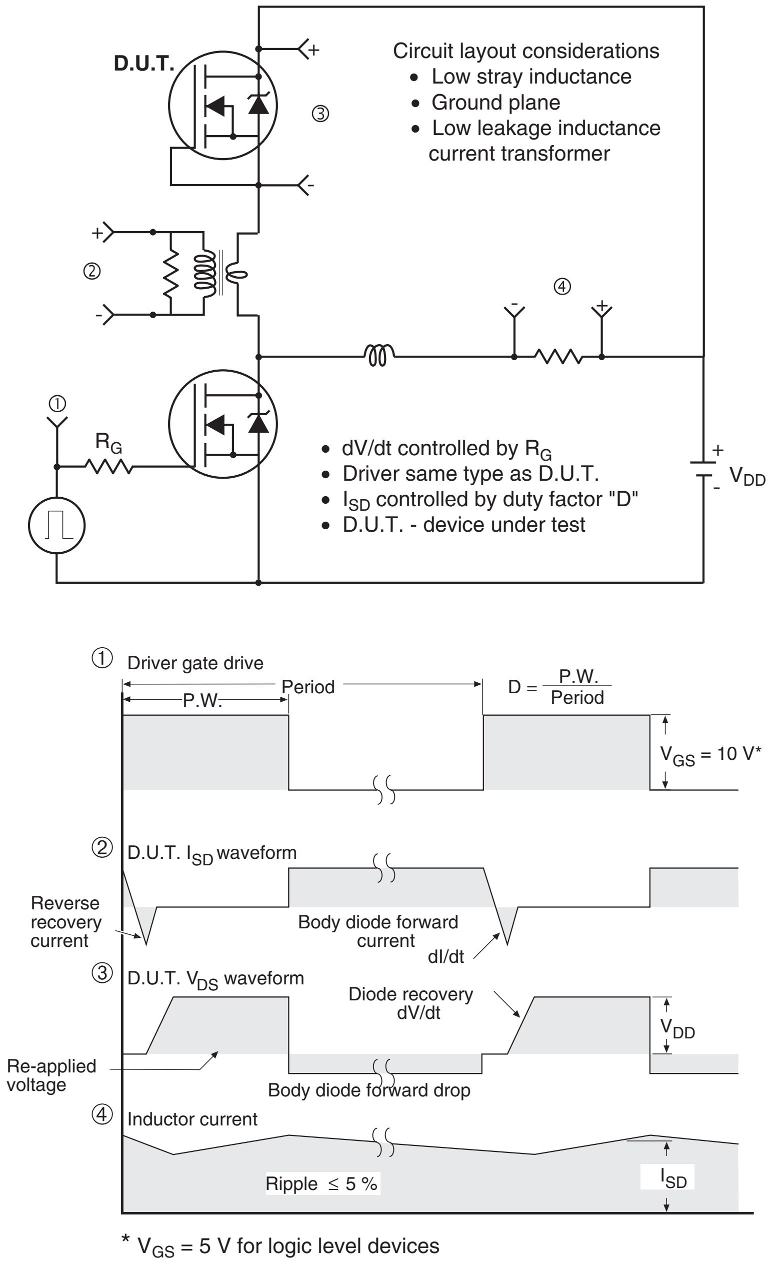


Fig.14 - For N-Channel

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