

International I^{OR} Rectifier

AUTOMOTIVE MOSFET

IRF1607PbF

PD -95487

Typical Applications

- 42 Volts Automotive Electrical Systems
- Electrical Power Steering (EPS)
- Integrated Starter Alternator
- Lead-Free

Benefits

- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Automotive [Q101] Qualified

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	142@	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	100@	
I _{DM}	Pulsed Drain Current ①	570	
P _D @ T _C = 25°C	Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	1250	mJ
I _{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	
E _{AR}	Repetitive Avalanche Energy ②	mJ	
dv/dt	Peak Diode Recovery dv/dt ③	5.2	V/ns
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

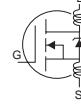
Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.40	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

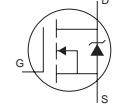
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.086	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	0.0058	0.0075	Ω	$V_{\text{GS}} = 10\text{V}$, $I_D = 85\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = 10\text{V}$, $I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	79	—	—	S	$V_{\text{DS}} = 25\text{V}$, $I_D = 85\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 75\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 60\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
Q_g	Total Gate Charge	—	210	320	nC	$I_D = 85\text{A}$
Q_{gs}	Gate-to-Source Charge	—	45	68		$V_{\text{DS}} = 60\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	73	110		$V_{\text{GS}} = 10\text{V}$
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	22	—	ns	$V_{\text{DD}} = 38\text{V}$
t_r	Rise Time	—	130	—		$I_D = 85\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	84	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	86	—		$V_{\text{GS}} = 10\text{V}$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	7750	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	1230	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	310	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	5770	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 1.0\text{V}$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	790	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 60\text{V}$, $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance ⑤	—	1420	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 60V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	142⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	570		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 85\text{A}$, $V_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	130	200	ns	$T_J = 25^\circ\text{C}$, $I_F = 85\text{A}$
Q_{rr}	Reverse Recovery Charge	—	690	1040	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.21\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 85\text{A}$, $V_{GS}=10\text{V}$ (See Figure 12).
- ③ $I_{SD} \leq 85\text{A}$, $dI/dt \leq 310\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by $T_{J\text{max}}$, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

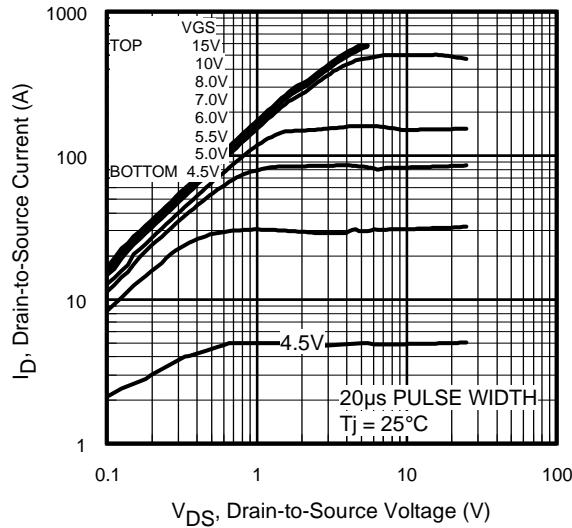


Fig 1. Typical Output Characteristics

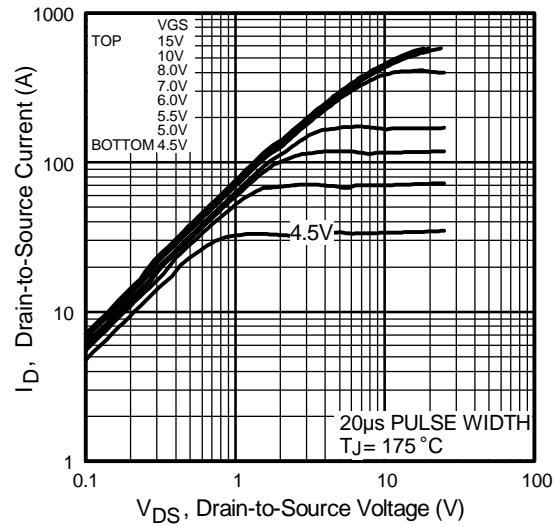


Fig 2. Typical Output Characteristics

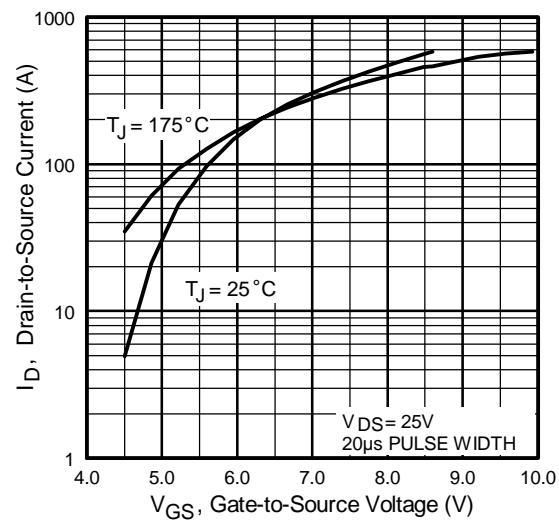


Fig 3. Typical Transfer Characteristics

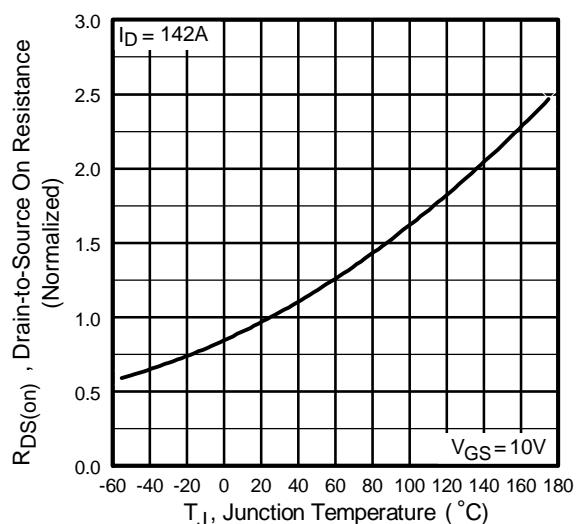


Fig 4. Normalized On-Resistance
Vs. Temperature

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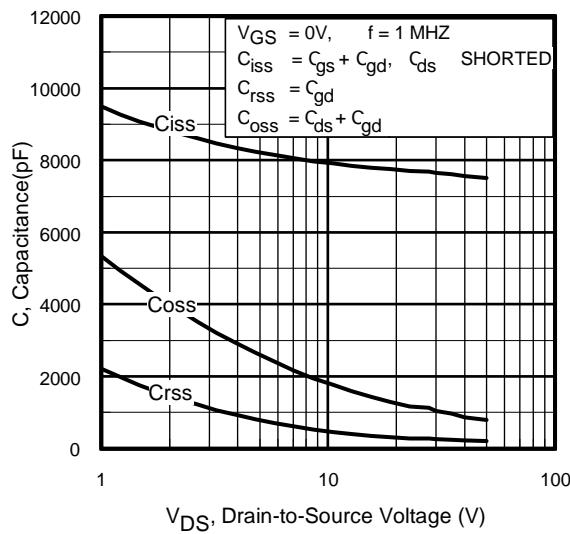


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

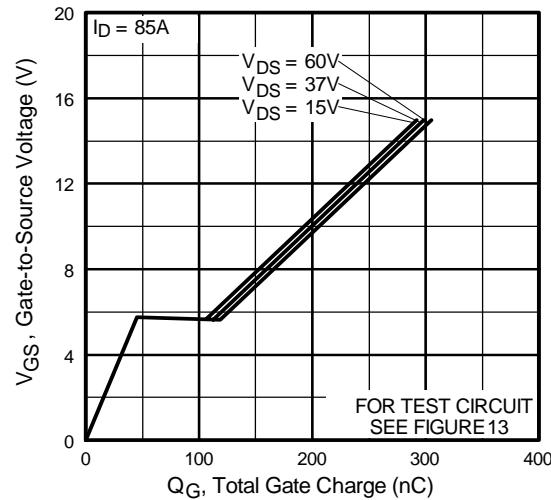


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

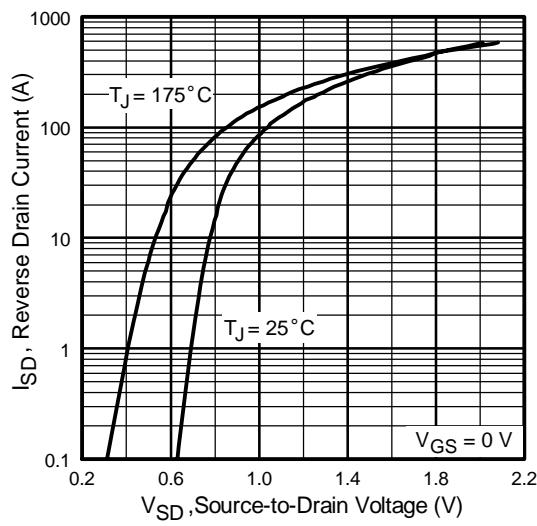


Fig 7. Typical Source-Drain Diode
Forward Voltage

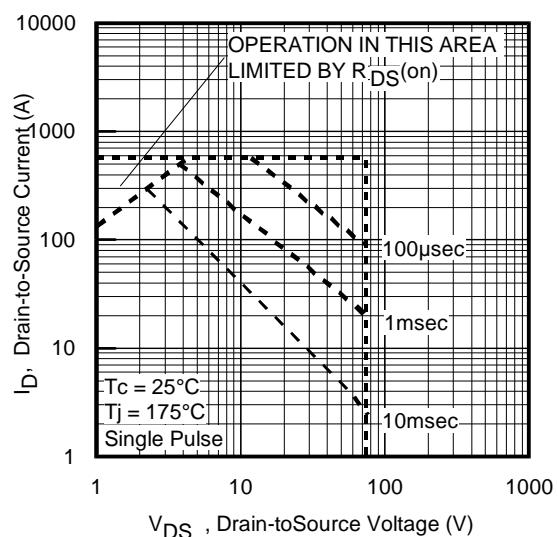


Fig 8. Maximum Safe Operating Area

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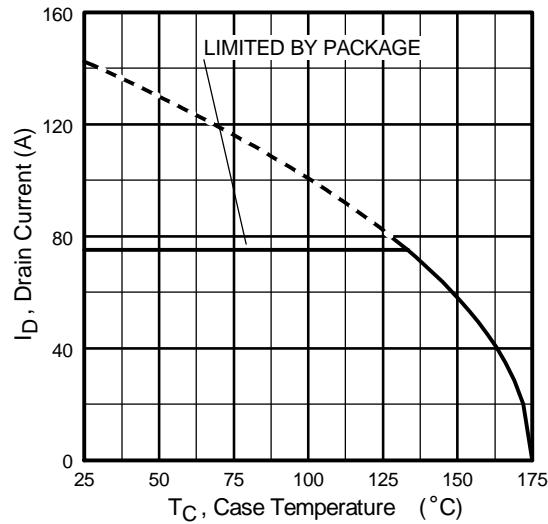


Fig 9. Maximum Drain Current Vs.
Case Temperature

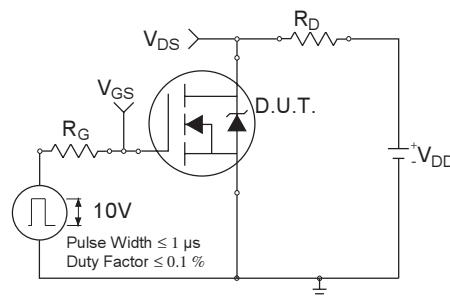


Fig 10a. Switching Time Test Circuit

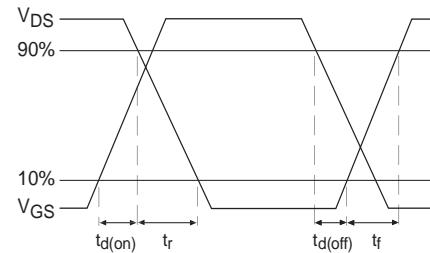


Fig 10b. Switching Time Waveforms

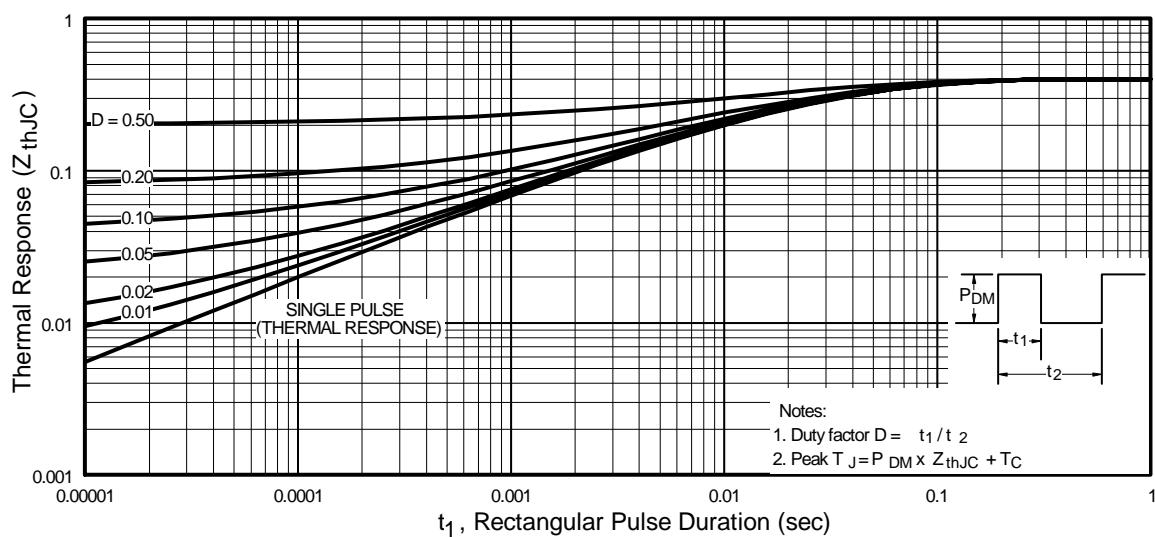


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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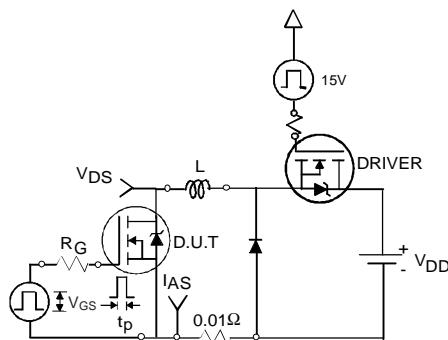


Fig 12a. Unclamped Inductive Test Circuit

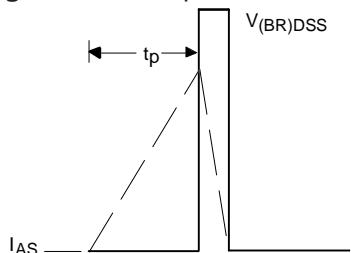


Fig 12b. Unclamped Inductive Waveforms

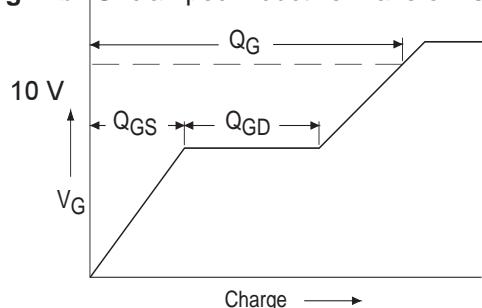


Fig 13a. Basic Gate Charge Waveform

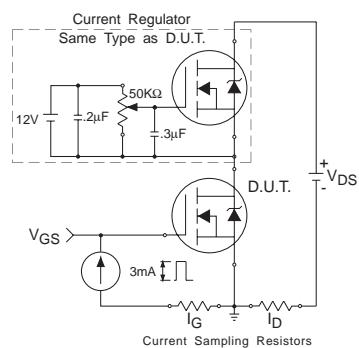


Fig 13b. Gate Charge Test Circuit

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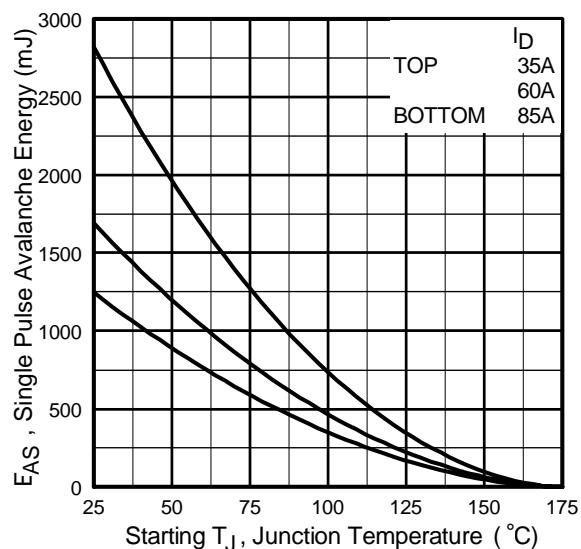


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

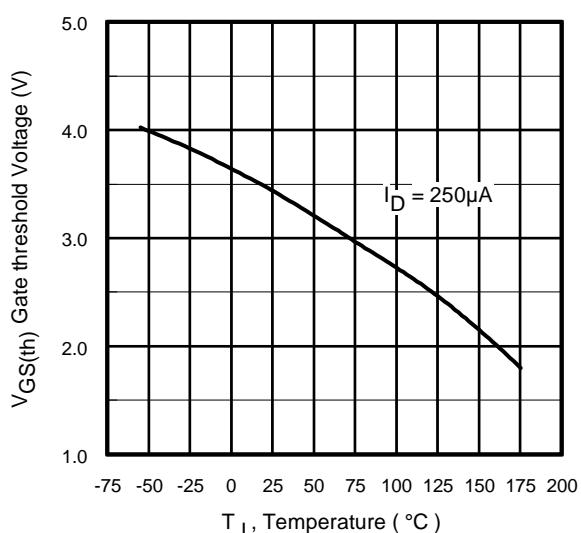


Fig 14. Threshold Voltage Vs. Temperature
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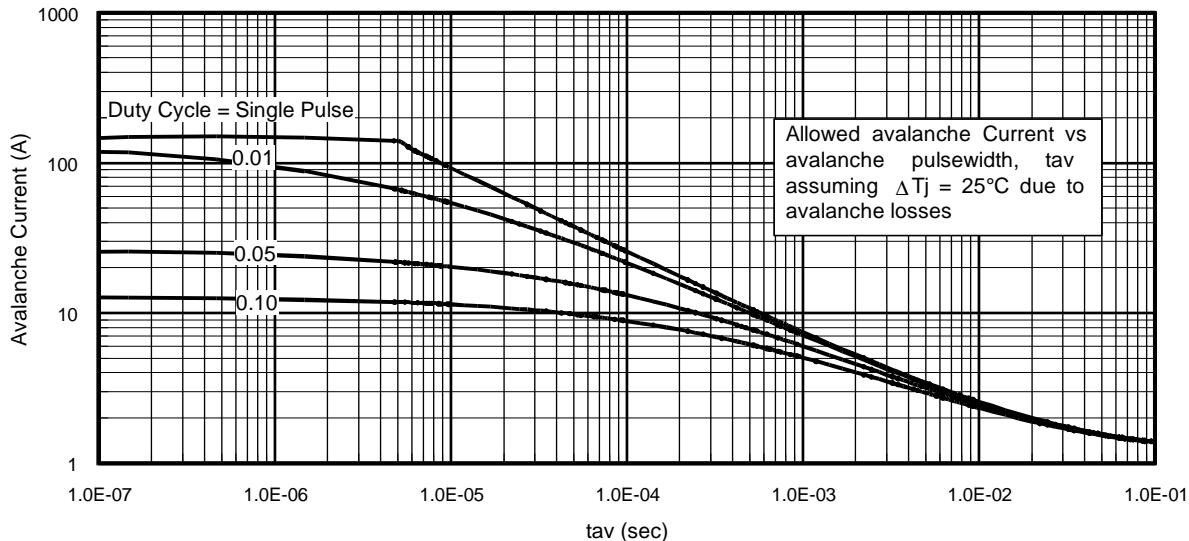


Fig 15. Typical Avalanche Current Vs.Pulsewidth

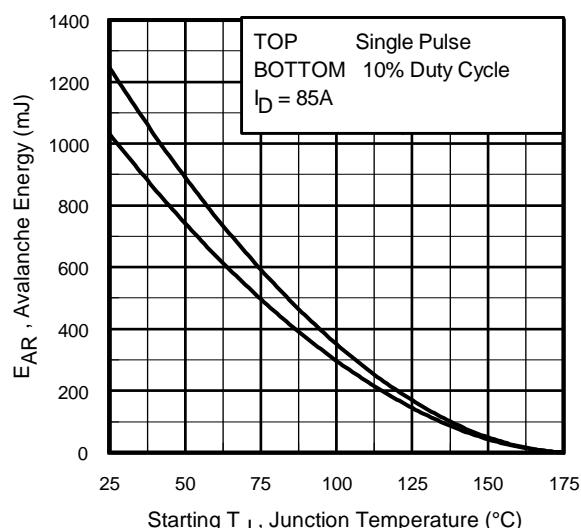


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
 (For further info, see AN-1005 at www.irf.com)**

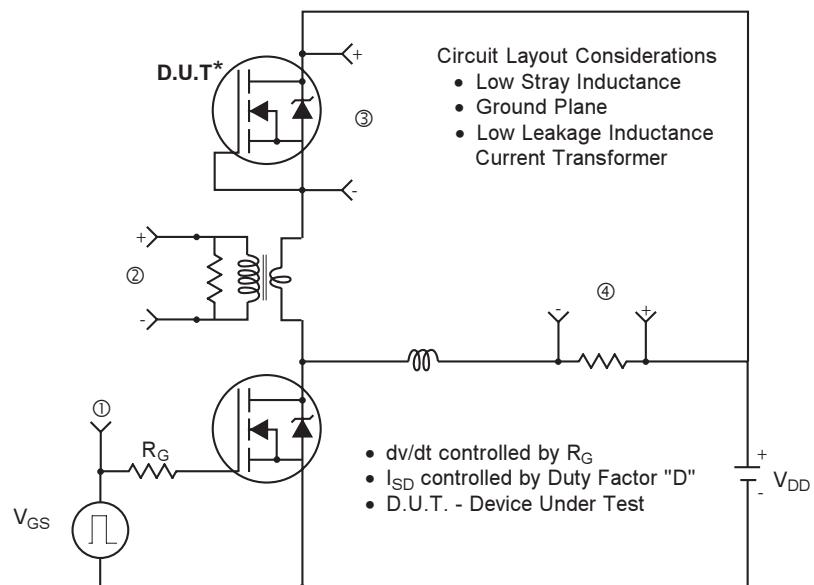
1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
 4. $P_D(\text{ave})$ = Average power dissipation per single avalanche pulse.
 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
 6. I_{av} = Allowable avalanche current.
 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
- t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f_{av}$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_D(\text{ave}) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

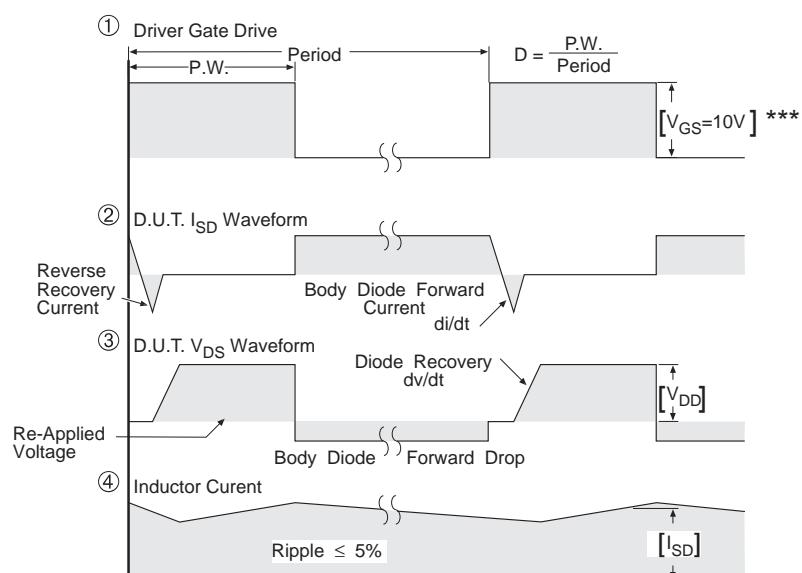
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_D(\text{ave}) \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0\text{V}$ for Logic Level and 3V Drive Devices

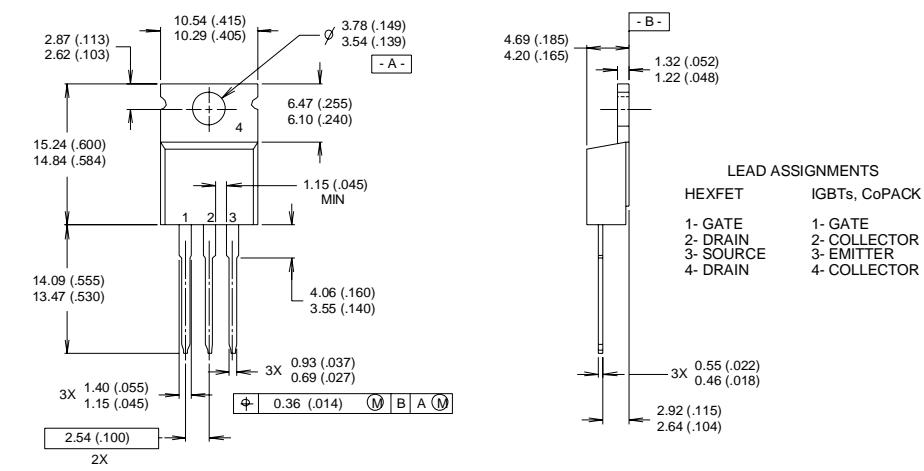
Fig 17. For N-channel HEXFET® power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

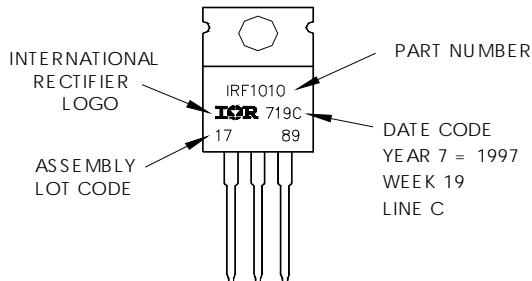
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010

LOT CODE 1789

ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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