



IRFR1N60A, IRFU1N60A, SiHFR1N60A, SiHFU1N60A

Vishay Siliconix

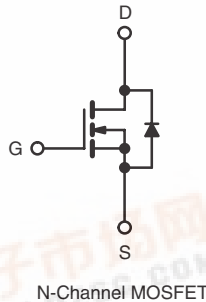
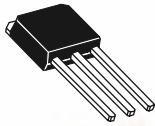
Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Max.) (Ω)	$V_{GS} = 10\text{ V}$ 7.0
Q_g (Max.) (nC)	14
Q_{gs} (nC)	2.7
Q_{gd} (nC)	8.1
Configuration	Single

DPAK (TO-252)



IPAK (TO-251)



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Lead (Pb)-free Available



RoHS* COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- Power Factor Correction

TYPICAL SMPS TOPOLOGIES

- Low Power Single Transistor Flyback

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR1N60APbF	IRFR1N60ATRLPbF ^a	IRFR1N60ATRPbF ^a	IRFR1N60ATRRPbF ^a	IRFU1N60APbF
	SiHFR1N60A-E3	SiHFR1N60ATL-E3 ^a	SiHFR1N60AT-E3 ^a	SiHFR1N60ATR-E3 ^a	SiHFU1N60A-E3
SnPb	IRFR1N60A	-	IRFR1N60ATR ^a	-	IRFU1N60A
	SiHFR1N60A	-	SiHFR1N60AT ^a	-	SiHFU1N60A

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	600	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current ^a	I_{DM}	5.6		
Linear Derating Factor		0.28	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b	E_{AS}	93	mJ	
Repetitive Avalanche Current ^a	I_{AR}	1.4	A	
Repetitive Avalanche Energy ^a	E_{AR}	3.6	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	36	W
Peak Diode Recovery dV/dt ^c		dV/dt	3.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 95\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 1.4\text{ A}$ (see fig. 12).
- $I_{SD} \leq 1.4\text{ A}$, $dI/dt \leq 180\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

*Pb-containing terminations are not RoHS compliant, exemptions may apply

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
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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0		
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.84\text{ A}^b$	-	-	7.0	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 0.84\text{ A}$	0.88	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	229	-	pF	
Output Capacitance	C_{oss}		-	32.6	-		
Reverse Transfer Capacitance	C_{rss}		-	2.4	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	320		-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	11.5		-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	130	-		
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}, V_{DS} = 400\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	14	nC	
Gate-Source Charge	Q_{gs}		-	-	2.7		
Gate-Drain Charge	Q_{gd}		-	-	8.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 1.4\text{ A}, R_G = 2.15\text{ }\Omega, R_D = 178\text{ }\Omega, \text{ see fig. 10}^b$	-	9.8	-	ns	
Rise Time	t_r		-	14	-		
Turn-Off Delay Time	$t_{d(off)}$		-	18	-		
Fall Time	t_f		-	20	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.4	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	5.6		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.4\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 1.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	290	440	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	510	760	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

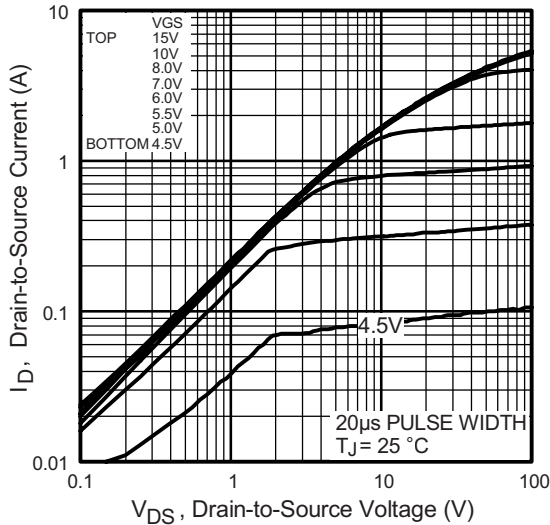


Fig. 1 - Typical Output Characteristics

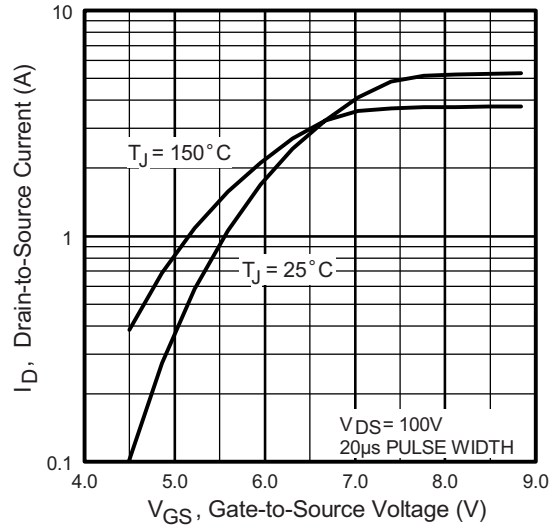


Fig. 3 - Typical Transfer Characteristics

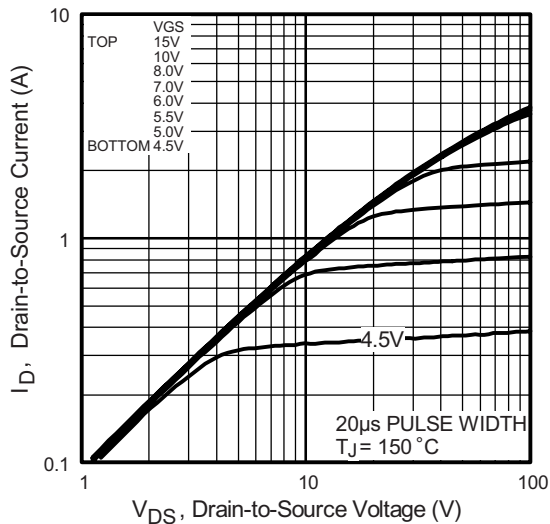


Fig. 2 - Typical Output Characteristics

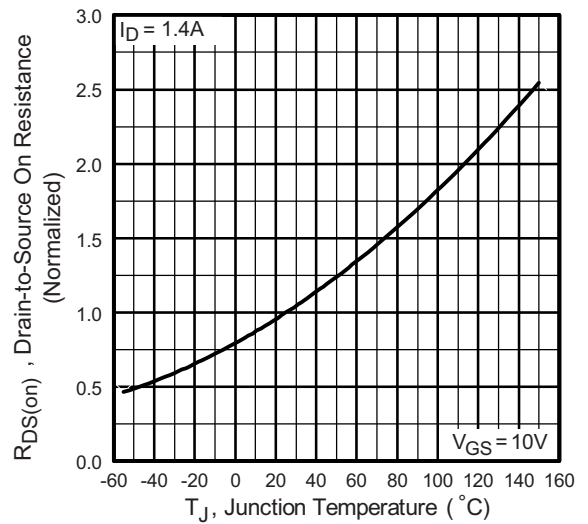


Fig. 4 - Normalized On-Resistance vs. Temperature

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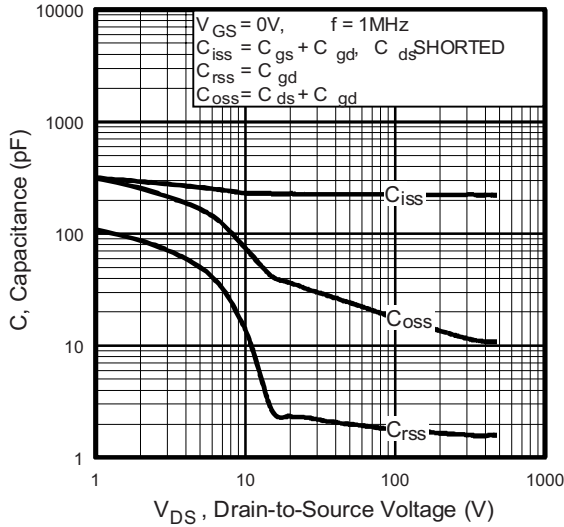


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

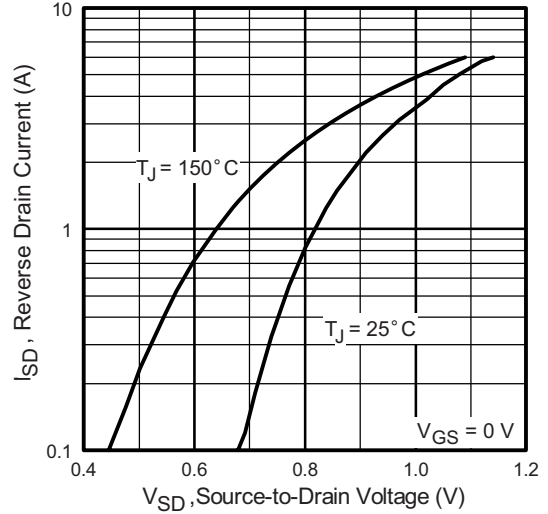


Fig. 7 - Typical Source-Drain Diode Forward Voltage

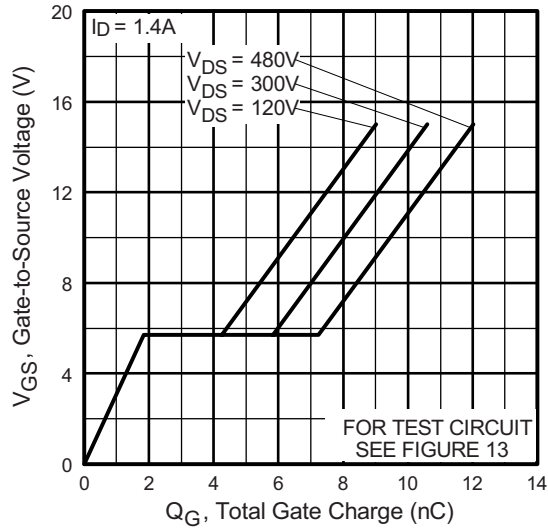


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

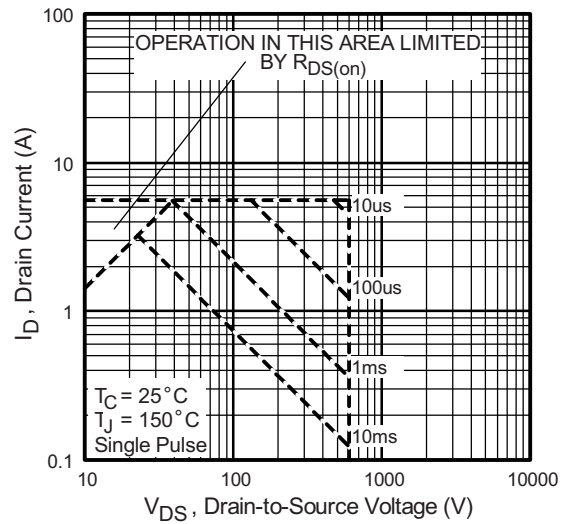


Fig. 8 - Maximum Safe Operating Area



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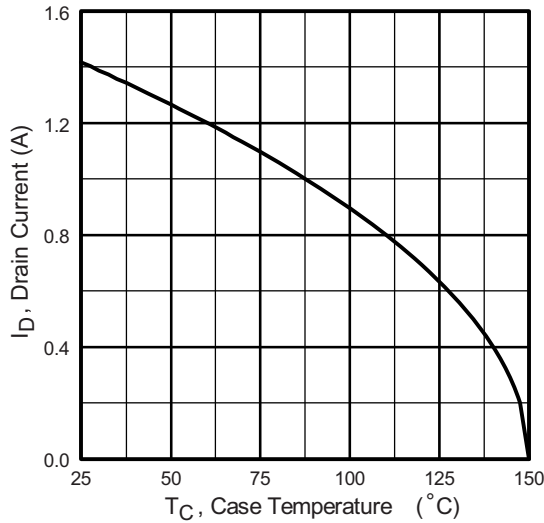


Fig. 9 - Maximum Drain Current vs. Case Temperature

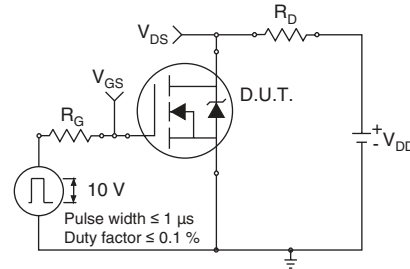


Fig. 10a - Switching Time Test Circuit

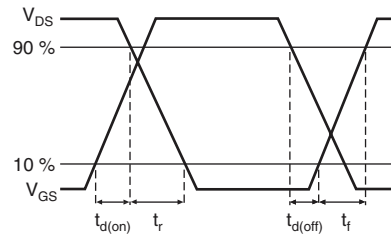


Fig. 10b - Switching Time Waveforms

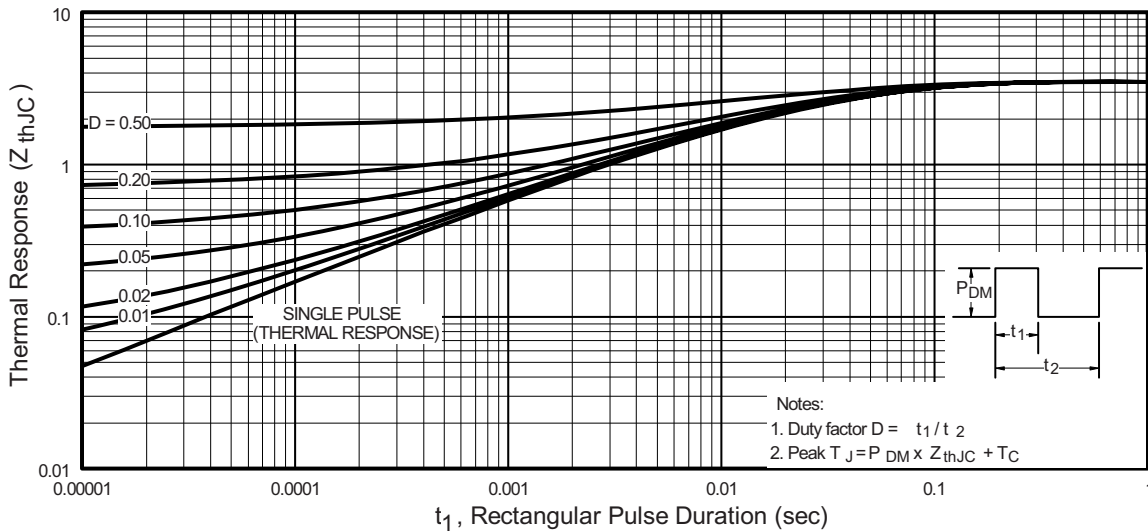


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

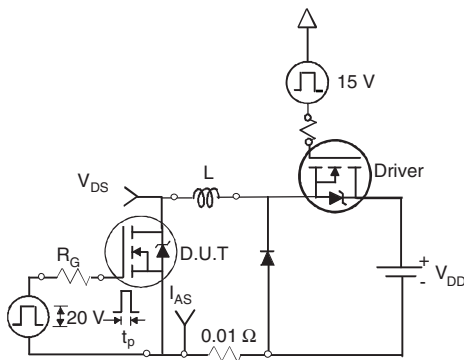


Fig. 12a - Unclamped Inductive Test Circuit

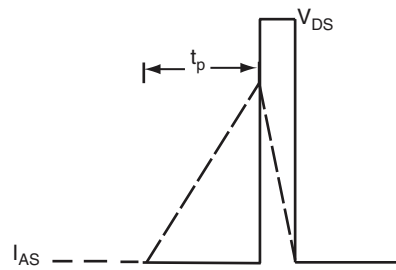


Fig. 12b - Unclamped Inductive Waveforms

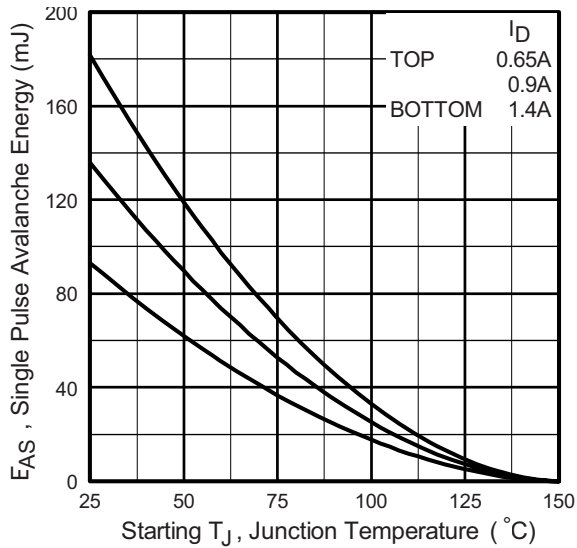


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

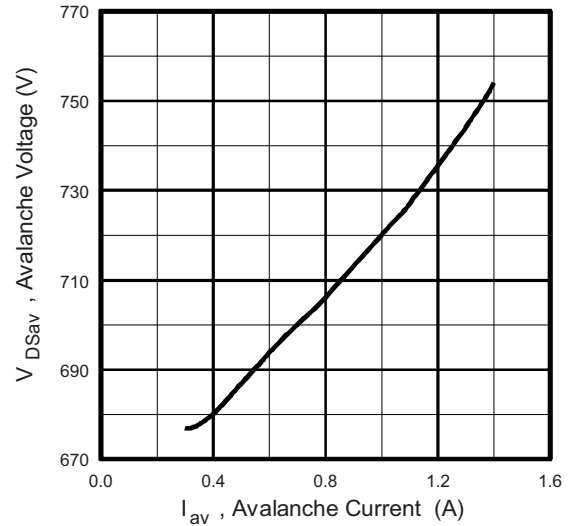


Fig. 12d - Basic Gate Charge Waveform

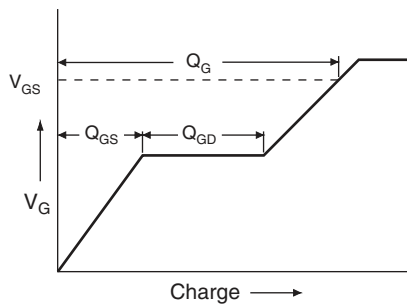


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

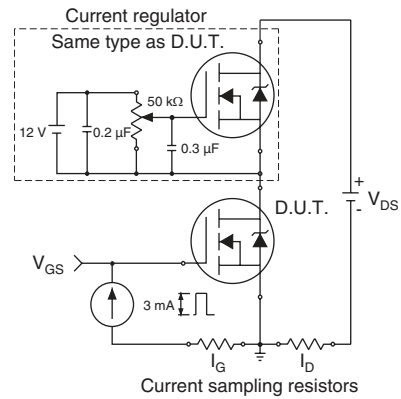


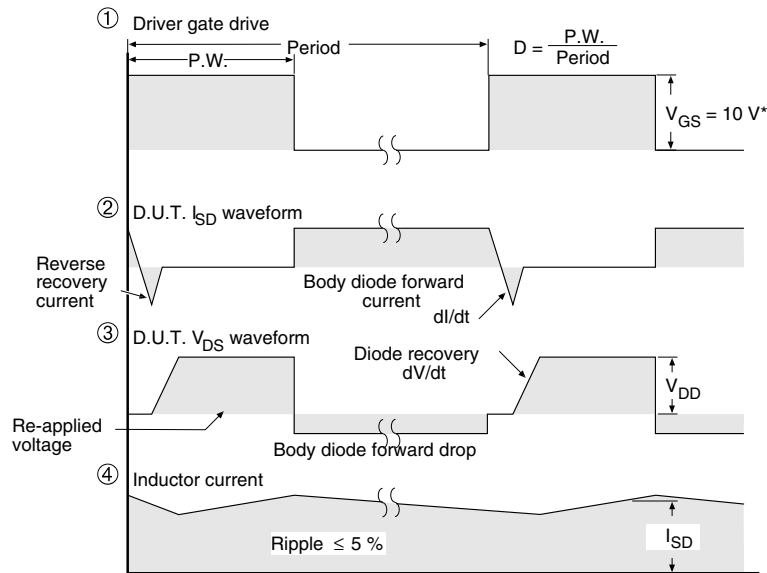
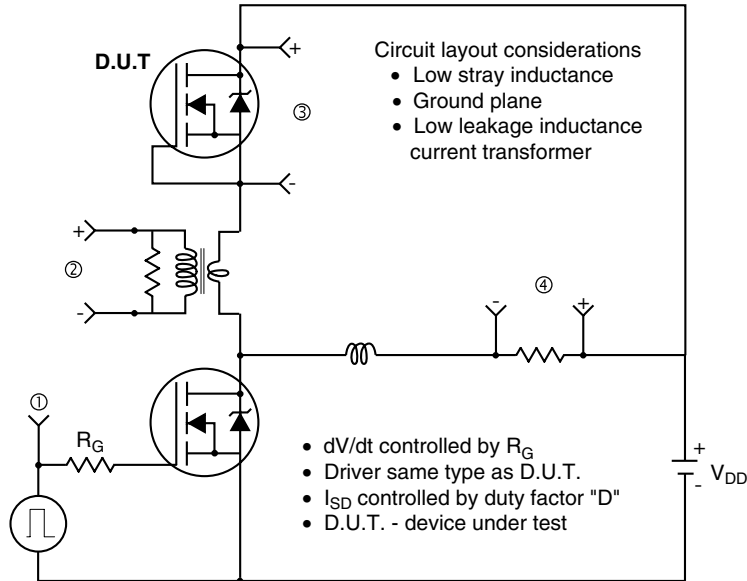
Fig. 13b - Gate Charge Test Circuit



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Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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