

International IOR Rectifier

PD - 96902A

IRFB4410

IRFS4410

IRFSL4410

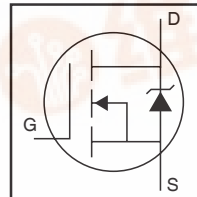
Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

HEXFET® Power MOSFET



V_{DS}		100V
$R_{DS(on)}$	typ.	8.0mΩ
	max.	10mΩ
I_D		96A



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	96①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	68①	
I_{DM}	Pulsed Drain Current ②	380	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	19	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	220	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 16a, 16b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.61	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface, TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑦	—	62	
	Junction-to-Ambient (PCB Mount), D²Pak ⑧⑨	—	40	



Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.094	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	8.0	10	m Ω	$V_{GS} = 10V, I_D = 58A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
R_G	Gate Input Resistance	—	1.5	—	Ω	$f = 1MHz$, open drain

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	120	—	—	S	$V_{DS} = 50V, I_D = 58A$
Q_g	Total Gate Charge	—	120	180	nC	$I_D = 58A$
Q_{gs}	Gate-to-Source Charge	—	31	—		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	44	—		$V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 65V$
t_r	Rise Time	—	80	—		$I_D = 58A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 4.1\Omega$
t_f	Fall Time	—	50	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	5150	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	360	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	190	—		$f = 1.0MHz$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	420	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑦, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	500	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑧, See Fig. 5

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	96①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	380	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 58A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	38	56	ns	$T_J = 25^\circ\text{C}$ $V_R = 85V,$
		—	51	77		$T_J = 125^\circ\text{C}$ $I_F = 58A$
Q_{rr}	Reverse Recovery Charge	—	61	92	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	110	170		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.8	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.14mH$
 $R_G = 25\Omega$, $I_{AS} = 58A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 58A$, $di/dt \leq 650A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_g is measured at T_J approximately 90°C .

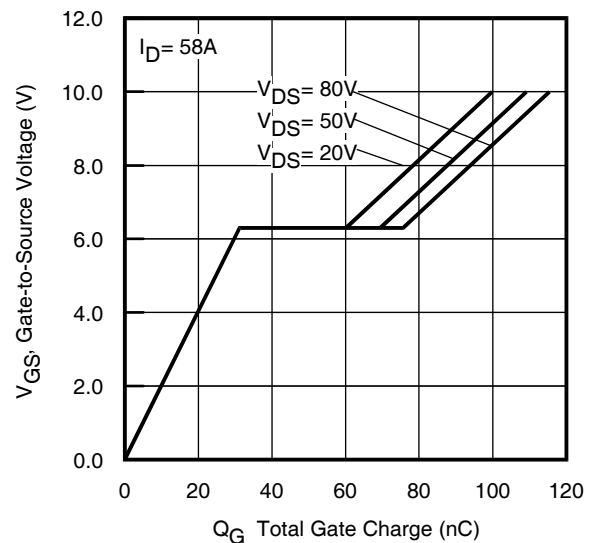
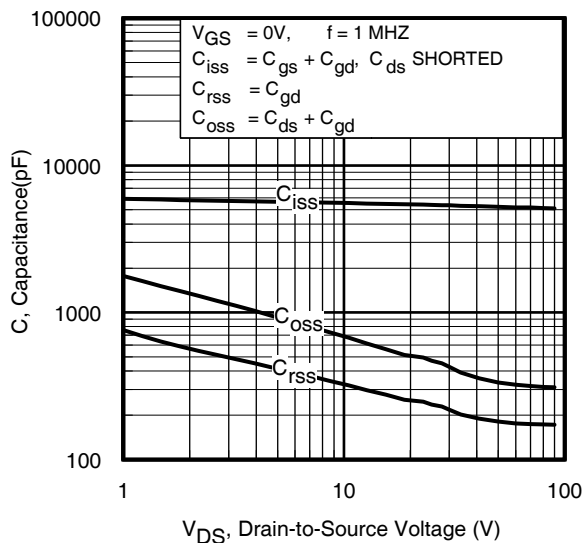
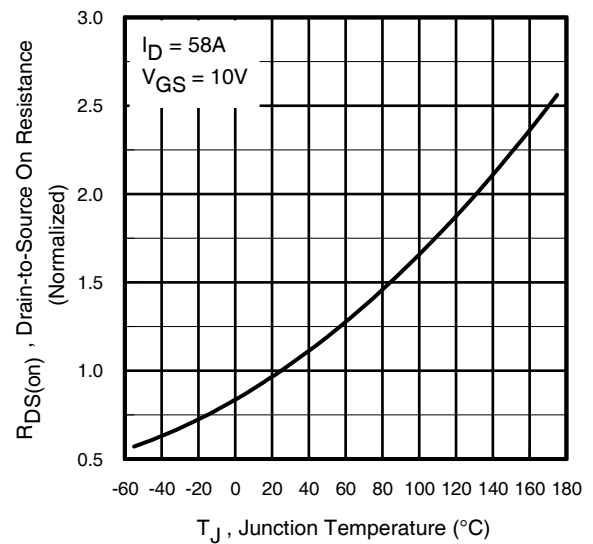
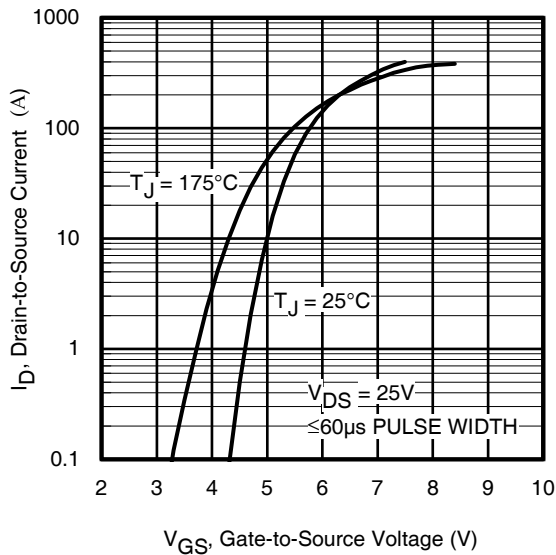
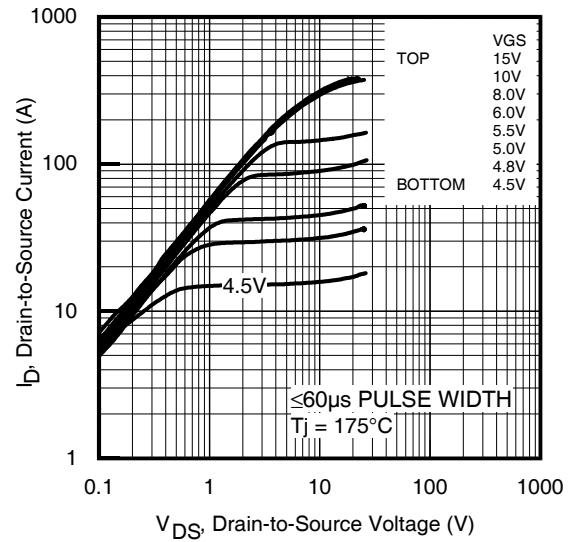
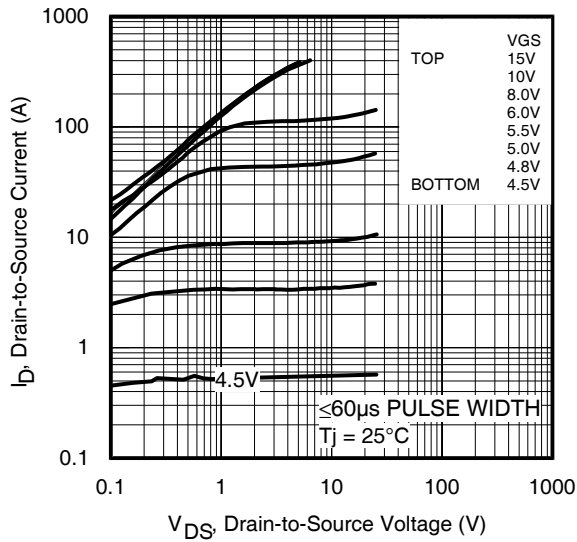


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

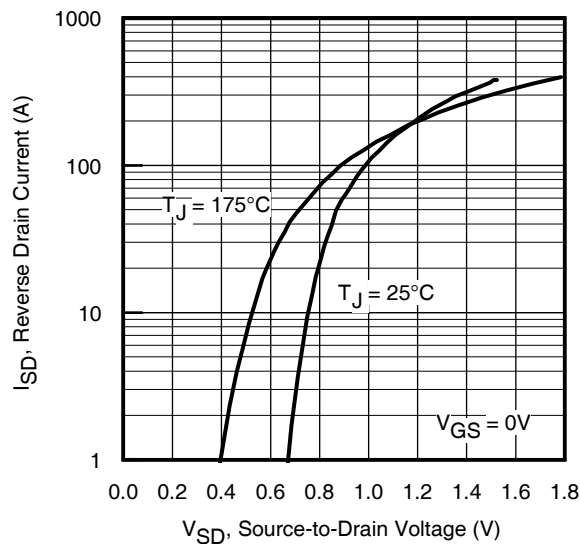


Fig 7. Typical Source-Drain Diode Forward Voltage

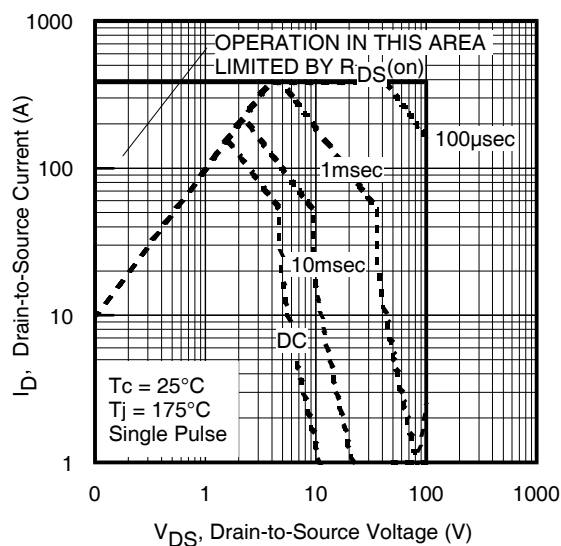


Fig 8. Maximum Safe Operating Area

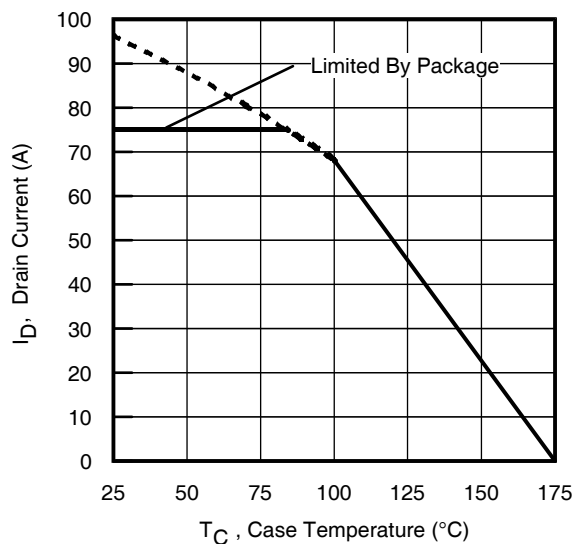


Fig 9. Maximum Drain Current vs. Case Temperature

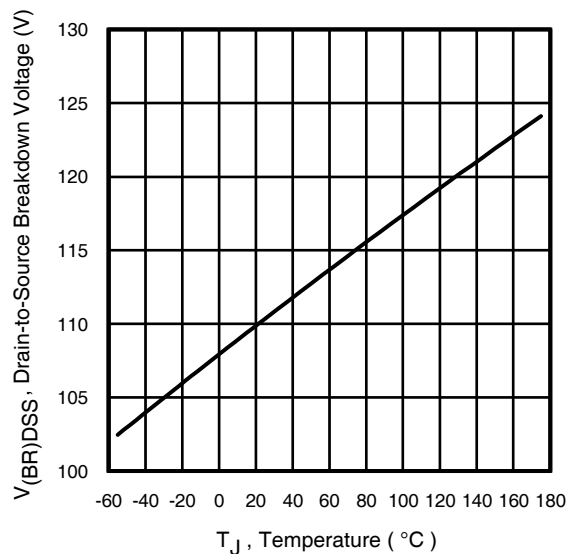


Fig 10. Drain-to-Source Breakdown Voltage

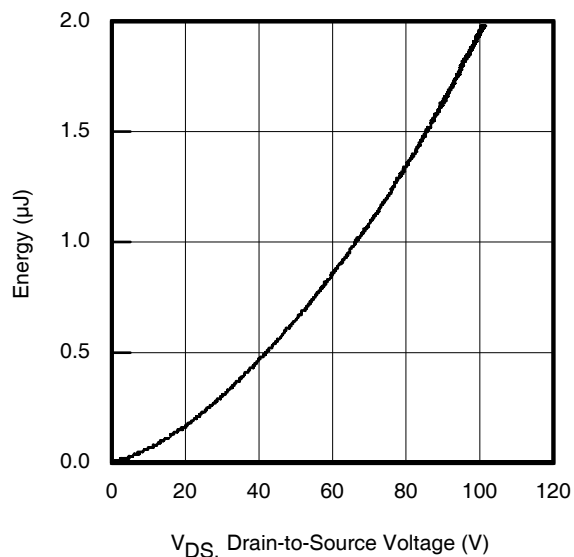


Fig 11. Typical C_{OSS} Stored Energy

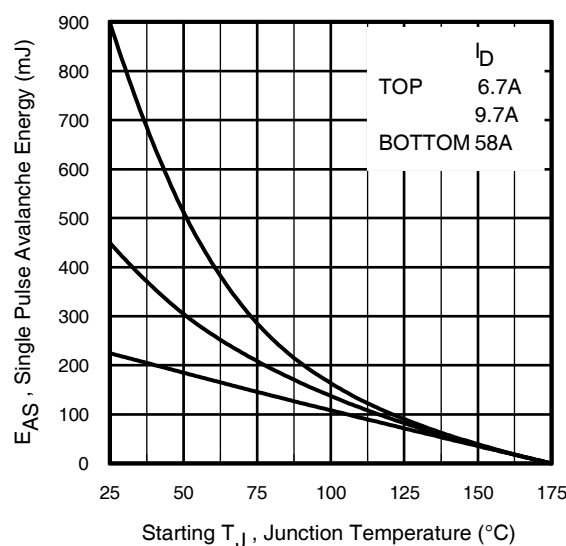


Fig 12. Maximum Avalanche Energy vs. Drain Current

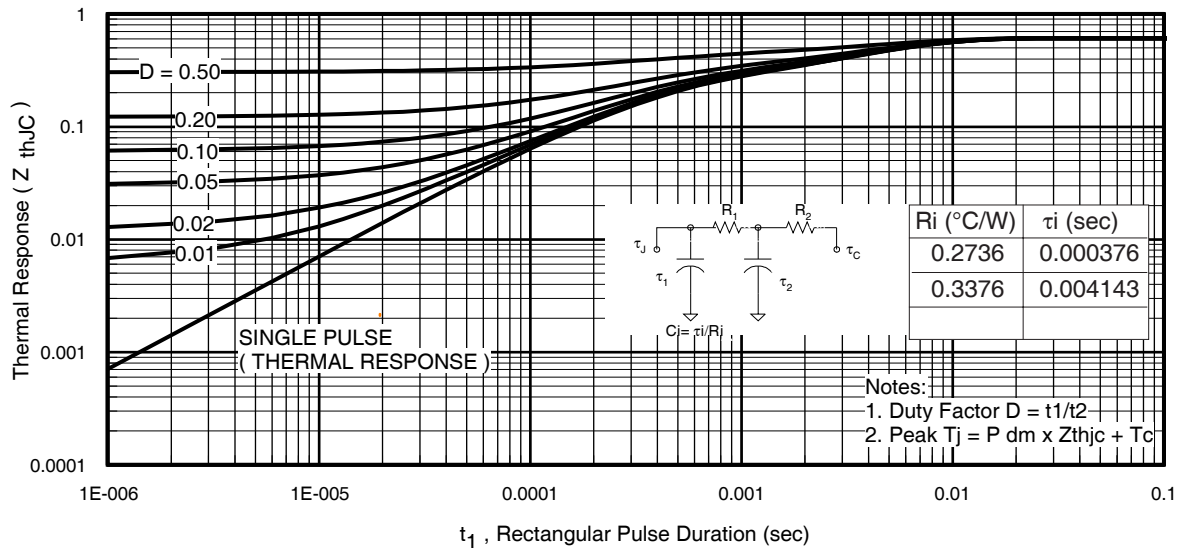


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

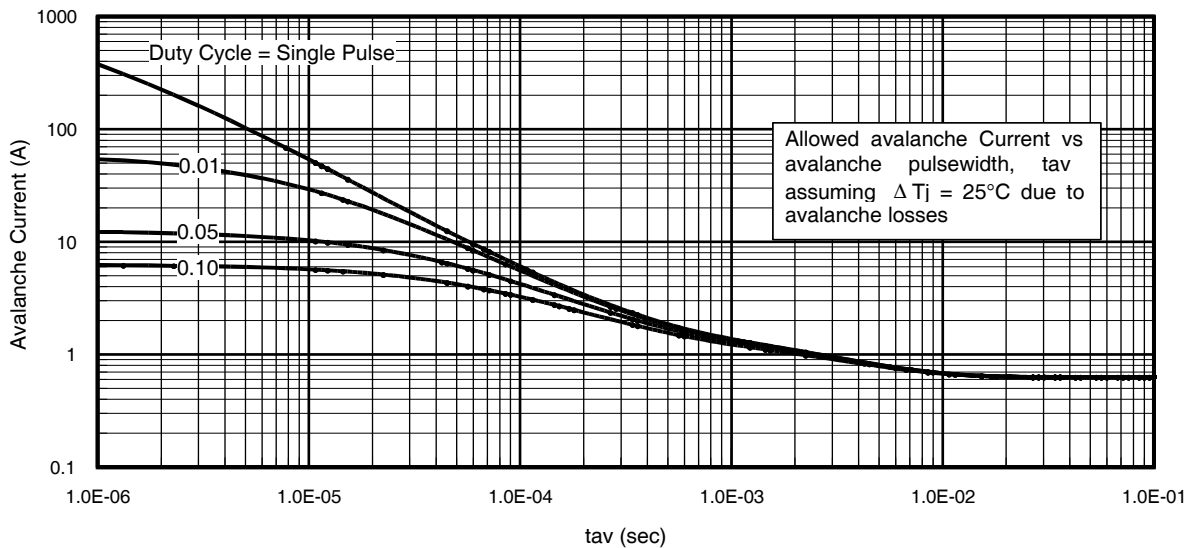
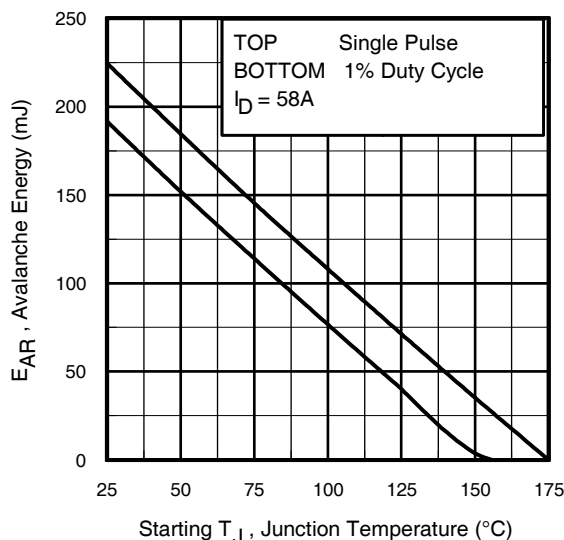


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:

Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.

4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

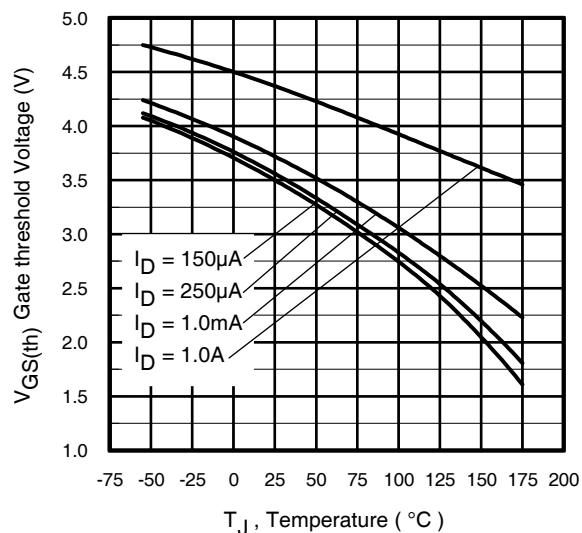


Fig. 16. Threshold Voltage vs. Temperature

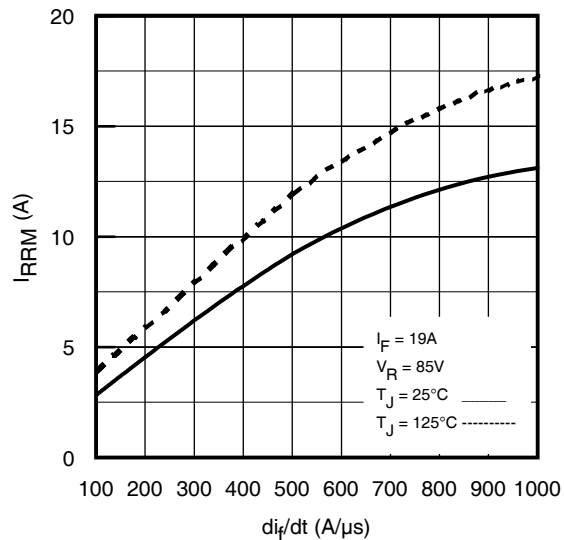


Fig. 17 - Typical Recovery Current vs. di_T/dt

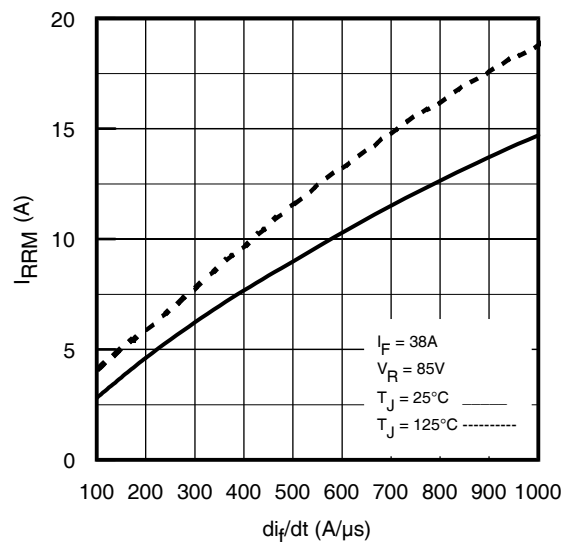


Fig. 18 - Typical Recovery Current vs. di_T/dt

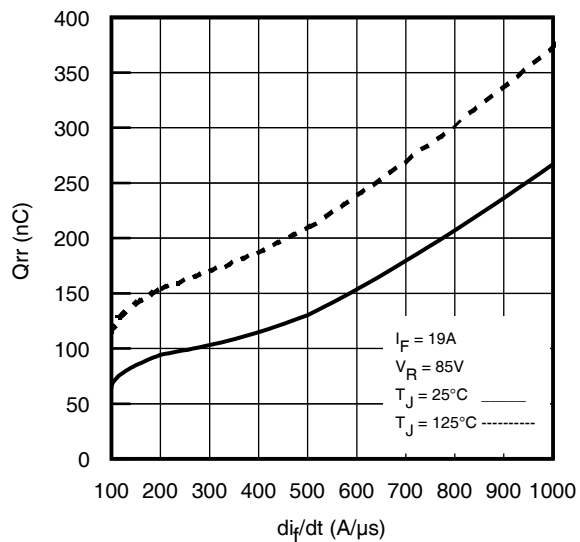


Fig. 19 - Typical Stored Charge vs. di_T/dt

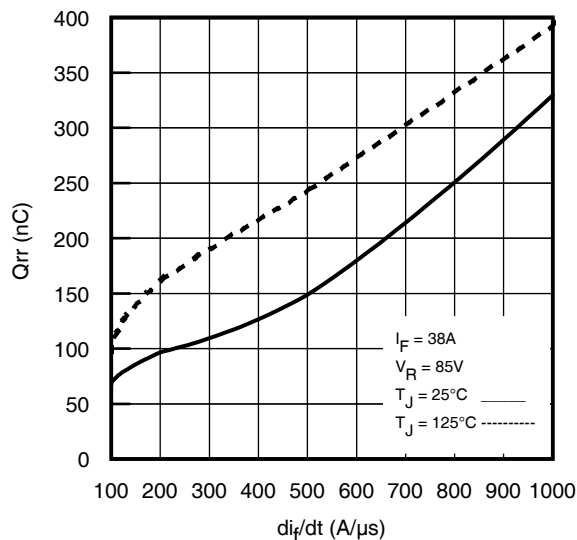


Fig. 20 - Typical Stored Charge vs. di_T/dt

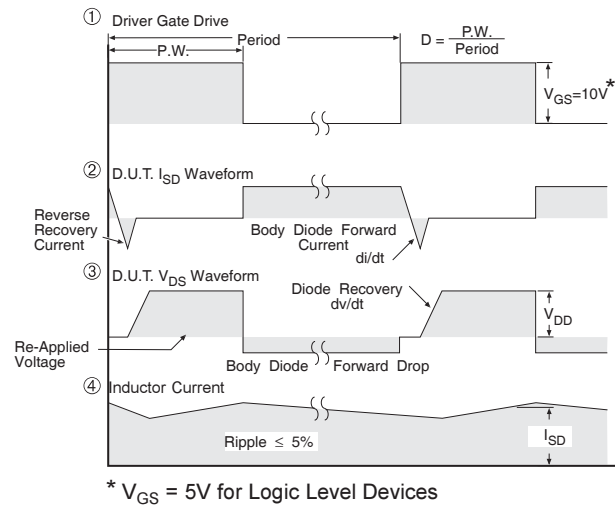
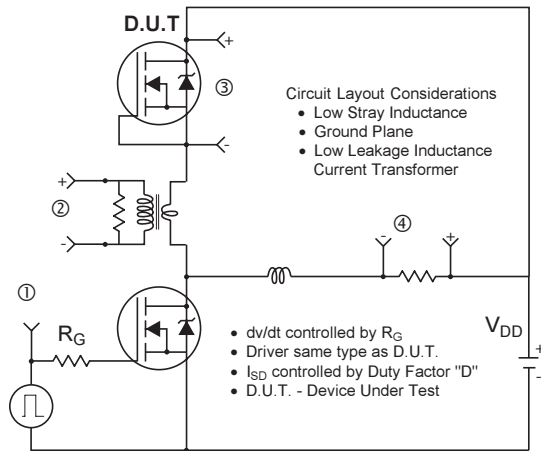


Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

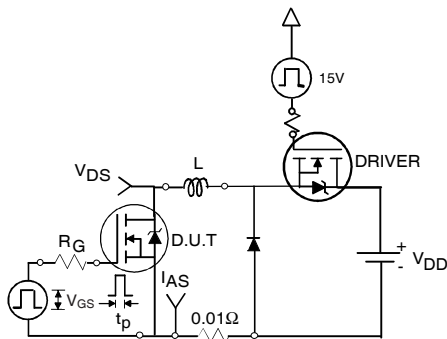


Fig 21a. Unclamped Inductive Test Circuit

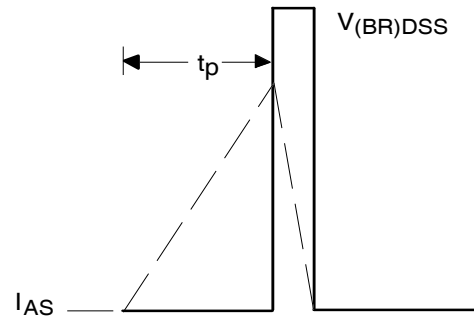


Fig 21b. Unclamped Inductive Waveforms

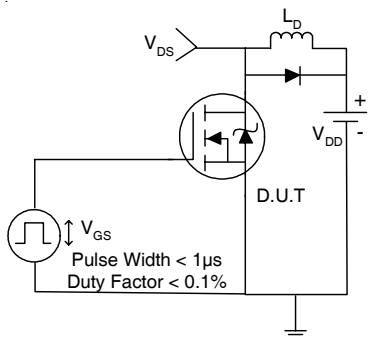


Fig 22a. Switching Time Test Circuit

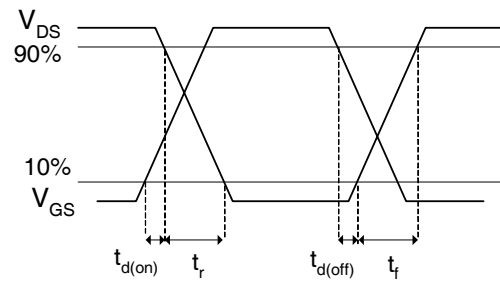


Fig 22b. Switching Time Waveforms

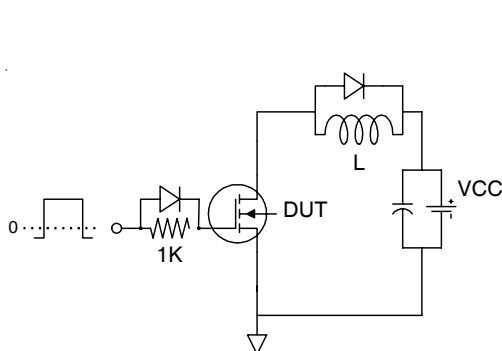


Fig 23a. Gate Charge Test Circuit

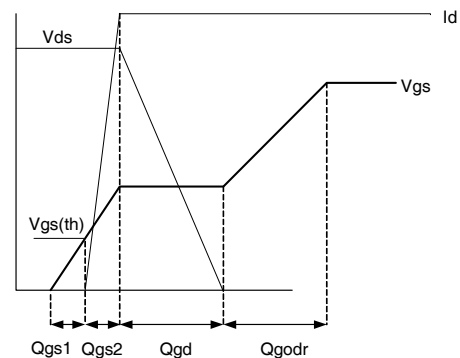
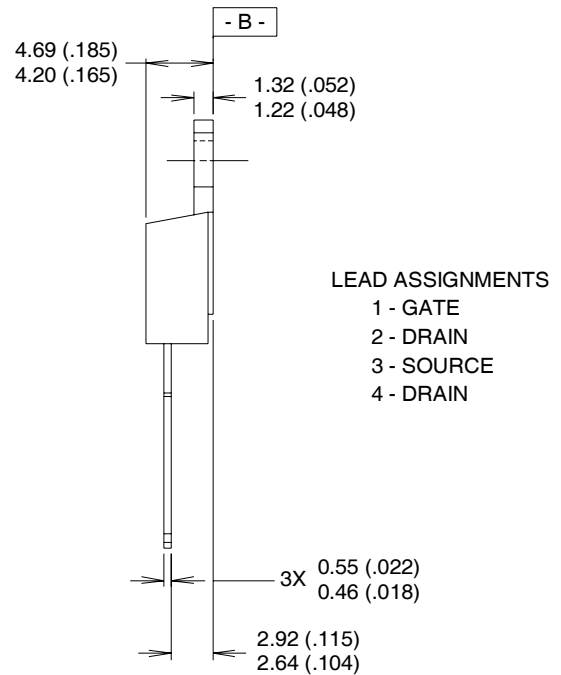


Fig 23b. Gate Charge Waveform

International
IOR Rectifier

Dimensions are shown in millimeters (inches)

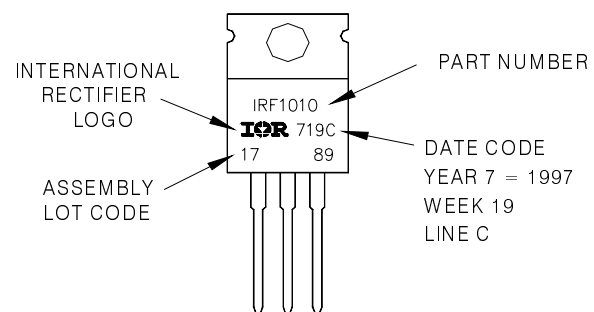


NOTES:

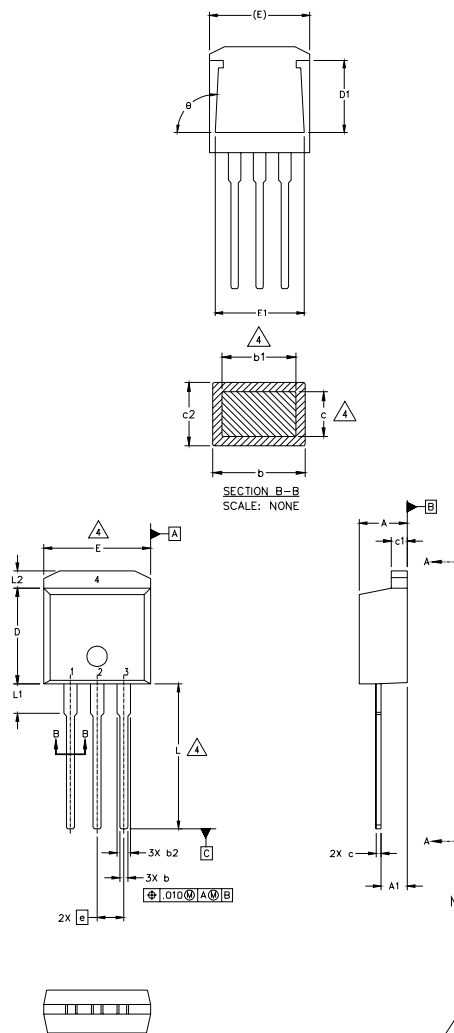
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982. 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
2 CONTROLLING DIMENSION : INCH 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

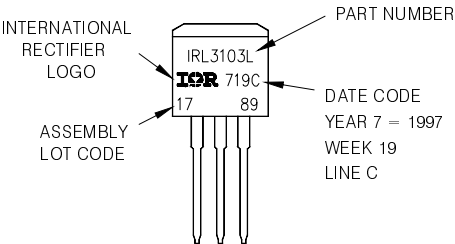
HEXFET	IGBT
1.- GATE	1- GATE
2.- DRAIN	2- COLLECTOR
3.- SOURCE	3- EMITTER
4.- DRAIN	4- COLLECTOR

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

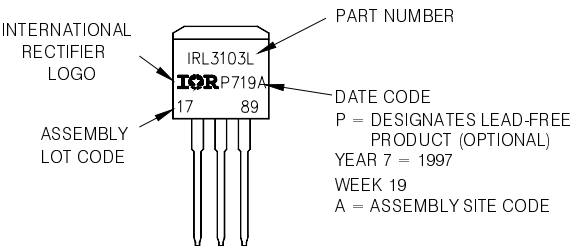
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'



OR



International
IOR Rectifier

GAUGE PLANE

0°-B°

L4

L1

A1

H

SEATING PLANE

DETAIL - "A"

ROTATED 90°

SCALE 8: 1

SECTION B-B

SCALE: NONE

FOOT PRINT

SCALE 2: 1

SECTION A-A

DETAIL A

1. DIMENSION

2. DIMENSION

3. DIMENSION

PER

SYM- BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	4
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	L2
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		m
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		93°
θ	90°	93°	90°	93°	

<u>HEXFET</u>	<u>IGBTs, CoPACK</u>	<u>DIODES</u>
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

D²Pak Part Marking Information

Diagram illustrating the markings on a power MOSFET package:

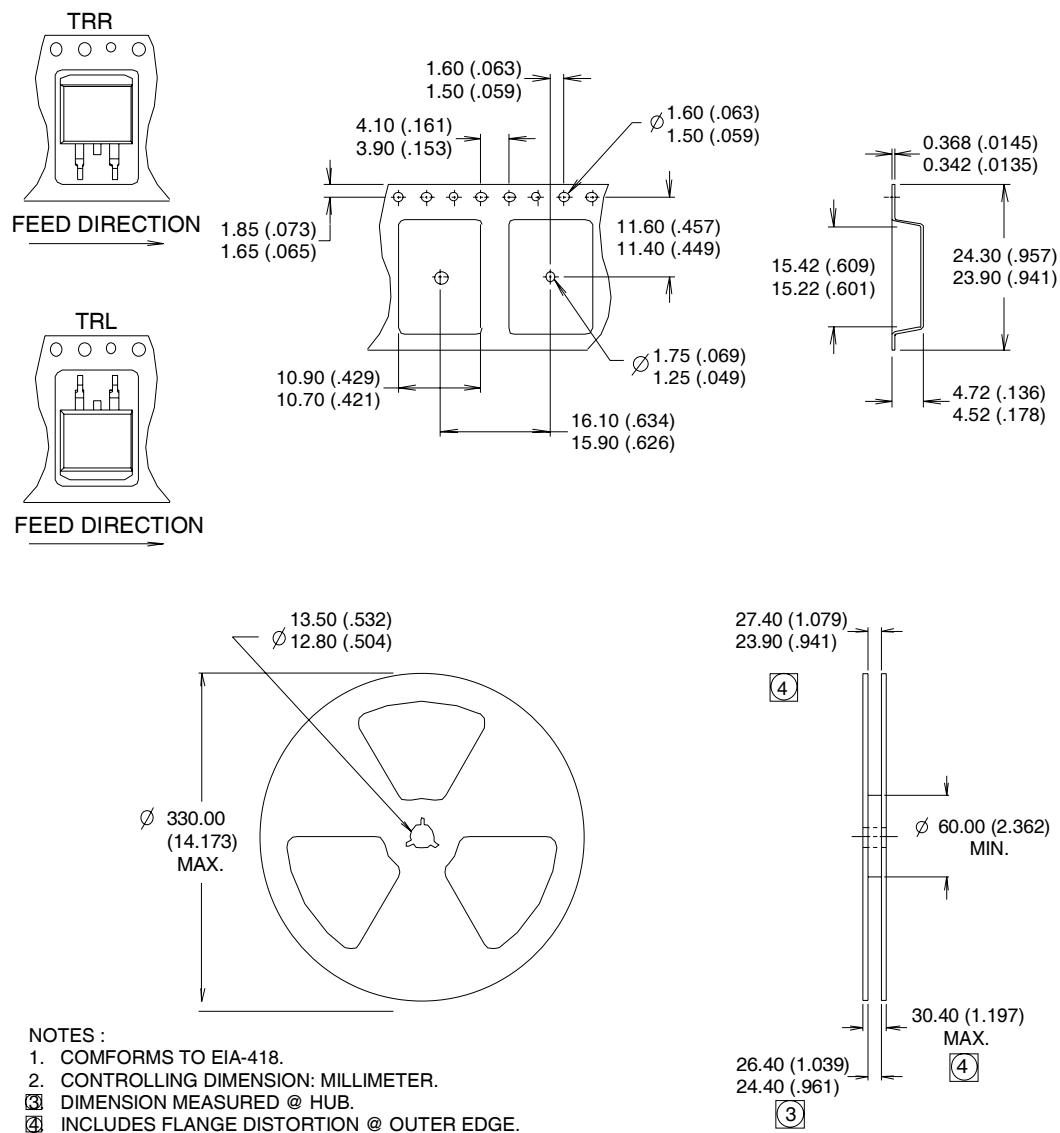
- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo.
- PART NUMBER**: Points to "F530S".
- DATE CODE**: Points to "002L".
- YEAR 0 = 2000**: Points to "002L".
- WEEK 02**: Points to "002L".
- INF 1**: Points to "002L".
- ASSEMBLY LOT CODE**: Points to "80 24".

OR

Diagram illustrating the markings on a power MOSFET package:

- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo.
- PART NUMBER**: Points to "F530S".
- DATE CODE**: Points to "P002A".
- ASSEMBLY LOT CODE**: Points to "80" and "24".
- Additional Markings**:
 - P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
 - YEAR 0 = 2000
 - WEEK 02
 - A = ASSEMBLY SITE CODE

D²Pak Tape & Reel Information



Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.