



## IRF640T

N-channel 200V - 0.15Ω - 15A - TO-220  
MESH OVERLAY™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRF640T	200V	<0.16Ω	15A

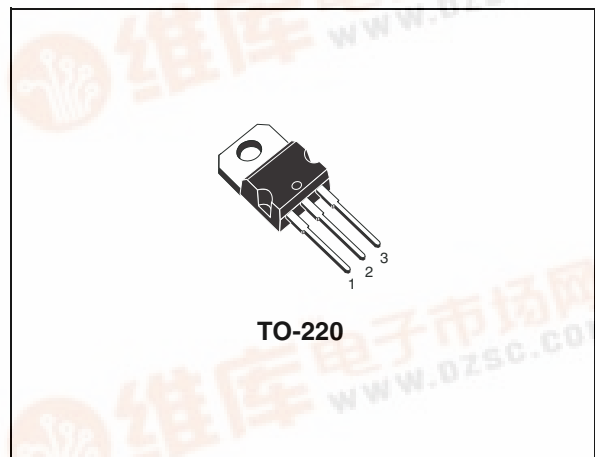
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances

### Description

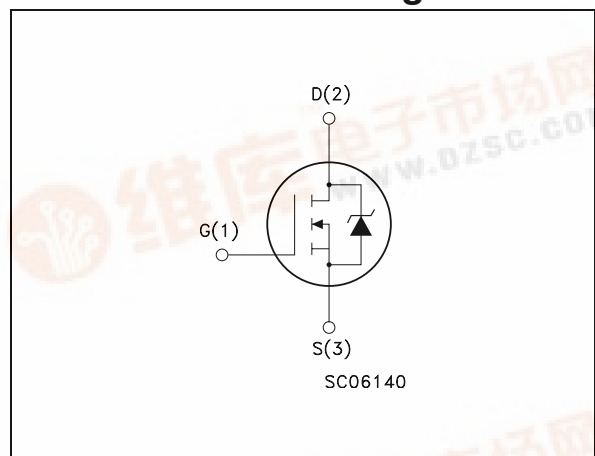
This Power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
IRF640T	IRF640T	TO-220	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	200	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	15	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	10	A
$I_{DM}^{(1)}$	Drain current (pulsed)	60	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	90	W
	Derating factor	0.72	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 15\text{A}$ ,  $di/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\%V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	15	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_d = I_{AR}$ , $V_{DD} = 50\text{V}$ )	110	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0$	200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 7.5\text{A}$		0.15	0.16	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 8\text{V}$ , $I_D = 7.5\text{A}$		12		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		800		pF
$C_{oss}$	Output capacitance			165		pF
$C_{rss}$	Reverse transfer capacitance			26		pF
$Q_g$	Total gate charge	$V_{DD} = 160\text{V}$ , $I_D = 15\text{A}$		24		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{V}$		4.4		nC
$Q_{gd}$	Gate-drain charge	(see Figure 14)		11.6		nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=100\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		11.5 22		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=100\text{ V}$ , $I_D=7.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		19 11		ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$ , $V_{GS}=0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=15\text{ A}$ , $V_{DD}=50\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see Figure 18)		125 0.55 8.8		ns $\mu\text{C}$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=15\text{ A}$ , $V_{DD}=50\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J=150^\circ\text{C}$ (see Figure 18)		148 0.73 9.9		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

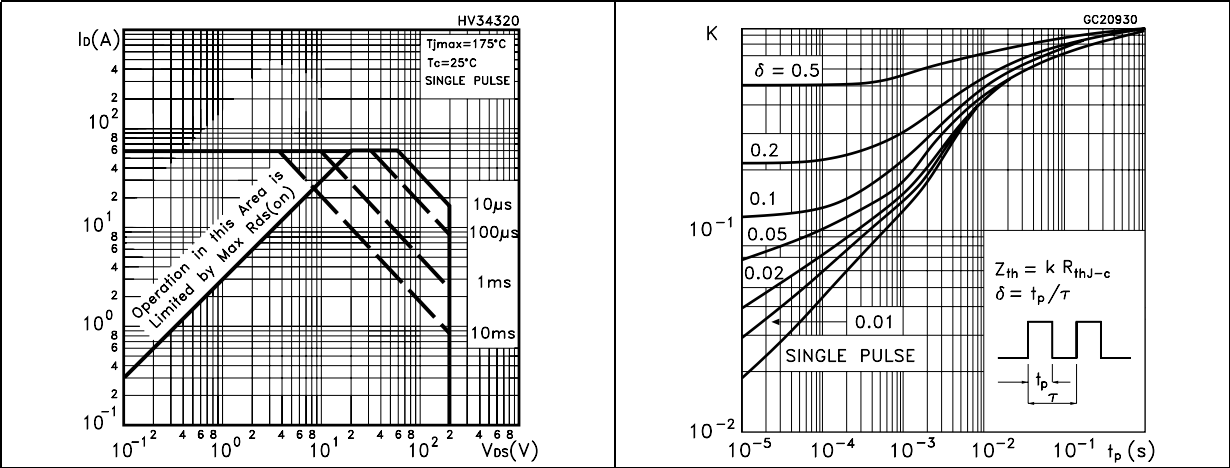


Figure 3. Output characteristics

Figure 4. Transfer characteristics

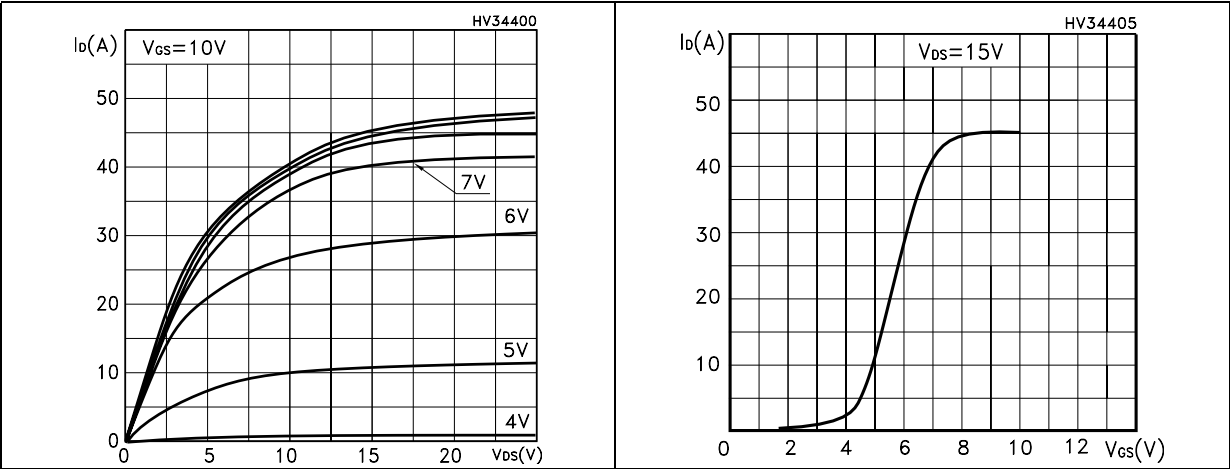


Figure 5. Static drain-source on resistance

Figure 6. Normalized  $BV_{DSS}$  vs temperature

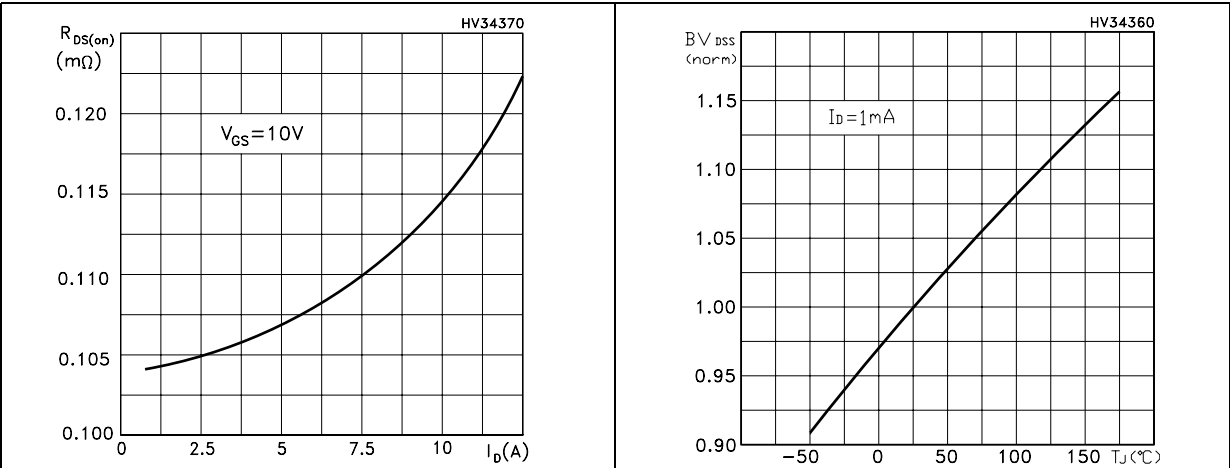


Figure 7. Gate charge vs gate-source voltage      Figure 8. Capacitance variations

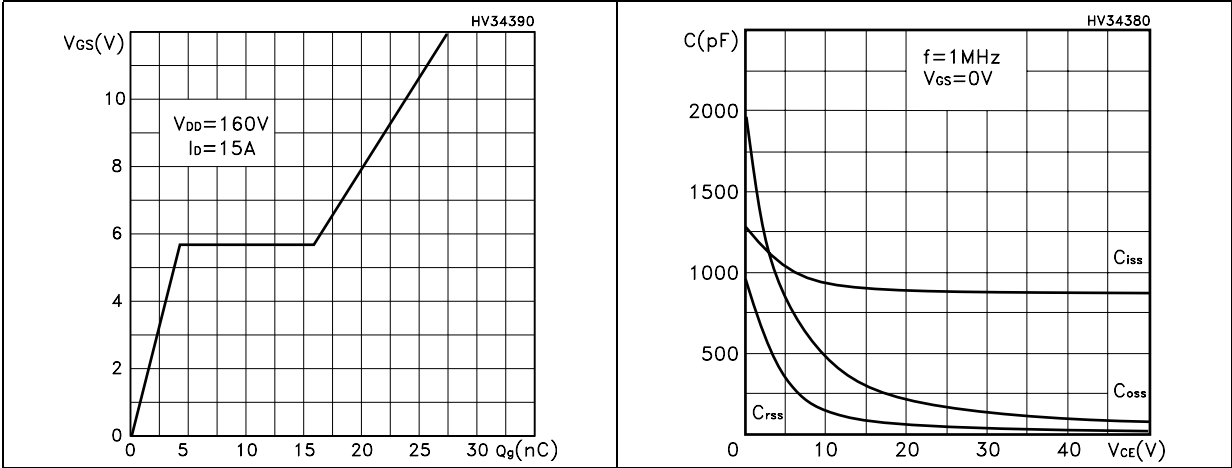


Figure 9. Normalized gate threshold voltage vs temperature      Figure 10. Normalized on resistance vs temperature

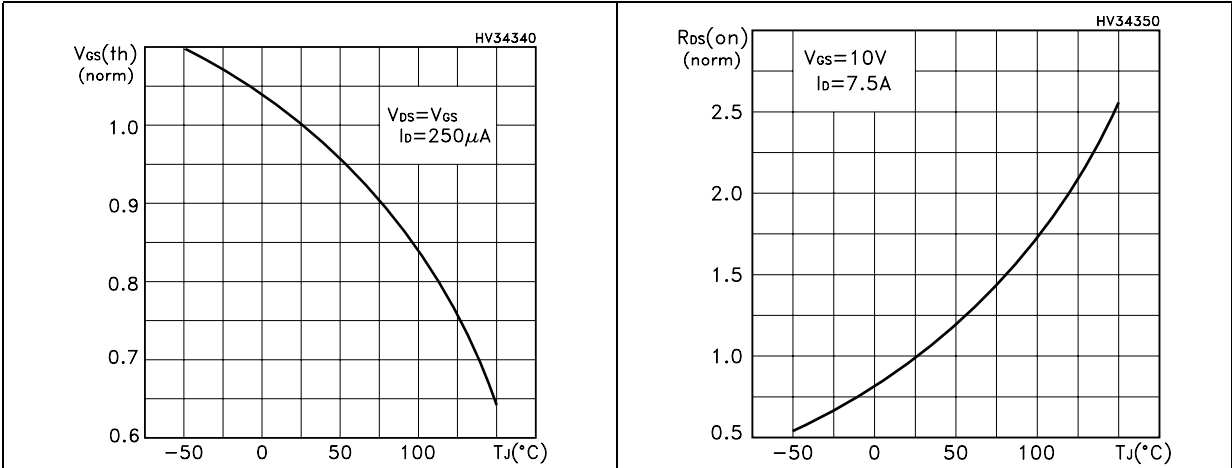
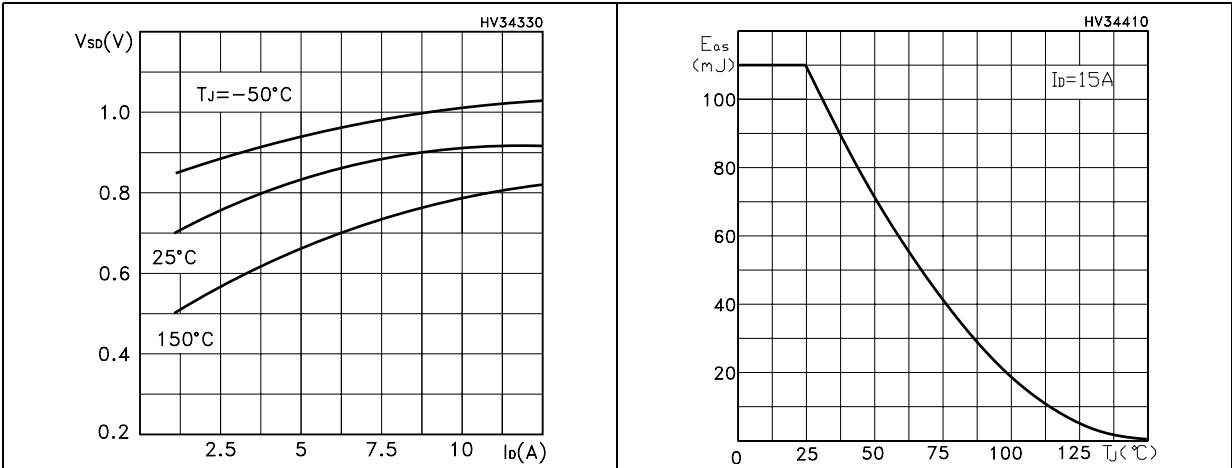
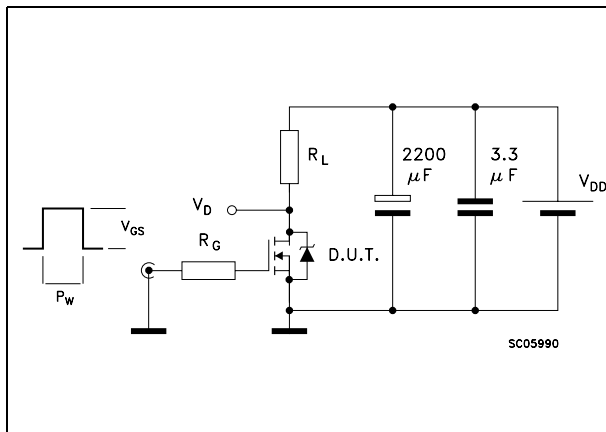


Figure 11. Source-drain forward characteristics      Figure 12. Maximum avalanche energy vs temperature

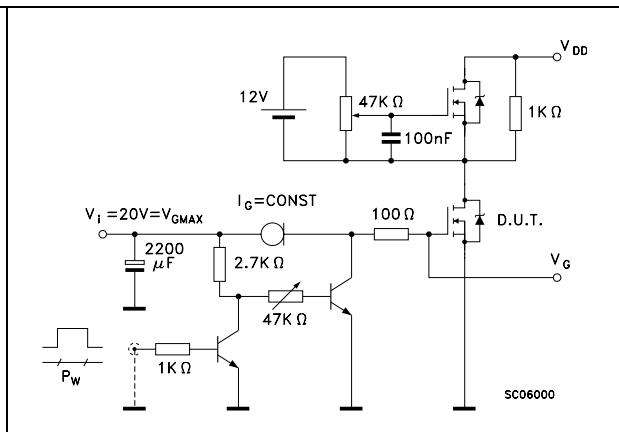


### 3 Test circuit

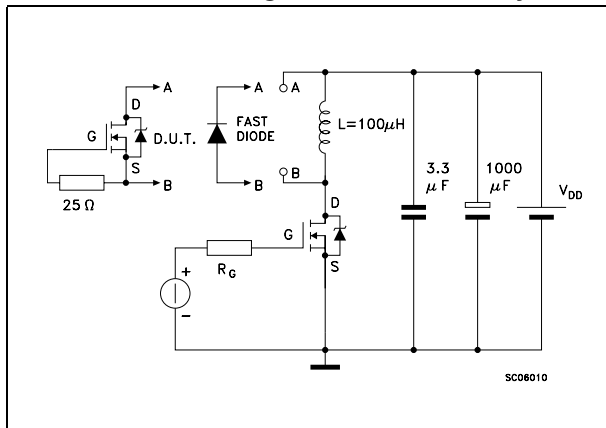
**Figure 13. Switching times test circuit for resistive load**



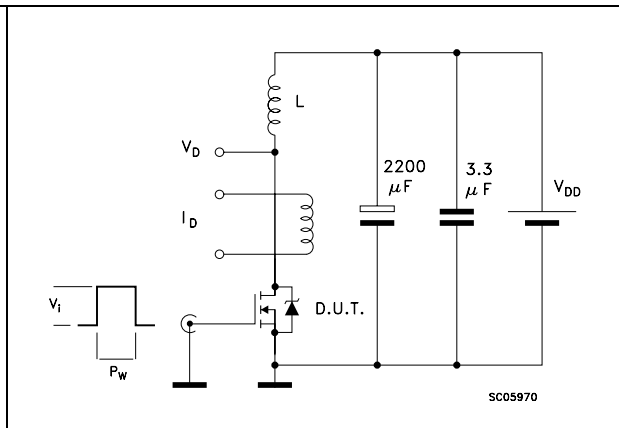
**Figure 14. Gate charge test circuit**



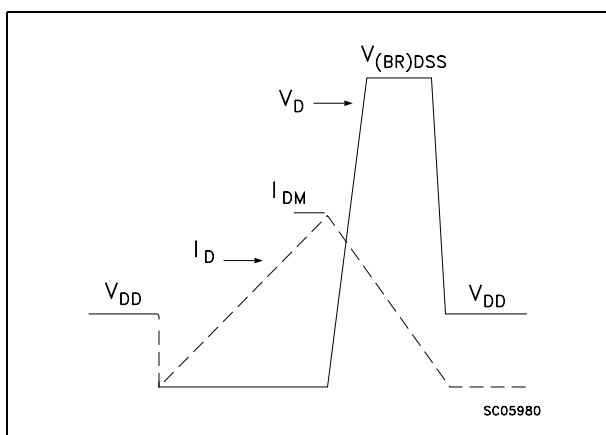
**Figure 15. Test circuit for inductive load switching and diode recovery times**



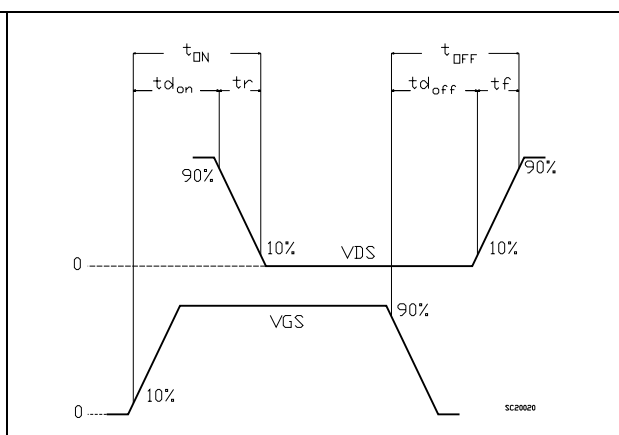
**Figure 16. Unclamped Inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**

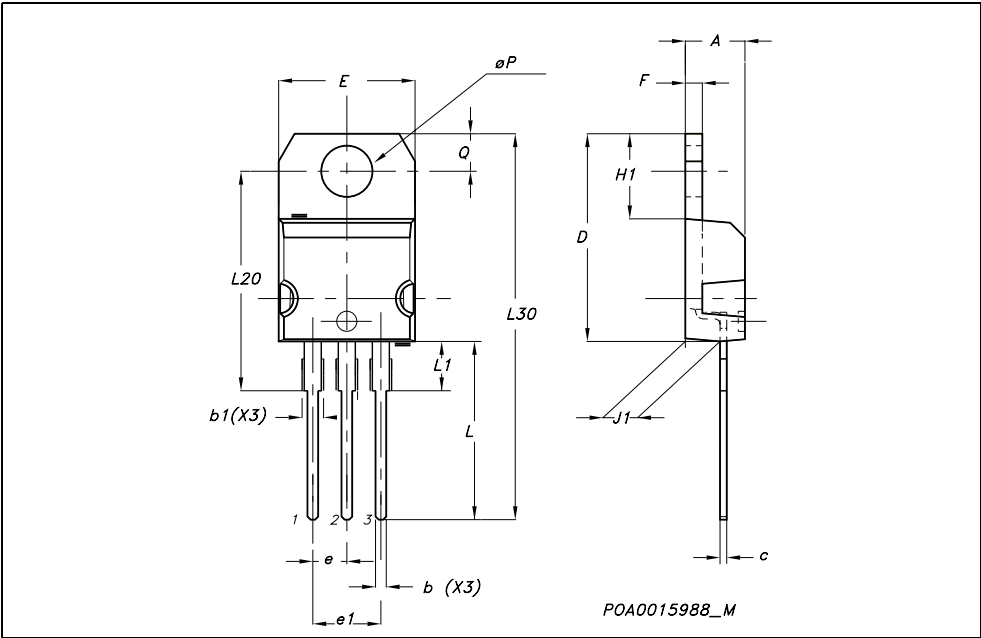




## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 8. Revision history**

Date	Revision	Changes
06-Oct-2006	1	First Release

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