

# International I<sup>R</sup> Rectifier

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

## Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	3.5	-2.3	A
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	2.8	-1.8	
I <sub>DM</sub>	Pulsed Drain Current ①	14	-10	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/nS
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to + 150		°C

## Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
R <sub>θJA</sub>	Maximum Junction-to-Ambient ④	—	—	62.5	°C/W

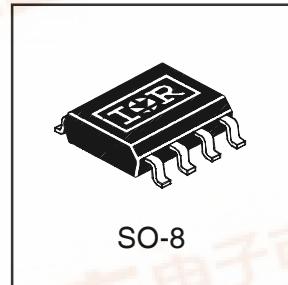
PD - 95164

# IRF7105PbF

HEXFET® Power MOSFET

	N-Ch	P-Ch
V <sub>DSS</sub>	25V	-25V
R <sub>DS(on)</sub>	0.10Ω	0.25Ω
I <sub>D</sub>	3.5A	-2.3A

Top View



SO-8

# IRF7105PbF

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	N-Ch	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
		P-Ch	-25	—	—		$V_{GS} = 0V, I_D = -250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.030	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.015	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(\text{ON})}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.083	0.10	$\Omega$	$V_{GS} = 10V, I_D = 1.0\text{A}$ ③
		N-Ch	—	0.14	0.16		$V_{GS} = 4.5V, I_D = 0.50\text{A}$ ③
		P-Ch	—	0.16	0.25		$V_{GS} = -10V, I_D = -1.0\text{A}$ ③
		P-Ch	—	0.30	0.40		$V_{GS} = -4.5V, I_D = -0.50\text{A}$ ③
$V_{GS(\text{th})}$	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
		P-Ch	-1.0	—	-3.0		$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
$g_f$	Forward Transconductance	N-Ch	—	4.3	—	S	$V_{DS} = 15V, I_D = 3.5\text{A}$ ③
		P-Ch	—	3.1	—		$V_{DS} = -15V, I_D = -3.5\text{A}$ ③
$I_{DSS}$	Drain-to-Source Leakage Current	N-Ch	—	—	2.0	$\mu\text{A}$	$V_{DS} = 20V, V_{GS} = 0V$
		P-Ch	—	—	-2.0		$V_{DS} = -20V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -20V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	N-P	—	—	$\pm 100$		$V_{GS} = \pm 20V$
$Q_g$	Total GateCharge	N-Ch	—	9.4	27	nC	N-Channel $I_D = 2.3\text{A}, V_{DS} = 12.5V, V_{GS} = 10V$ ③
		P-Ch	—	10	25		P-Channel $I_D = -2.3\text{A}, V_{DS} = -12.5V, V_{GS} = -10V$
$Q_{gs}$	Gate-to-Source Charge	N-Ch	—	1.7	—		
		P-Ch	—	1.9	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	N-Ch	—	3.1	—	ns	
		P-Ch	—	2.8	—		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	7.0	20		N-Channel $V_{DD} = 25V, I_D = 1.0\text{A}, R_G = 6.0\Omega, R_D = 25\Omega$ ③
		P-Ch	—	12	40		P-Channel $V_{DD} = -25V, I_D = -1.0\text{A}, R_G = 6.0\Omega, R_D = 25\Omega$
$t_r$	Rise Time	N-Ch	—	9.0	20		
		P-Ch	—	13	40		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	45	90	nH	
		P-Ch	—	45	90		
$t_f$	Fall Time	N-Ch	—	25	50		
		P-Ch	—	37	50		
$L_D$	Internal Drain Inductance	N-P	—	4.0	—		Between lead , 6mm (0.25in.)from package and center of die contact
$L_S$	Internal Source Inductance	N-P	—	6.0	—		
$C_{iss}$	Input Capacitance	N-Ch	—	330	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$
		P-Ch	—	290	—		P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	N-Ch	—	250	—		
		P-Ch	—	210	—		
$C_{rss}$	Reverse Transfer Capacitance	N-Ch	—	61	—		
		P-Ch	—	67	—		

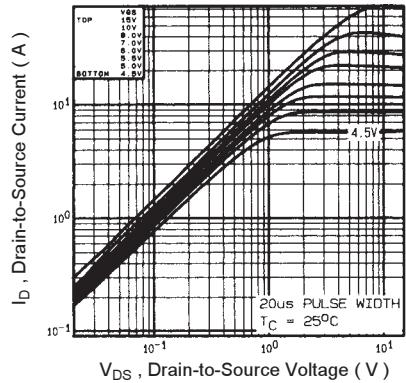
## Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
$I_{SM}$	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	14		
		P-Ch	—	—	-9.2		
$V_{SD}$	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.3\text{A}, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -1.3\text{A}, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	N-Ch	—	36	54	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 1.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$
		P-Ch	—	69	100		P-Channel $T_J = 25^\circ\text{C}, I_F = -1.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$ ③
$Q_{rr}$	Reverse Recovery Charge	N-Ch	—	41	75	nC	
		P-Ch	—	90	180		
$t_{on}$	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② N-Channel  $I_{SD} \leq 3.5\text{A}$ ,  $di/dt \leq 90\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 150^\circ\text{C}$   
P-Channel  $I_{SD} \leq -2.3\text{A}$ ,  $di/dt \leq 90\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 150^\circ\text{C}$
- ③ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Surface mounted on FR-4 board,  $t \leq 10\text{sec}$ .

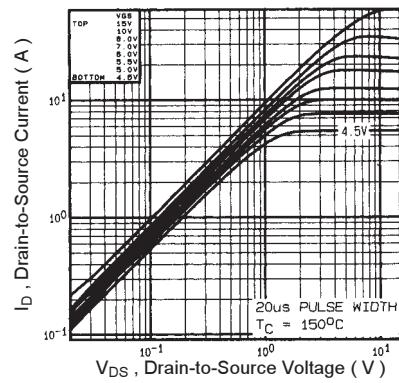
International  
**IR** Rectifier



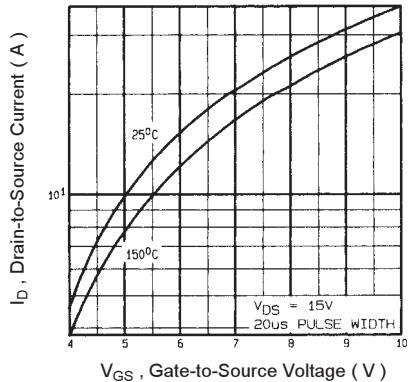
**Fig 1.** Typical Output Characteristics

N-Channel

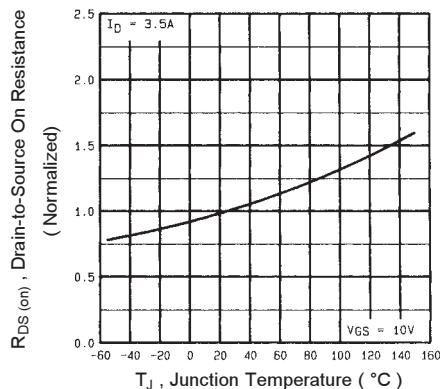
**IRF7105PbF**



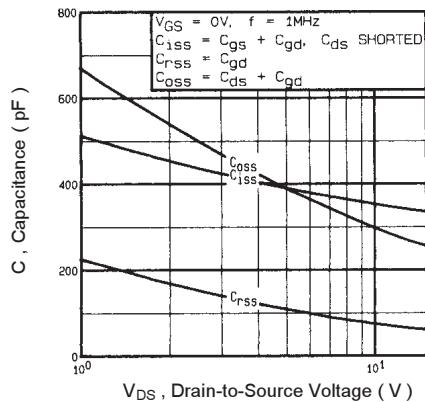
**Fig 2.** Typical Output Characteristics



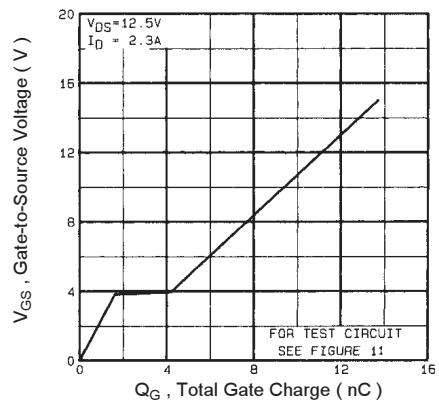
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance Vs. Temperature



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

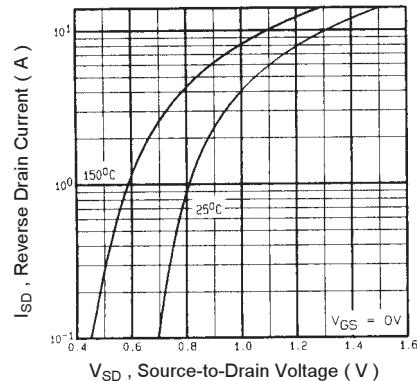


**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

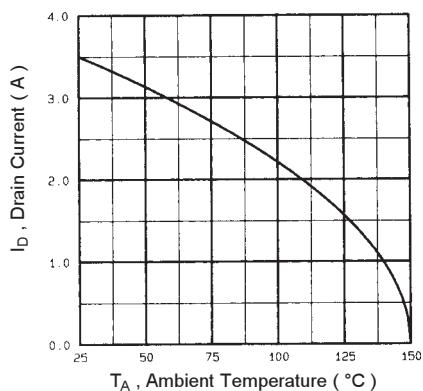
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N-Channel

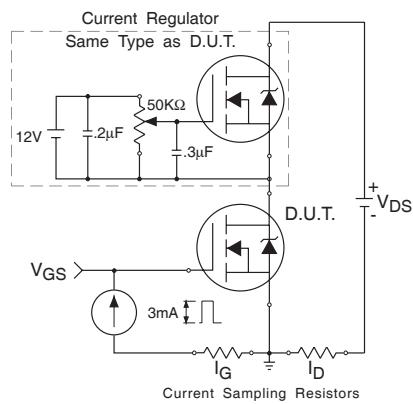
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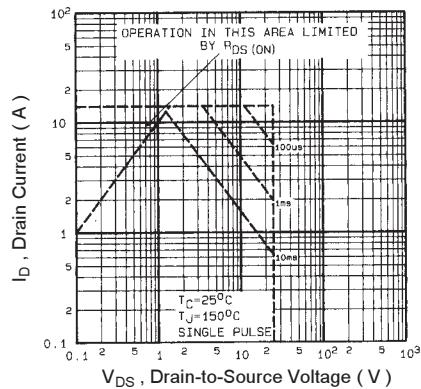
**Fig 7.** Typical Source-Drain Diode Forward Voltage



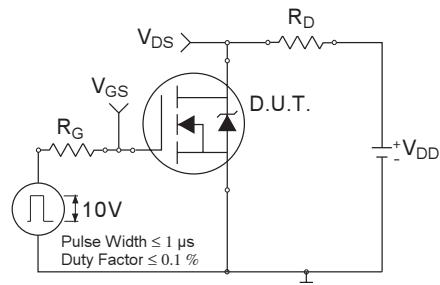
**Fig 9.** Maximum Drain Current Vs. Ambient Temperature



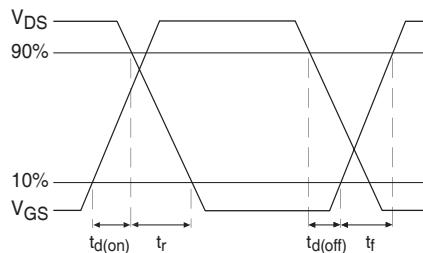
**Fig 11a.** Gate Charge Test Circuit



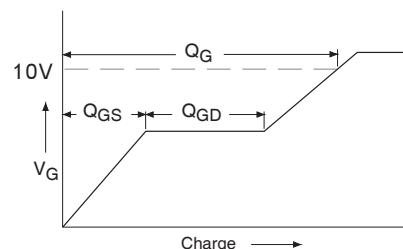
**Fig 8.** Maximum Safe Operating Area



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



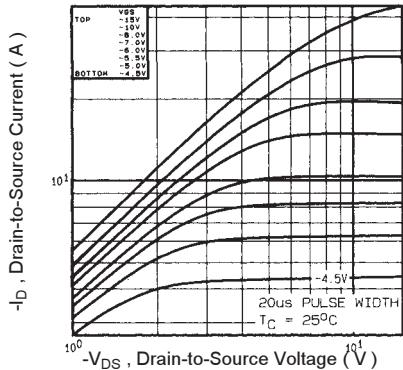
**Fig 11b.** Basic Gate Charge Waveform

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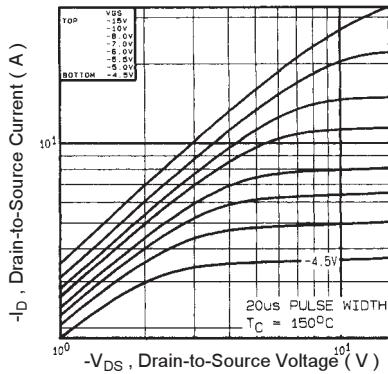
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P-Channel

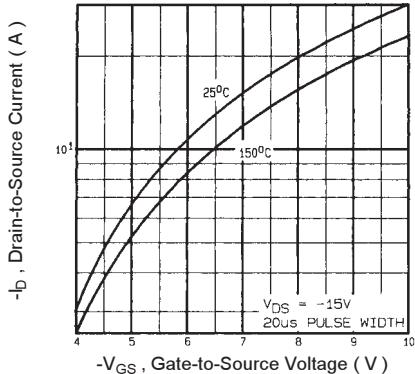
**IRF7105PbF**



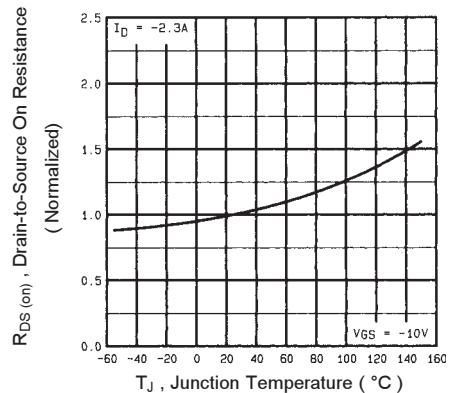
**Fig 12.** Typical Output Characteristics



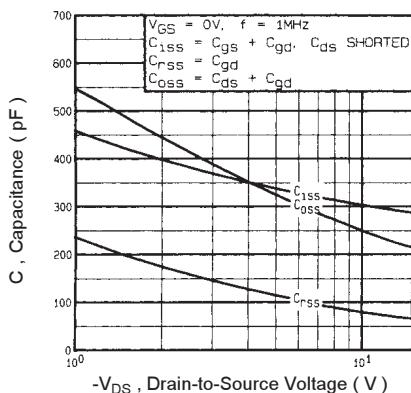
**Fig 13.** Typical Output Characteristics



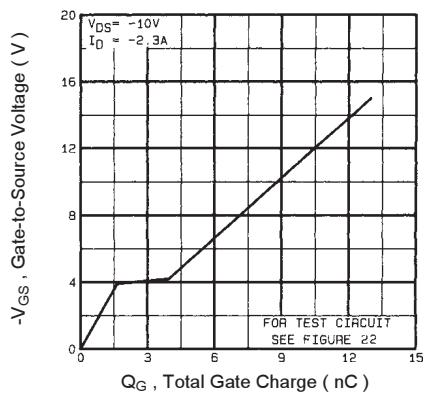
**Fig 14.** Typical Transfer Characteristics



**Fig 15.** Normalized On-Resistance Vs. Temperature



**Fig 16.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 17.** Typical Gate Charge Vs. Gate-to-Source Voltage

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P-Channel

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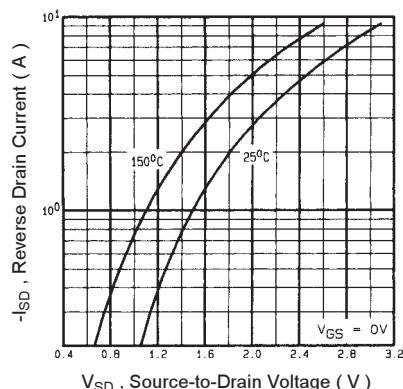


Fig 18. Typical Source-Drain Diode Forward Voltage

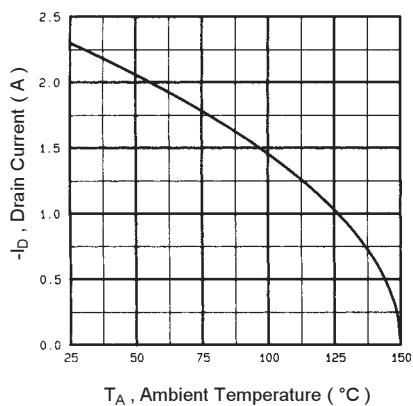


Fig 20. Maximum Drain Current Vs. Ambient Temperature

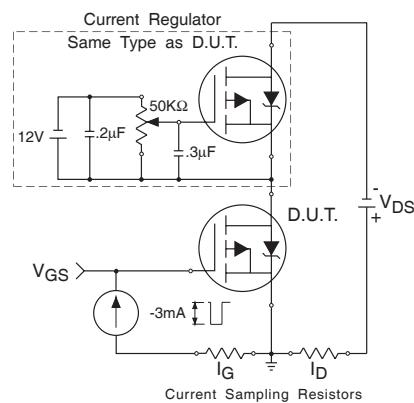


Fig 22a. Gate Charge Test Circuit

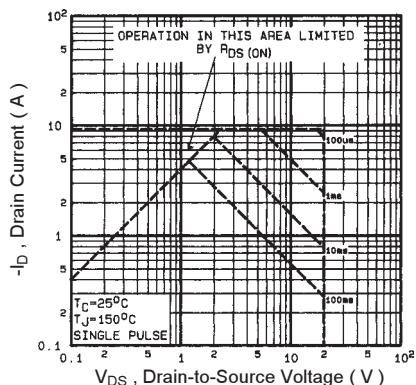


Fig 19. Maximum Safe Operating Area

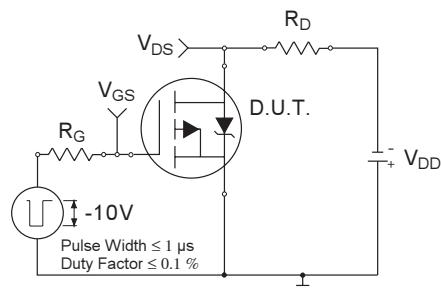


Fig 21a. Switching Time Test Circuit

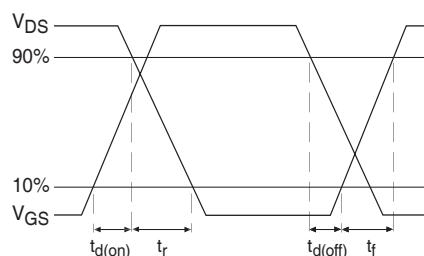


Fig 21b. Switching Time Waveforms

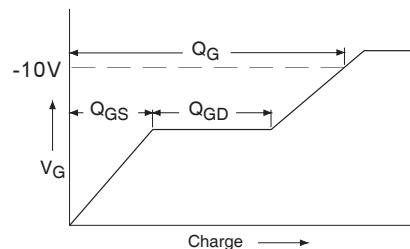
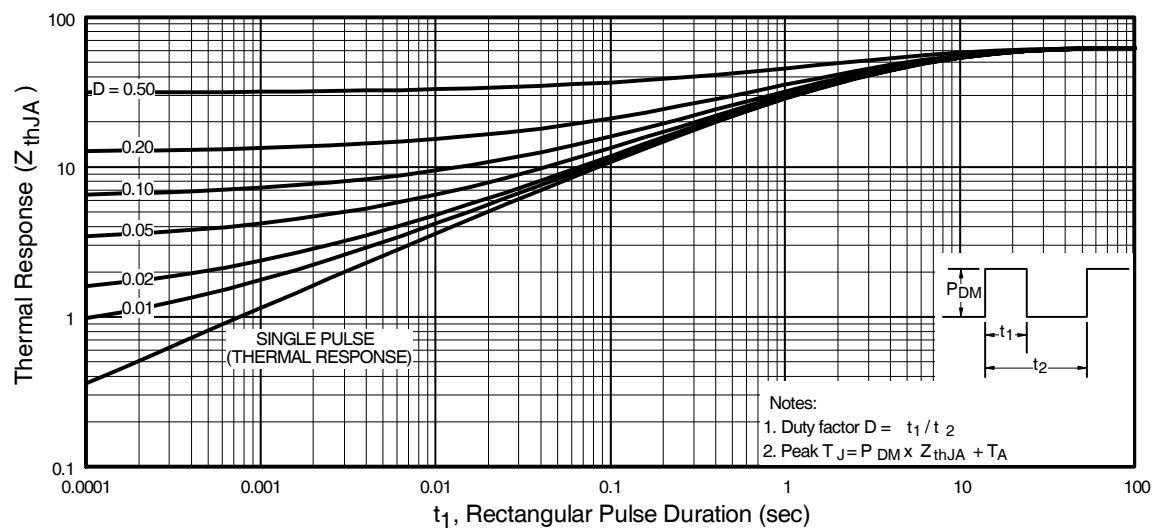


Fig 22b. Basic Gate Charge Waveform

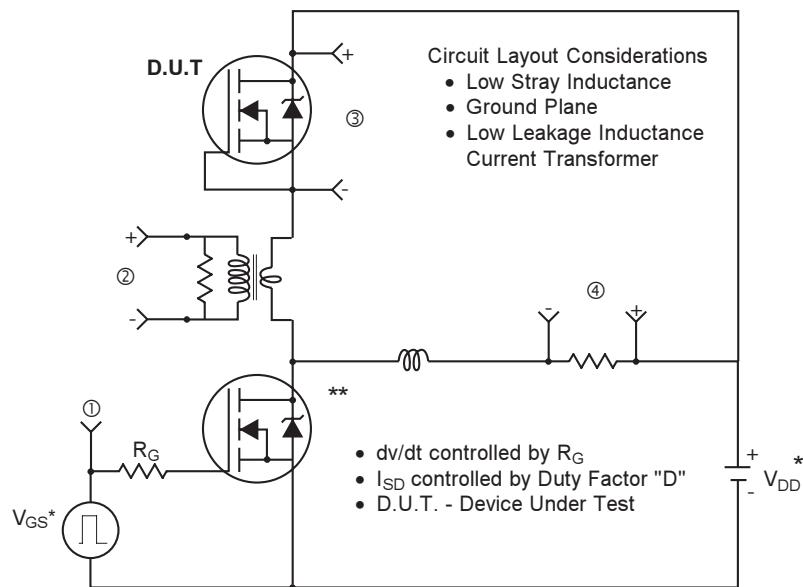


**Fig 23.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

# IRF7105PbF

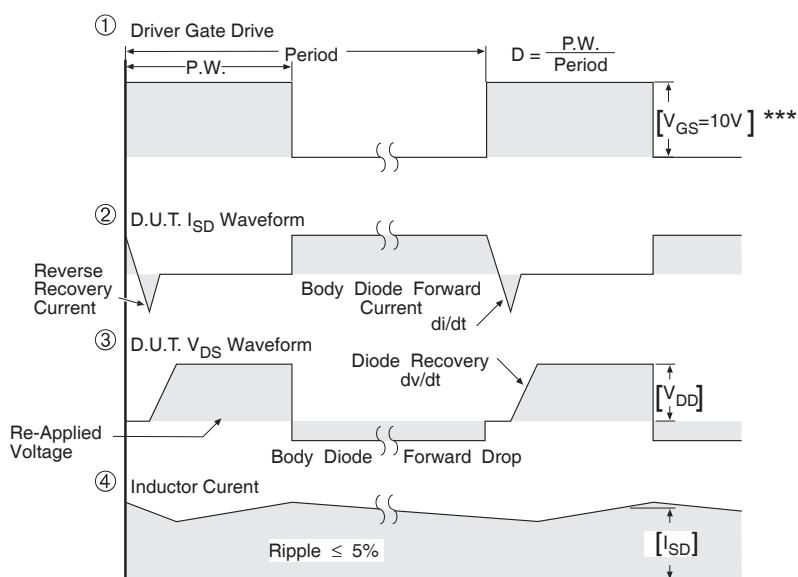
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## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements

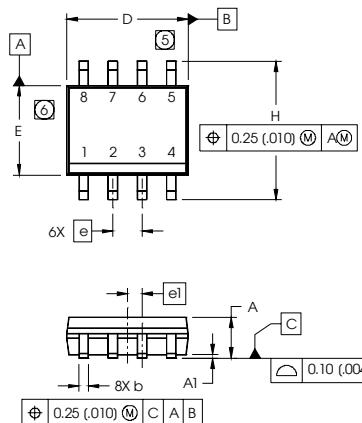


\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

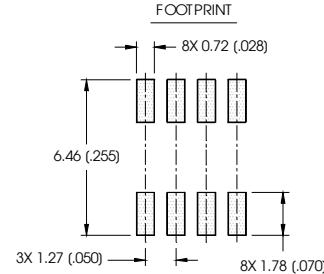
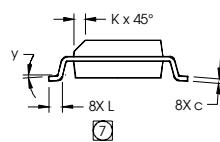
Fig 24. For N and P Channel HEXFETS

## SO-8 Package Outline

Dimensions are shown in millimeters (inches)

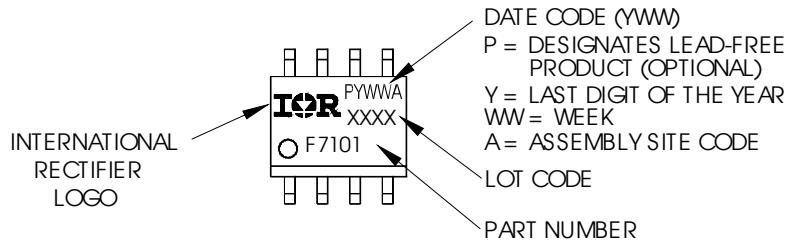


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.059	BASIC	1.27	BASIC
e1	.025	BASIC	0.635	BASIC
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
Y	0°	8°	0°	8°



## SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

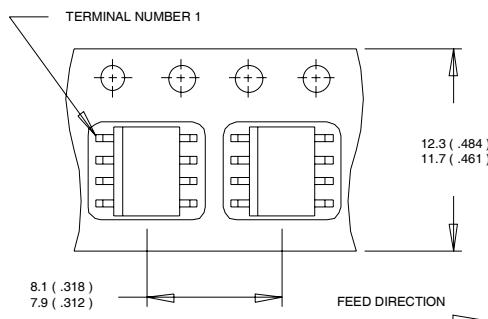


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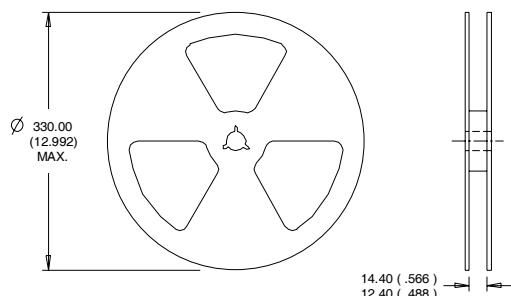
## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Consumer market.  
Qualification Standards can be found on IR's Web site.

International  
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