



# IRF740AS, IRF740AL, SiHF740AS, SiHF740AL

Vishay Siliconix

## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	400
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.55
$Q_g$ (Max.) (nC)	36
$Q_{gs}$ (nC)	9.9
$Q_{gd}$ (nC)	16
Configuration	Single

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  specified (AN 1001)
- Lead (Pb)-free Available



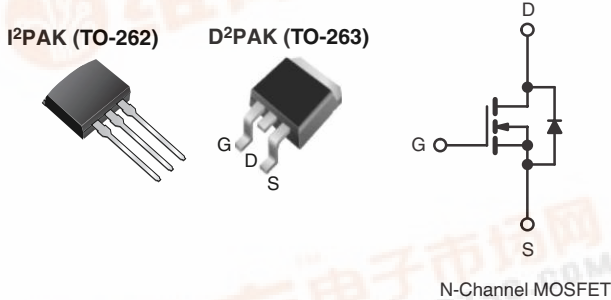
Available  
**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both for US Line Input Only)



ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free	IRF740ASPbF	IRF740ASTRLPbF <sup>a</sup>	IRF740ASTRRPbF <sup>a</sup>	IRF740ALPbF
	SiHF740AS-E3	SiHF740ASTL-E3 <sup>a</sup>	SiHF740ASTR-E3 <sup>a</sup>	SiHF740AL-E3
SnPb	IRF740AS	IRF740ASTRL <sup>a</sup>	IRF740ASTRR <sup>a</sup>	IRF740AL
	SiHF740AS	SiHF740ASTL <sup>a</sup>	SiHF740ASTR <sup>a</sup>	SiHF740AL

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		400	V
Gate-Source Voltage	$V_{GS}$		$\pm 30$	
Continuous Drain Current <sup>e</sup>	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	10	A
		$T_C = 100\text{ }^\circ\text{C}$	6.3	
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$		40	
Linear Derating Factor			1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b, e</sup>	$E_{AS}$		630	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$		10	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		12.5	mJ
Maximum Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$		3.1	W
	$T_C = 25\text{ }^\circ\text{C}$		125	
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>	$dV/dt$		5.9	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 12.6\text{ mH}$ ,  $R_G = 25\text{ }^\circ\Omega$ ,  $I_{AS} = 10\text{ A}$  (see fig. 12).
- $I_{SD} \leq 10\text{ A}$ ,  $dI/dt \leq 330\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- Uses IRF740A/SiHF740A data and test conditions.

\* Pb-containing terminations are not RoHS compliant, exemptions may apply

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


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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

## Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	400	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.48	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}^b$	-	-	0.55	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.0\text{ A}^d$	4.9	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>d</sup>	-	1030	-	pF	
Output Capacitance	$C_{oss}$		-	170	-		
Reverse Transfer Capacitance	$C_{rss}$		-	7.7	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1490	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 320\text{ V}, f = 1.0\text{ MHz}$	-	52	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 320\text{ V}$ , see fig. 6 and 13 <sup>b, d</sup>	-	-	36	nC
Gate-Source Charge	$Q_{gs}$			-	-	9.9	
Gate-Drain Charge	$Q_{gd}$			-	-	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 10\text{ A}, R_G = 10\text{ }\Omega, R_D = 19.5\text{ }\Omega$ , see fig. 10 <sup>b, d</sup>	-	10	-	ns	
Rise Time	$t_r$		-	35	-		
Turn-Off Delay Time	$t_{d(off)}$		-	24	-		
Fall Time	$t_f$		-	22	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	10	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	40		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.0	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b, d$	-	240	360	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.9	2.9	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

## Notes

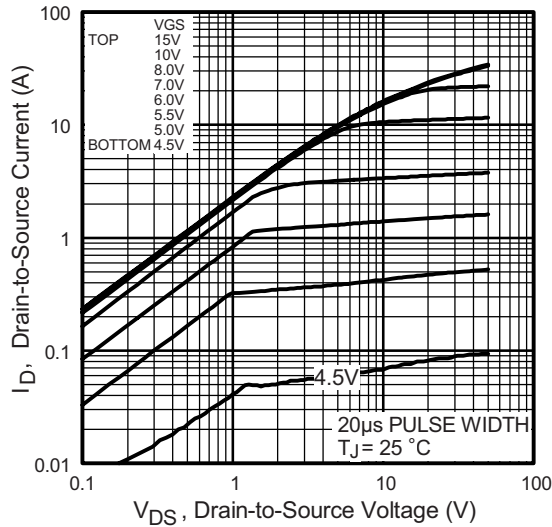
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DS}$ .
- Uses IRF740A/SiHF740A data and test conditions.



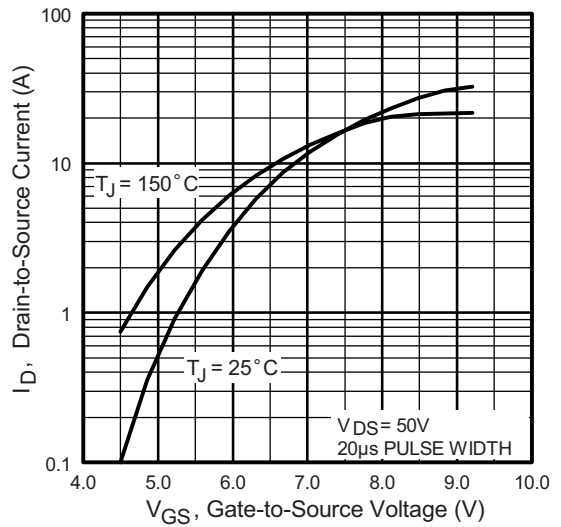
# IRF740AS, IRF740AL, SiHF740AS, SiHF740AL

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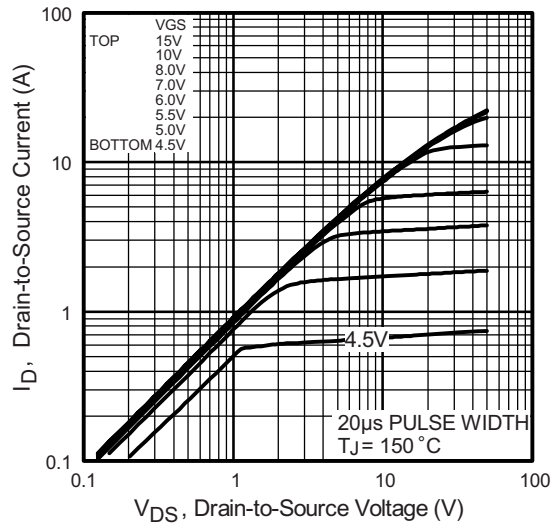
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



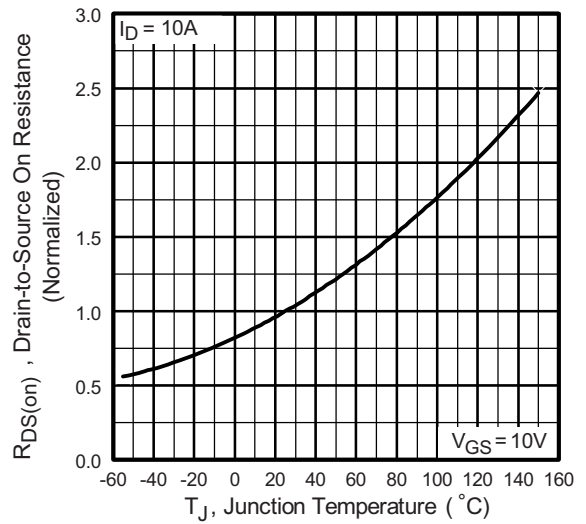
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

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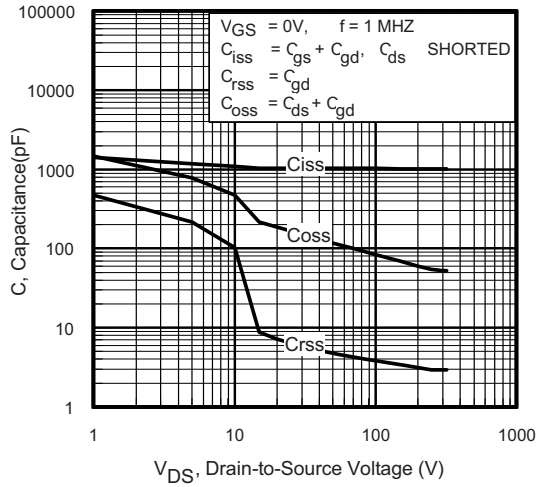


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

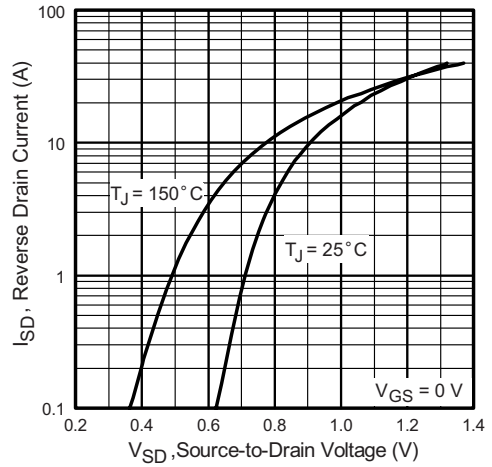


Fig. 7 - Typical Source-Drain Diode Forward Voltage

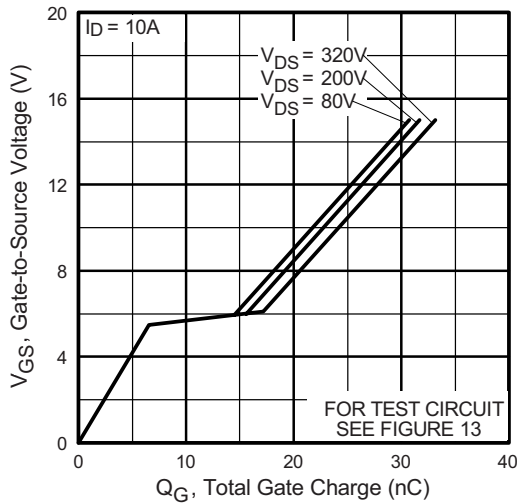


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

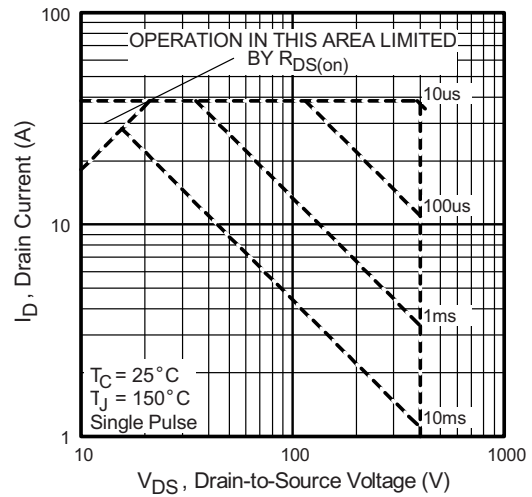


Fig. 8 - Maximum Safe Operating Area



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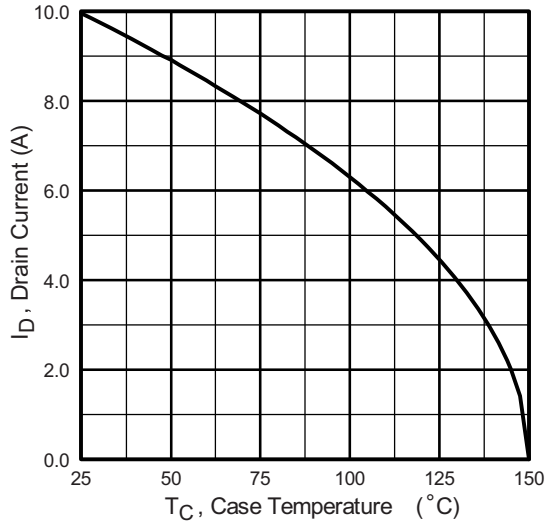


Fig. 9 - Maximum Drain Current vs. Case Temperature

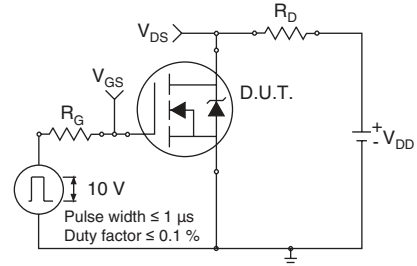


Fig. 10a - Switching Time Test Circuit

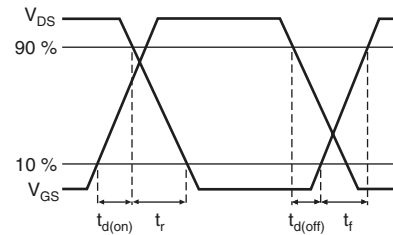


Fig. 10b - Switching Time Waveforms

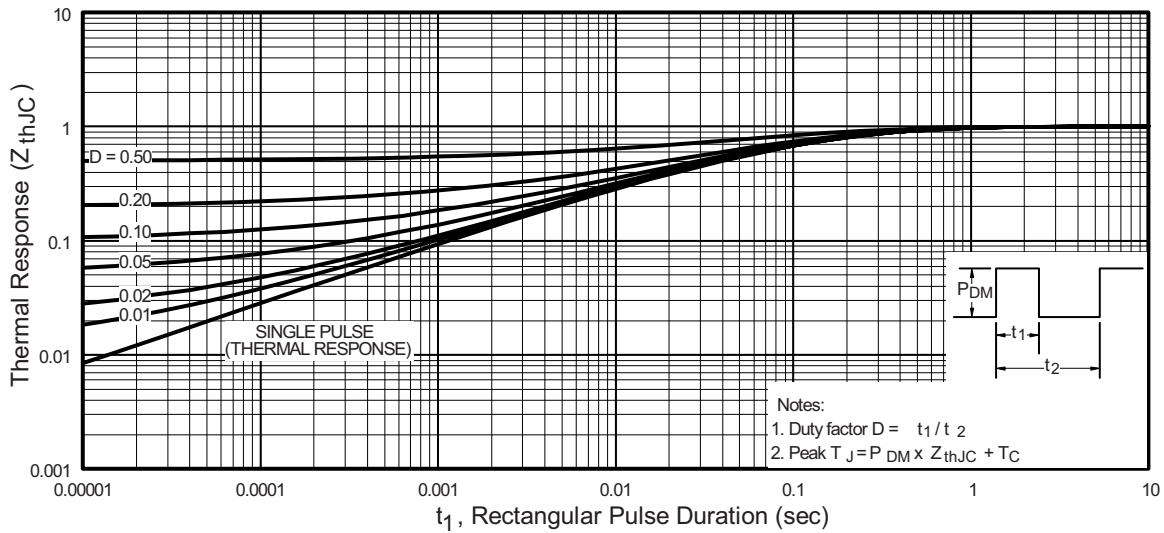


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

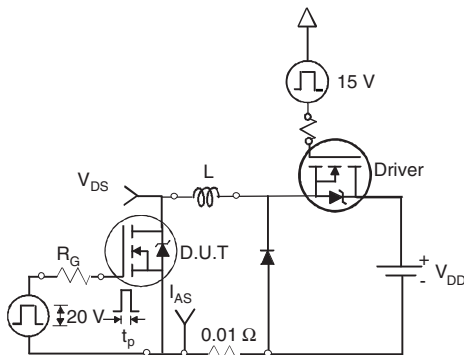


Fig. 12a - Unclamped Inductive Test Circuit

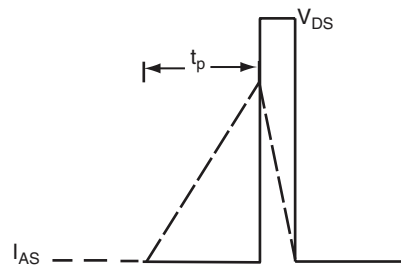


Fig. 12b - Unclamped Inductive Waveforms

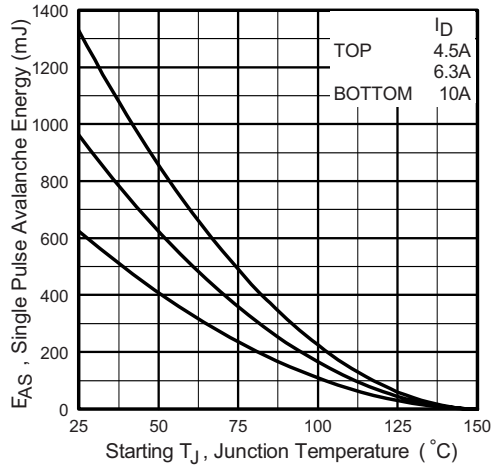


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

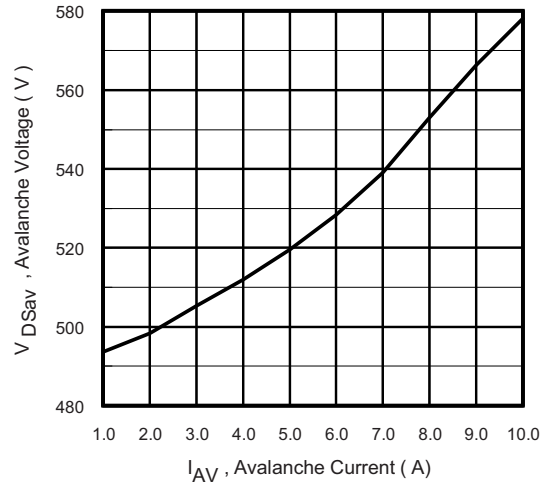


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

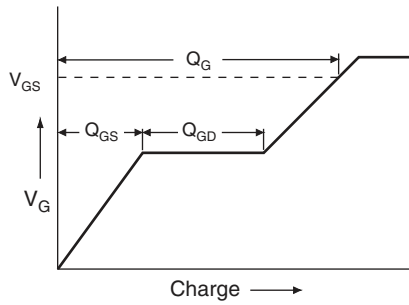


Fig. 13a - Basic Gate Charge Waveform

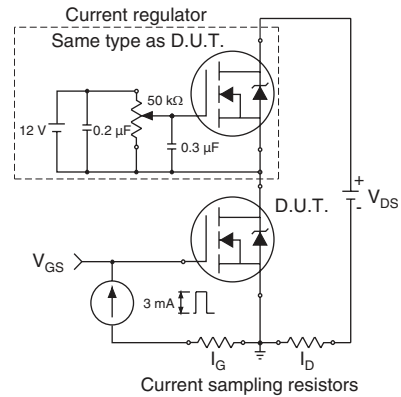
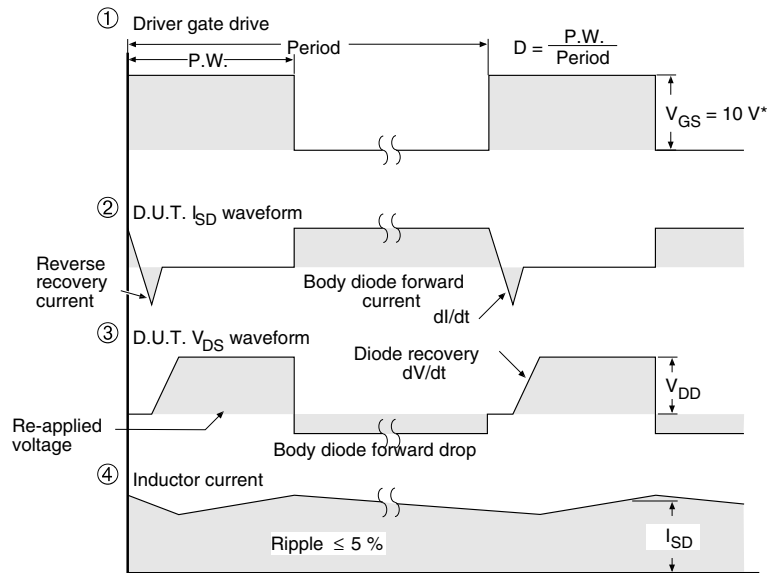
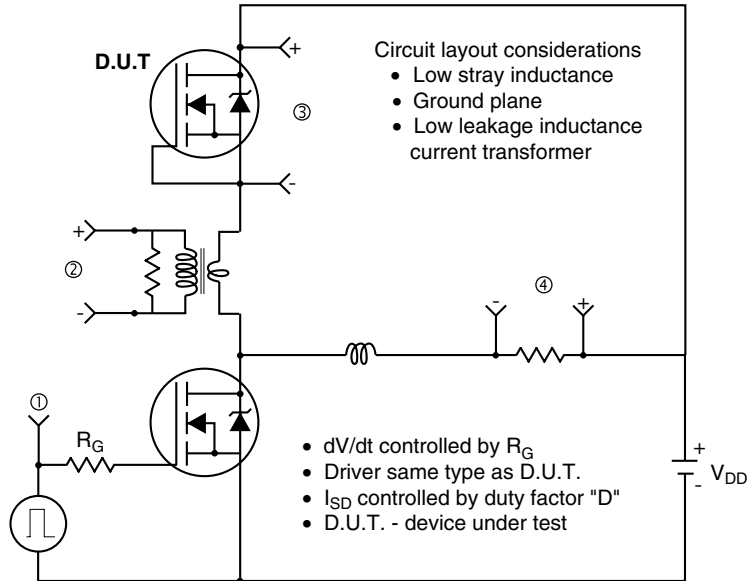


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

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