

International
IR Rectifier

SMPS MOSFET

PD - 95433

IRF8010SPbF
IRF8010LPbF

HEXFET® Power MOSFET

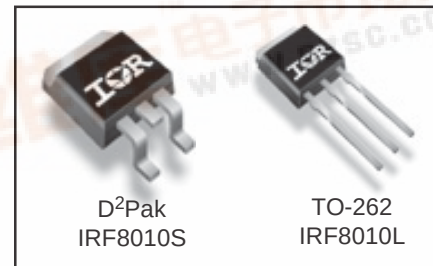
Applications

- High frequency DC-DC converters
- UPS and Motor Control
- Lead-Free

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Typical $R_{DS(on)} = 12m\Omega$

V_{DSS}	$R_{DS(on)}$ max	I_D
100V	15m Ω	80A ^②



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	80 ^②	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	57	
I_{DM}	Pulsed Drain Current ^①	320	
P_D @ $T_C = 25^\circ C$	Power Dissipation	260	W
	Linear Derating Factor	1.8	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ^③	16	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.57	$^\circ C/W$
$R_{\theta JC}$	Junction-to-Case (end of life) ^④	—	0.80	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ^⑤	—	40	

Notes ^① through ^⑤ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15	mΩ	$V_{GS} = 10V, I_D = 45A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

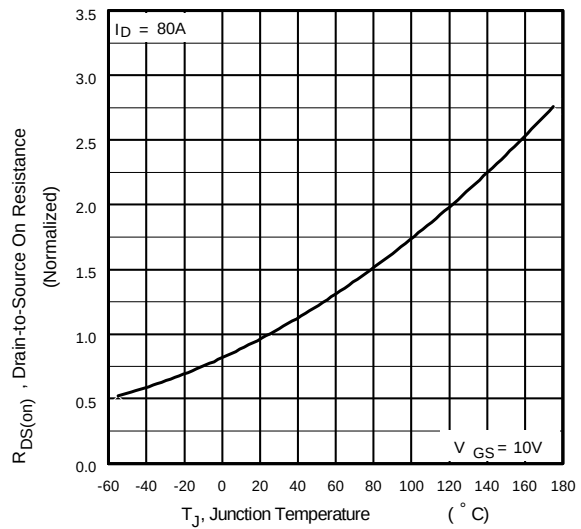
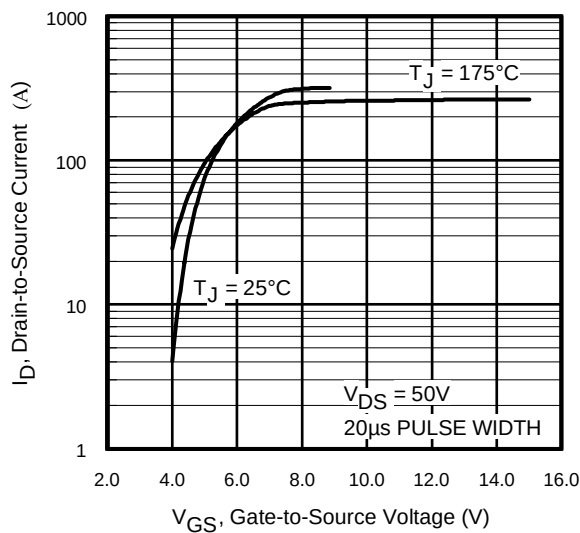
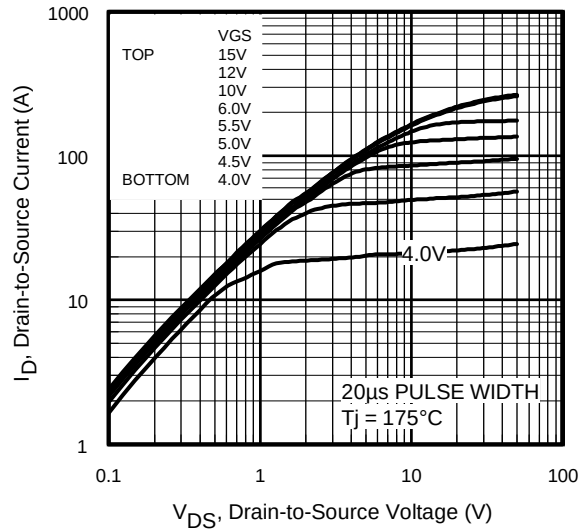
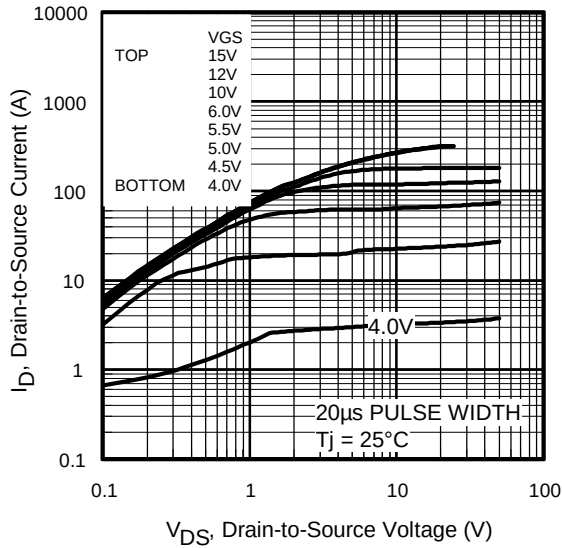
	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	82	—	—	V	$V_{DS} = 25V, I_D = 45A$
Q_g	Total Gate Charge	—	81	120	nC	$I_D = 80A$
Q_{gs}	Gate-to-Source Charge	—	22	—		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	130	—		$I_D = 80A$
$t_{d(off)}$	Turn-Off Delay Time	—	61	—		$R_G = 39\Omega$
t_f	Fall Time	—	120	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	3830	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	480	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	59	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	3830	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	280	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	530	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ③

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②⑦	—	310	mJ
I_{AR}	Avalanche Current ①	—	45	A
E_{AR}	Repetitive Avalanche Energy ①	—	26	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑦	—	—	320		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 80A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	99	150	ns	$T_J = 150^\circ\text{C}, I_F = 80A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	460	700	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



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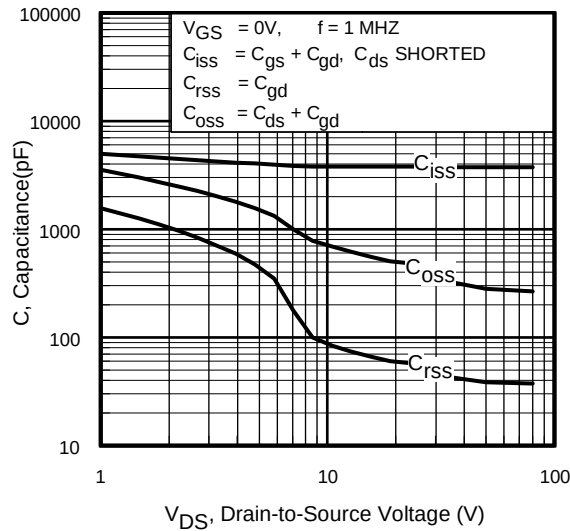


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

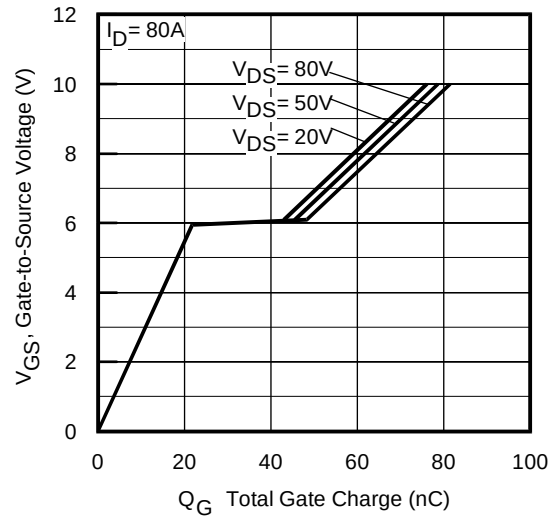


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

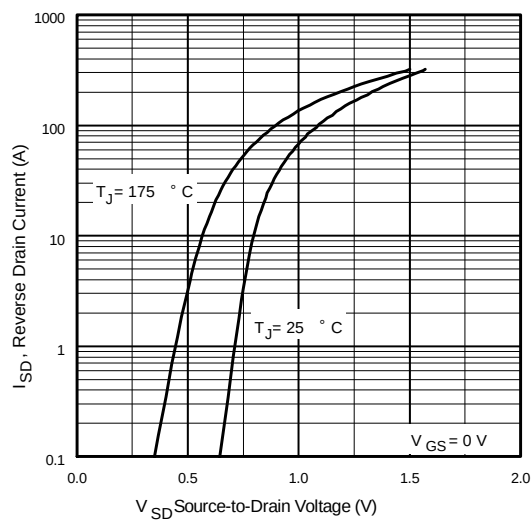


Fig 7. Typical Source-Drain Diode Forward Voltage

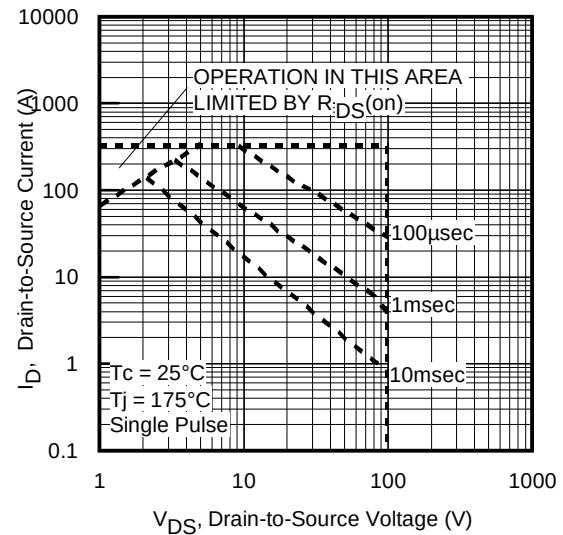


Fig 8. Maximum Safe Operating Area

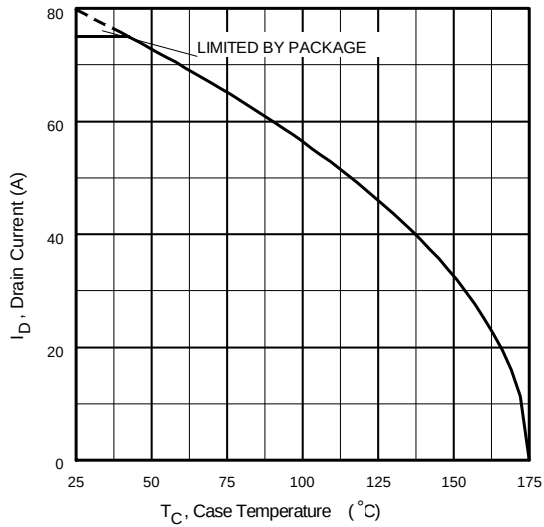


Fig 9. Maximum Drain Current Vs. Case Temperature

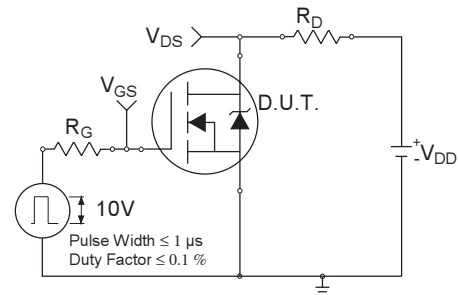


Fig 10a. Switching Time Test Circuit

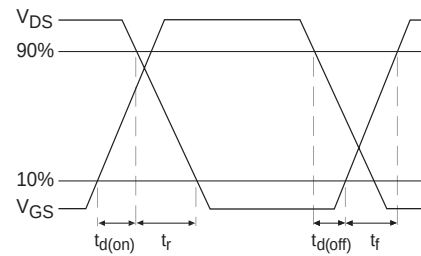


Fig 10b. Switching Time Waveforms

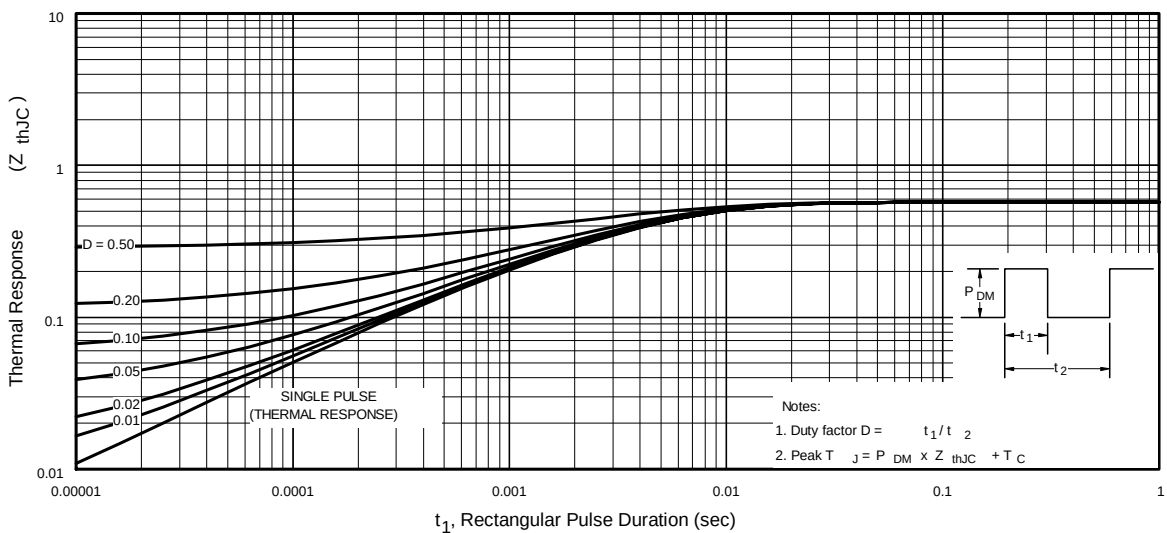


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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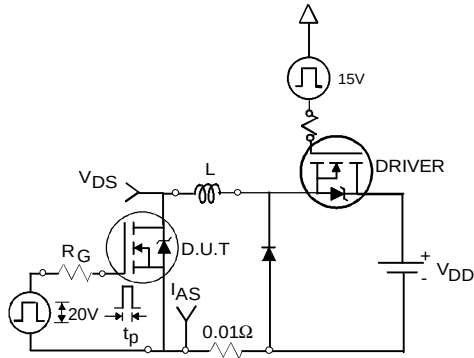


Fig 12a. Unclamped Inductive Test Circuit

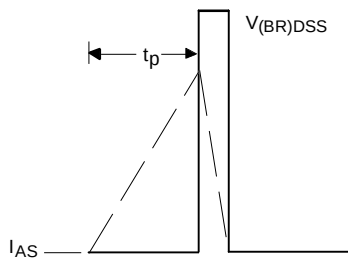


Fig 12b. Unclamped Inductive Waveforms

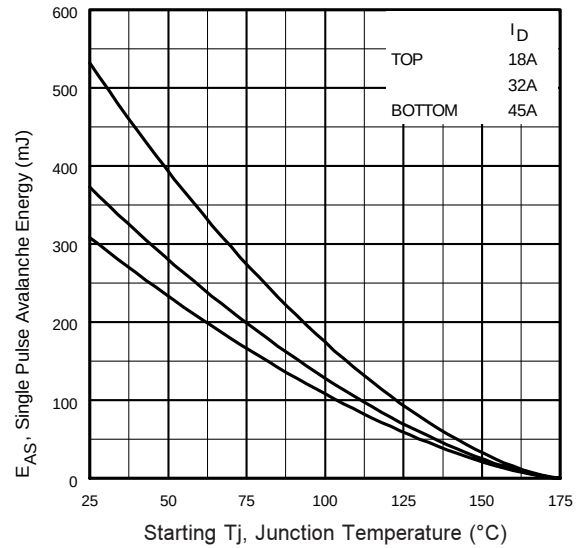


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

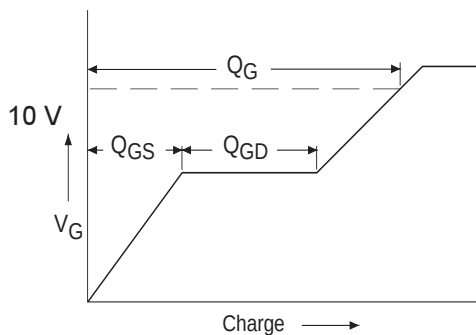


Fig 13a. Basic Gate Charge Waveform

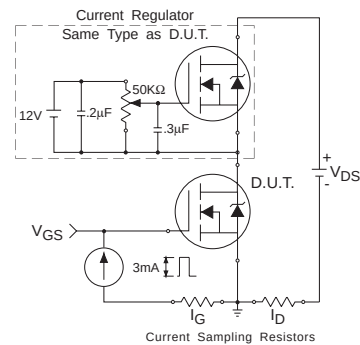
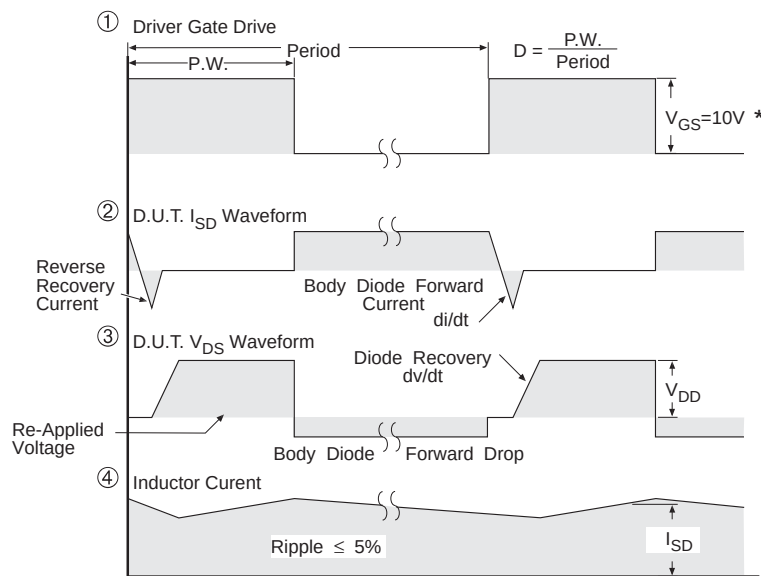
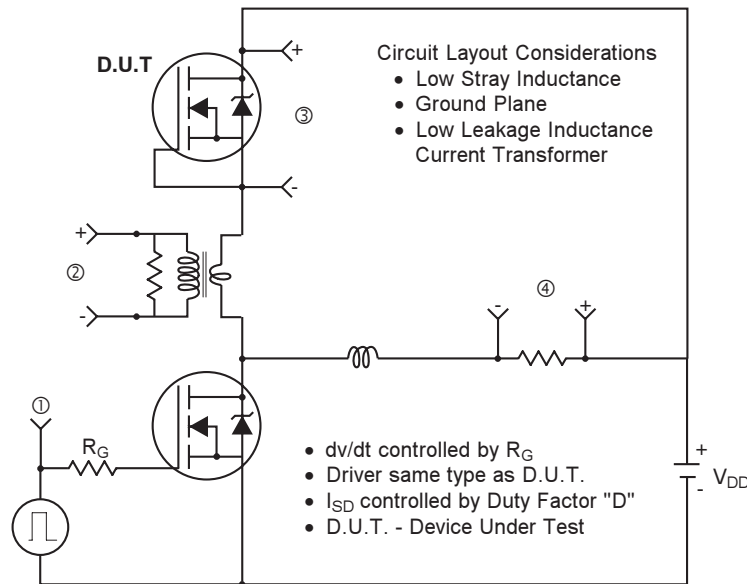


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

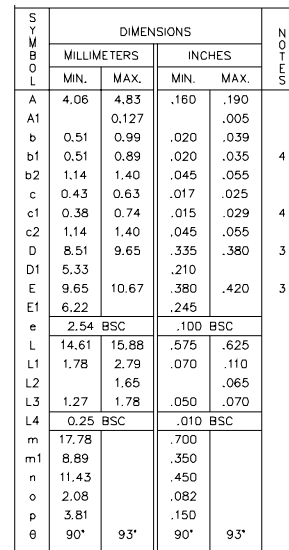


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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Dimensions are shown in millimeters (inches)



HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

• PART DEPENDENT.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON VV 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

ASSEMBLY LOT CODE

F530S
002L
80
24

OR

Diagram of an International Rectifier diode with the following markings and callouts:

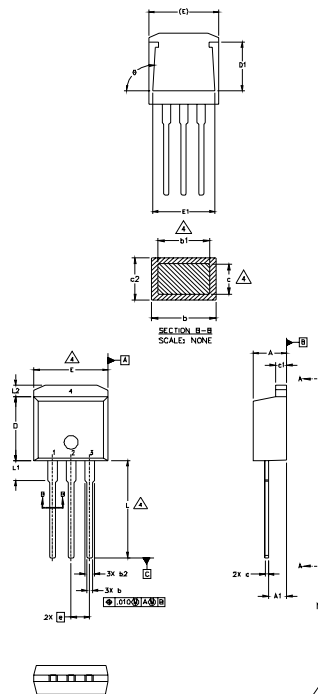
- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the diode body.
- PART NUMBER**: Points to the text "F530S" on the diode body.
- DATE CODE**: Points to the text "10P002A" on the diode body.
- ASSEMBLY LOT CODE**: Points to the numbers "80" and "24" on the diode body.

Additional information provided:

- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**
- YEAR 0 = 2000**
- WEEK 02**
- A = ASSEMBLY SITE CODE**

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

- 1. - GATE
- 2. - DRAIN
- 3. - SOURCE
- 4. - DRAIN

IGBT

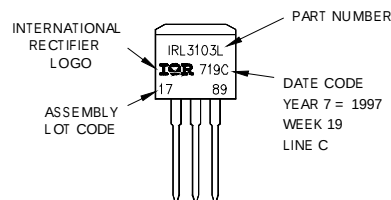
- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
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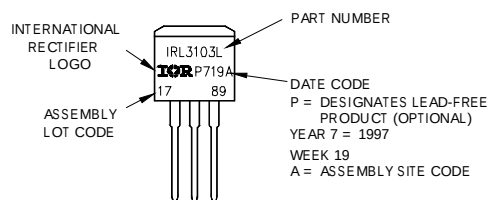
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



OR

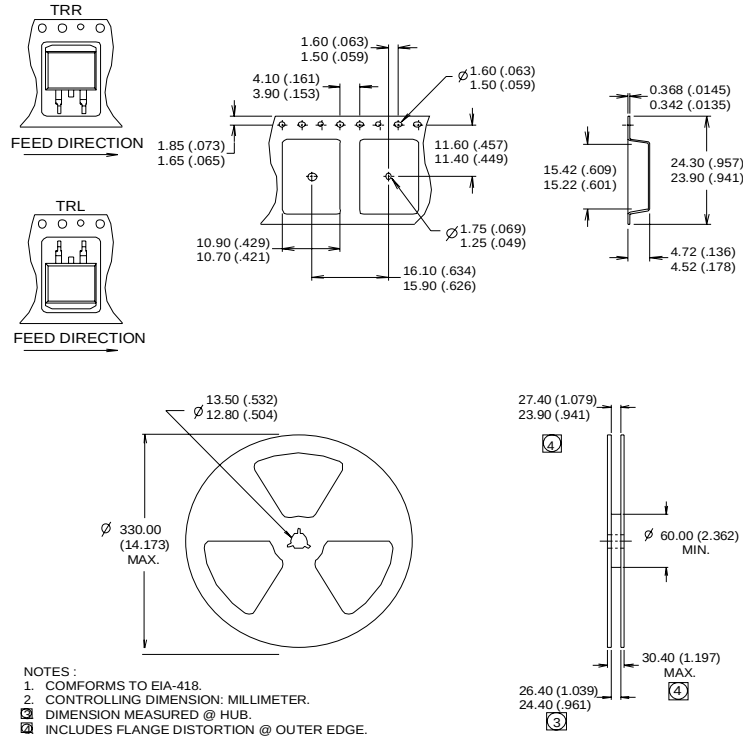


IRF8010S/LPbF

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)

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Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.31\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 45\text{A}$.
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ $R_{th(jc)}$ (end of life) is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium in worse case PCB mounting condition of material (solder/substrate), process and re-flow temperature.
- ⑥ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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