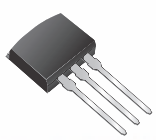
IRF9Z34S, SiHF9Z34S, IRF9Z34L, SiHF9Z34L

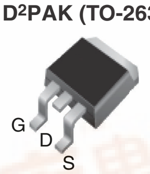
Vishay Siliconix

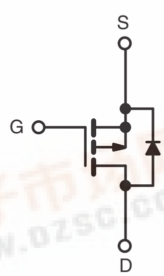
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 60	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	0.14
Q_g (Max.) (nC)	34	
Q_{gs} (nC)	9.9	
Q_{gd} (nC)	16	
Configuration	Single	

I[2]PAK (TO-262)   D[2]PAK (TO-263)







P-Channel MOSFET

FEATURES

- Advanced Process Technology
- Surface Mount (IRF9Z34S/SiHF9Z34S)
- Low-Profile Through-Hole (IRSiHF9Z34L/SiHF9Z34L)
- 175 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead (Pb)-free Available

Pb Available

RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D[2]PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D[2]PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRSiHF9Z34L/SiHF9Z34L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D[2]PAK (TO-263)	D[2]PAK (TO-263)	D[2]PAK (TO-263)	I[2]PAK (TO-262)
Lead (Pb)-free	IRF9Z34SPbF	IRF9Z34STRLPbF[a]	IRF9Z34STRRPbF[a]	IRF9Z34LPbF
	SiHF9Z34S-E3	SiHF9Z34STL-E3[a]	SiHF9Z34STR-E3[a]	SiHF9Z34L-E3
SnPb	IRF9Z34S	IRF9Z34STRL[a]	IRF9Z34STRR[a]	IRF9Z34L
	SiHF9Z34S	SiHF9Z34STL[a]	SiHF9Z34STR[a]	SiHF9Z34L

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 60	V
Gate-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 18	A
		T_C = 100 °C		- 13	
Pulsed Drain Current[a, e]			I_{DM}	- 72	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy[b, e]			E_{AS}	370	mJ
Avalanche Current[a]			I_{AR}	- 18	A
Repetitive Avalanche Energy[a]			E_{AR}	8.8	mJ

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Maximum Power Dissipation	T_C = 25 °C	P_D	3.7	W
	T_A = 25 °C		88	
Peak Diode Recovery dV/dt[c, e]		dV/dt	- 4.5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300[d]	

Notes

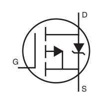
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 1.3 mH, R_G = 25 Ω, I_{AS} = - 18 A (see fig. 12).
c. I_{SD} ≤ - 18 A, dI/dt ≤ 170 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
d. 1.6 mm from case.
e. Uses IRF9Z34/SiHF9Z34 data and test conditions.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB Mounted, steady-state)[a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA		- 60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA[c]		-	- 0.06	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 60 V, V_{GS} = 0 V		-	-	- 100	µA
		V_{DS} = - 48 V, V_{GS} = 0 V, T_J = 150 °C		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 11 A[b]	-	-	0.14	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 25 V, I_D = - 11 A[c]		5.9	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 5[c]		-	1100	-	pF
Output Capacitance	C_{oss}			-	620	-	
Reverse Transfer Capacitance	C_{rss}			-	100	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 18 A, V_{DS} = - 48 V, see fig. 6 and 13[b, c]	-	-	34	nC
Gate-Source Charge	Q_{gs}			-	-	9.9	
Gate-Drain Charge	Q_{gd}			-	-	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 30 V, I_D = - 18 A, R_G = 12 Ω, R_D = 1.5 Ω, see fig. 10[b, c]		-	18	-	ns
Rise Time	t_r			-	120	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	58	-	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 18	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	- 72	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 18 A, V_{GS} = 0 V[b]	-	-	- 6.3	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 18 A, dI/dt = 100 A/µs[b, c]	-	100	200	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	280	520	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. Uses IRF9Z34/SiHF9Z34 data and test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

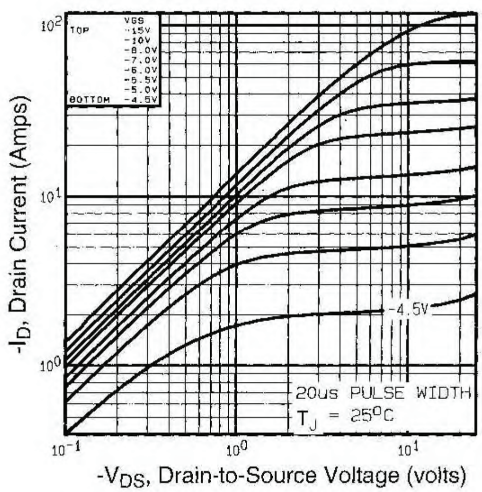


Fig. 1 - Typical Output Characteristics

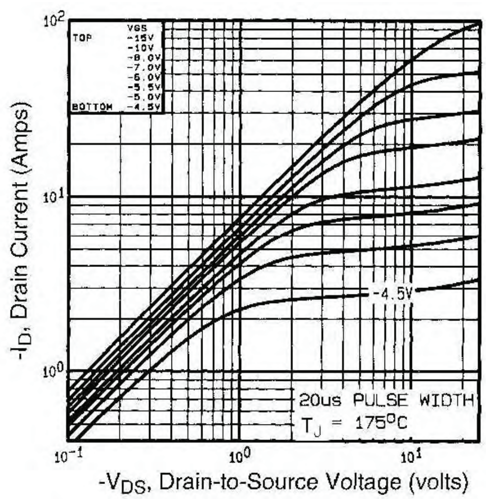


Fig. 2 - Typical Output Characteristics

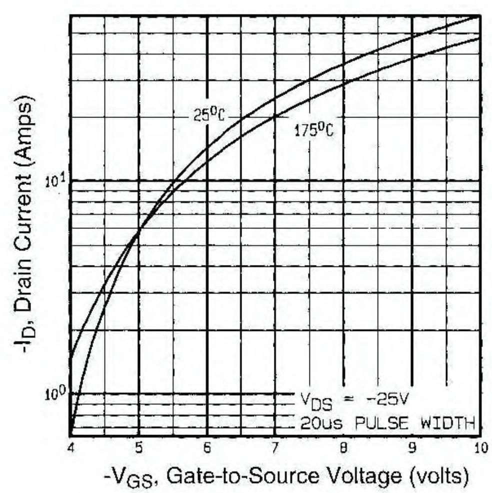


Fig. 3 - Typical Transfer Characteristics

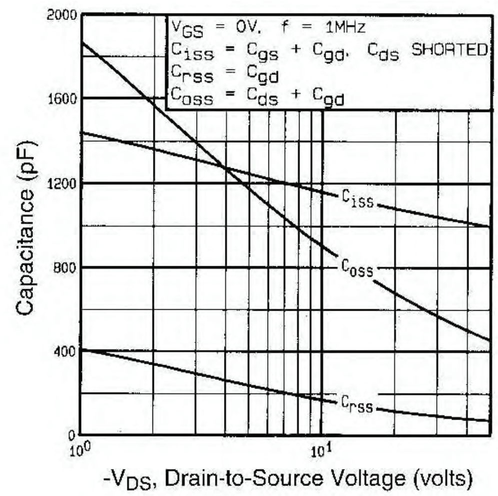


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

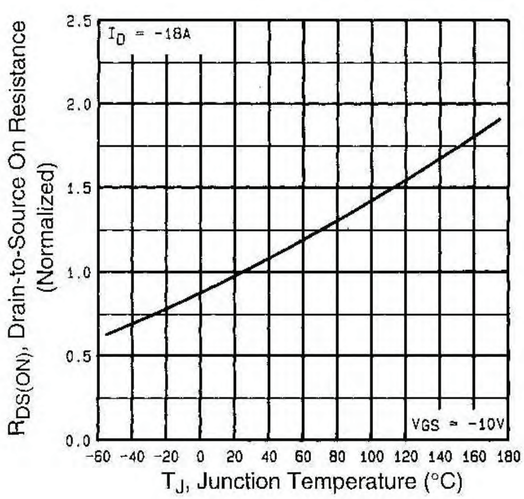


Fig. 4 - Normalized On-Resistance vs. Temperature

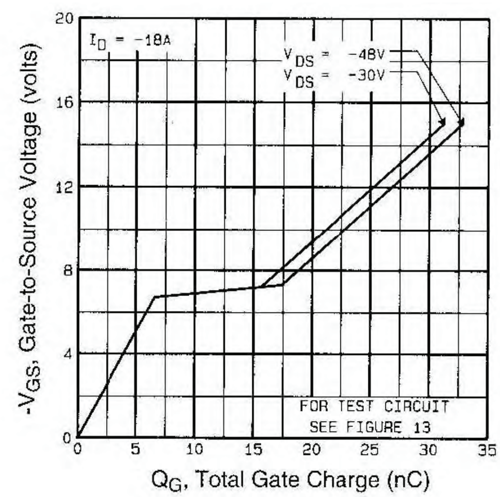


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

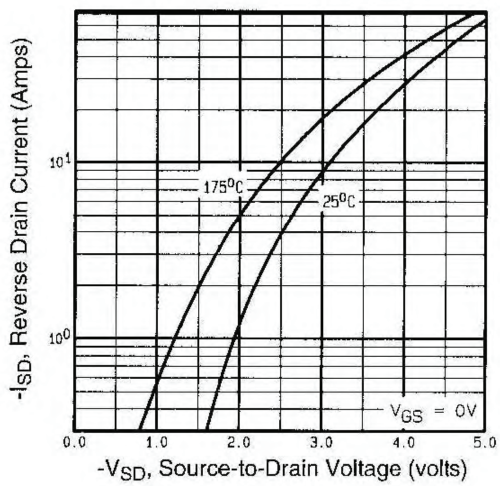


Fig. 7 - Typical Source-Drain Diode Forward Voltage

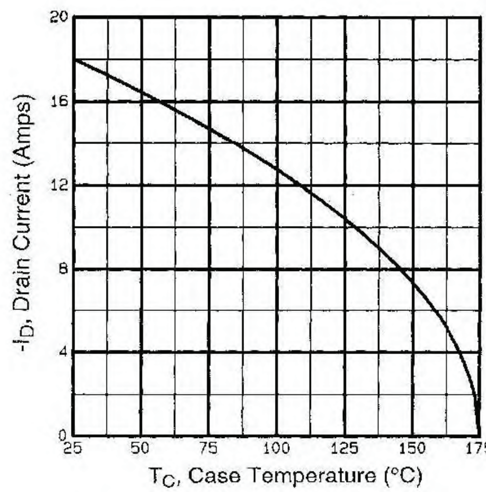


Fig. 9 - Maximum Drain Current vs. Case Temperature

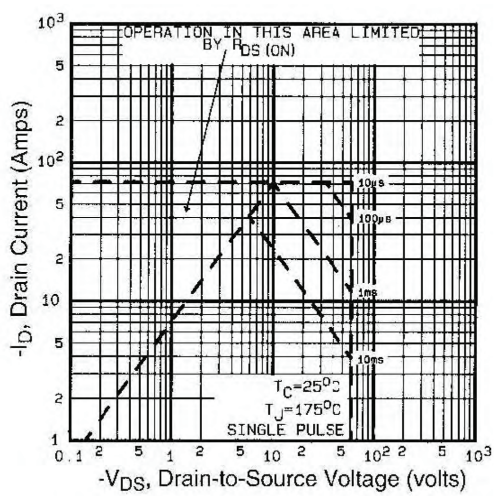


Fig. 8 - Maximum Safe Operating Area

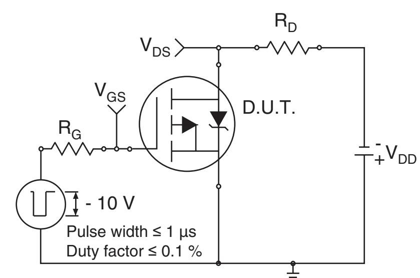


Fig. 10a - Switching Time Test Circuit

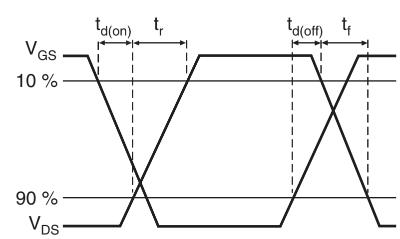


Fig. 10b - Switching Time Waveforms

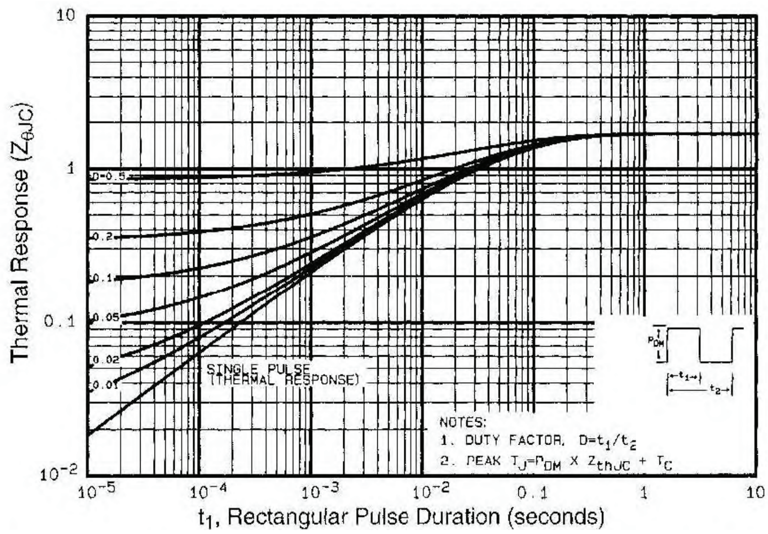


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

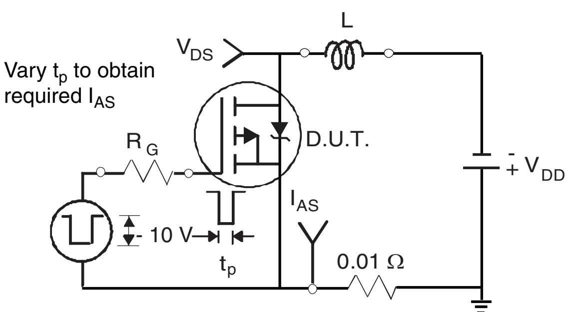


Fig. 12a - Unclamped Inductive Test Circuit

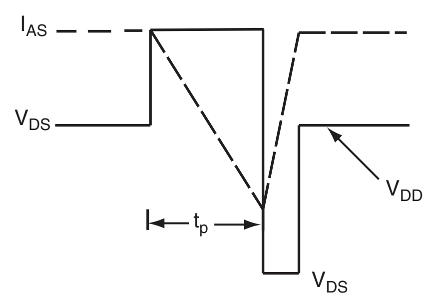


Fig. 12b - Unclamped Inductive Waveforms

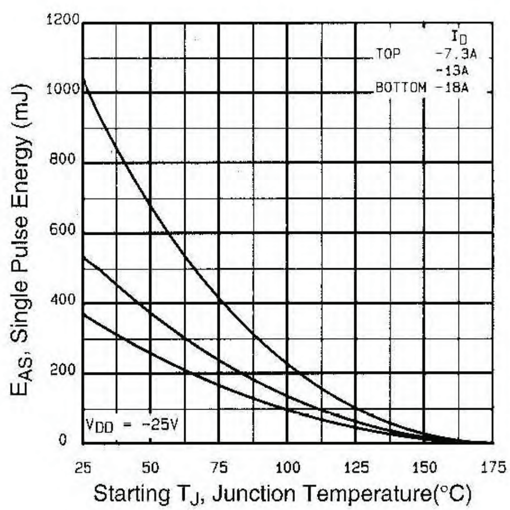


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

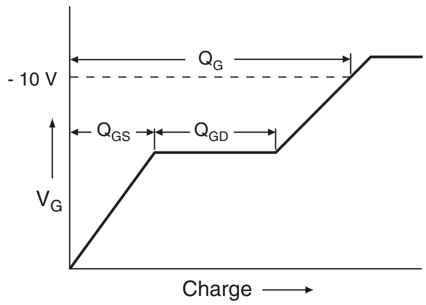


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

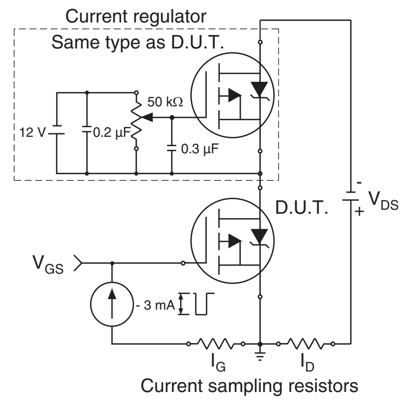
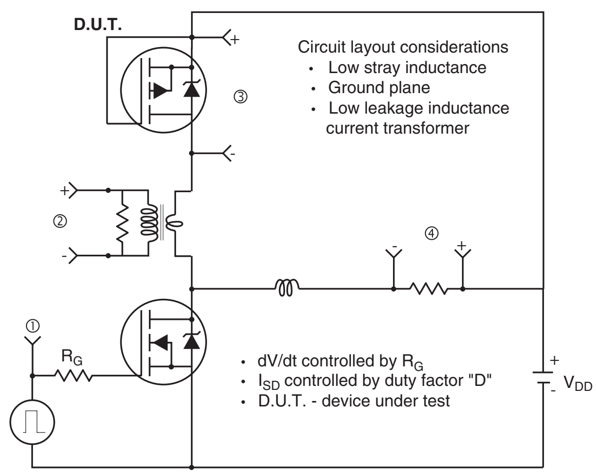
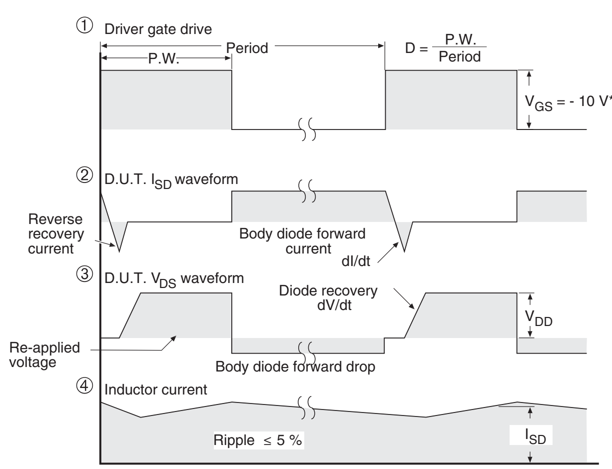


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

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