

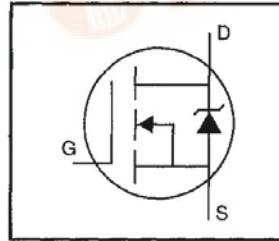
# International IR Rectifier

PD-95979

## IRLD120PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS}=4V$  &  $5V$
- 175°C Operating Temperature
- Lead-Free



$$V_{DSS} = 100V$$

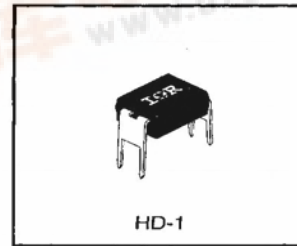
$$R_{DS(on)} = 0.27\Omega$$

$$I_D = 1.3A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	1.3	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	0.94	
$I_{DM}$	Pulsed Drain Current ①	10	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
$V_{GS}$	Gate-to-Source Voltage	±10	V
$E_{AS}$	Single Pulse Avalanche Energy ②	690	mJ
$I_{AR}$	Avalanche Current ①	1.3	A
$E_{AR}$	Repetitive Avalanche Energy ①	0.13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

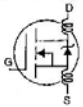
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W



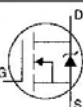
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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

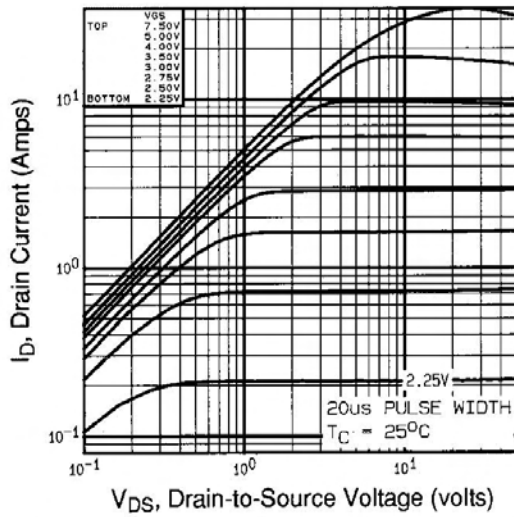
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	V <sub>GS</sub> =5.0V, I <sub>D</sub> =0.78A ④
		—	—	0.38		V <sub>GS</sub> =4.0V, I <sub>D</sub> =0.65A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	1.9	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =0.78A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =10V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> =-10V
Q <sub>g</sub>	Total Gate Charge	—	—	12	nC	I <sub>D</sub> =9.2A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	3.0		V <sub>DS</sub> =80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	7.1		V <sub>GS</sub> =5.0V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.8	—	ns	V <sub>DD</sub> =50V
t <sub>r</sub>	Rise Time	—	64	—		I <sub>D</sub> =9.2A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	21	—		R <sub>G</sub> =9.0Ω
t <sub>f</sub>	Fall Time	—	27	—		R <sub>D</sub> =5.2Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	6.0	—		
C <sub>ISS</sub>	Input Capacitance	—	490	—	pF	V <sub>GS</sub> =0V
C <sub>OSS</sub>	Output Capacitance	—	150	—		V <sub>DS</sub> = 25V
C <sub>RSS</sub>	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 5

## Source-Drain Ratings and Characteristics

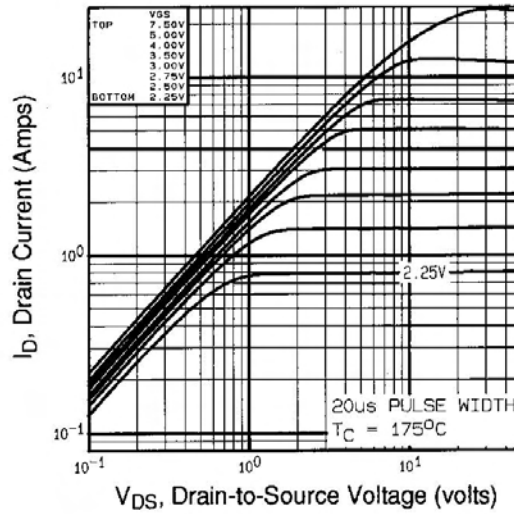
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	1.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	10		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =1.3A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	130	140	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =9.2A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.83	1.0	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

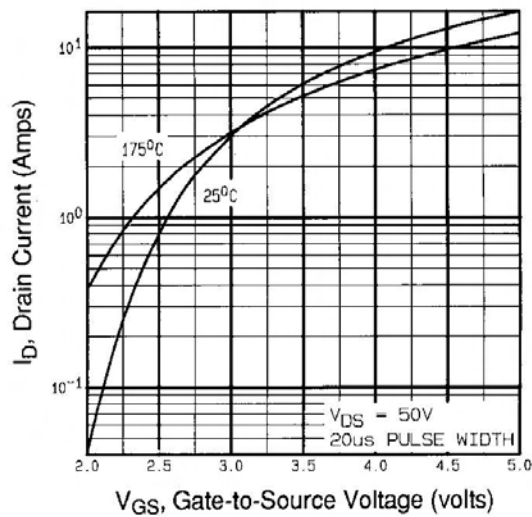
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=153mH  
R<sub>G</sub>=25Ω, I<sub>AS</sub>=2.6A (See Figure 12)
- ③ I<sub>SD</sub>≤9.2A, di/dt≤110A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>,  
T<sub>J</sub>≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



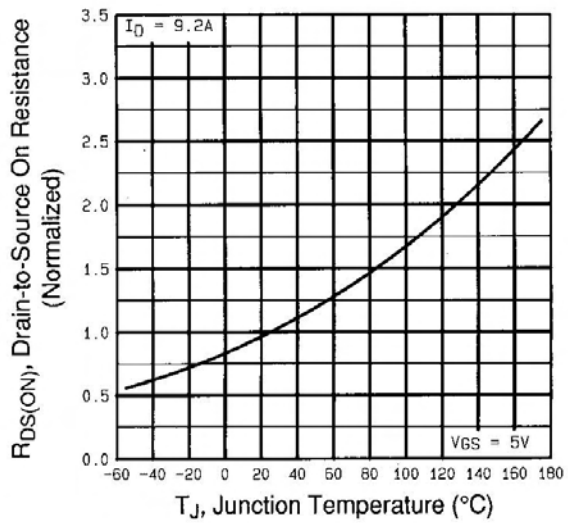
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^{\circ}\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^{\circ}\text{C}$



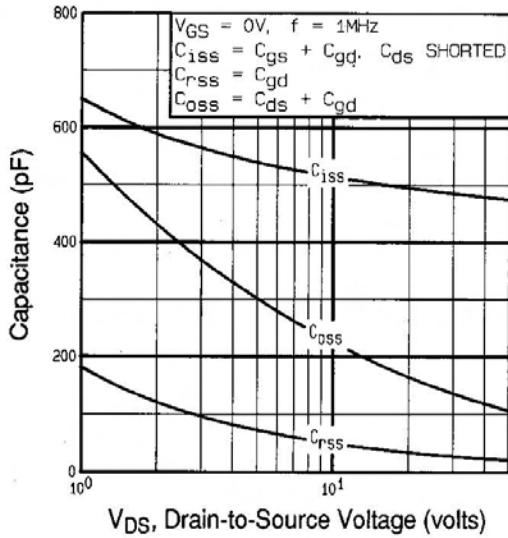
**Fig 3.** Typical Transfer Characteristics



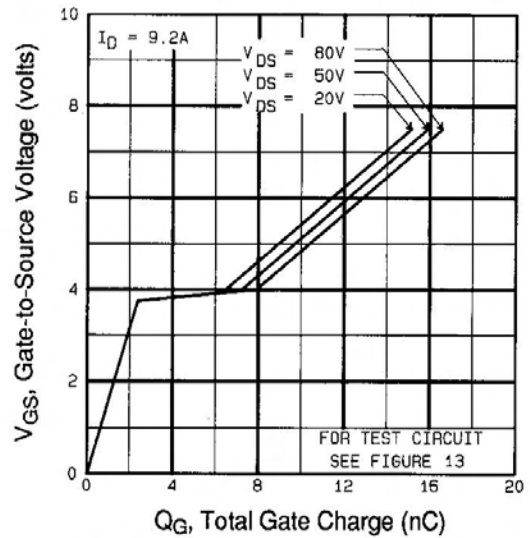
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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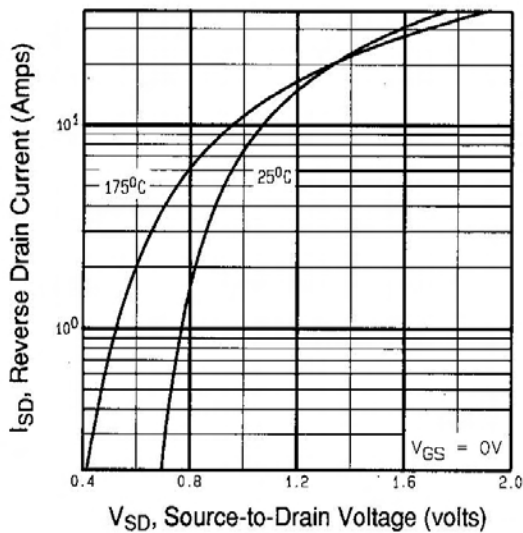
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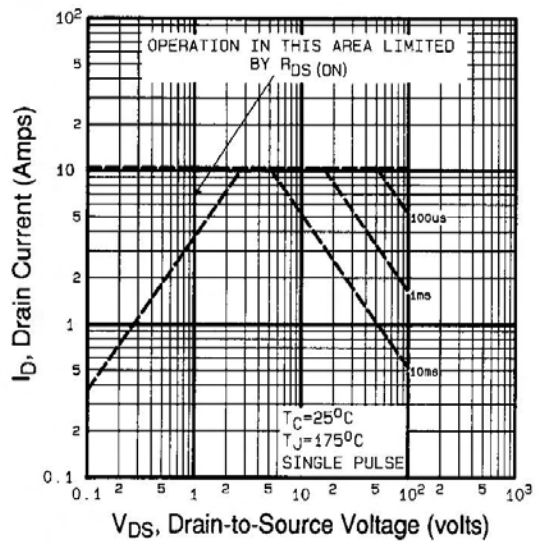
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



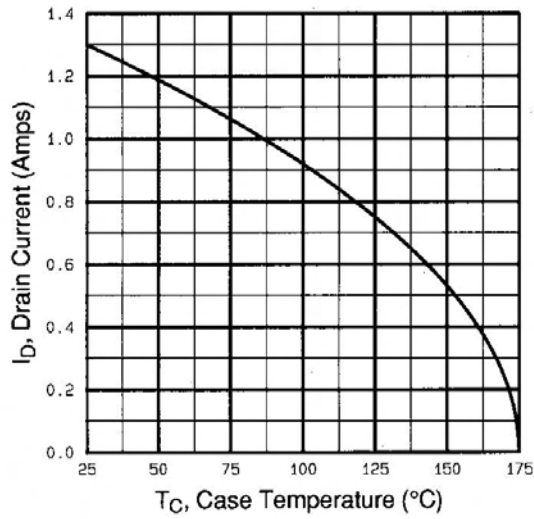
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



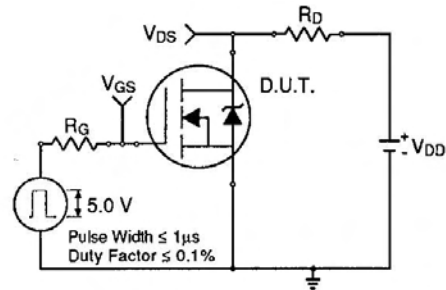
**Fig 7.** Typical Source-Drain Diode Forward Voltage



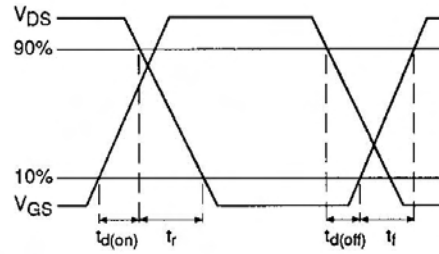
**Fig 8.** Maximum Safe Operating Area



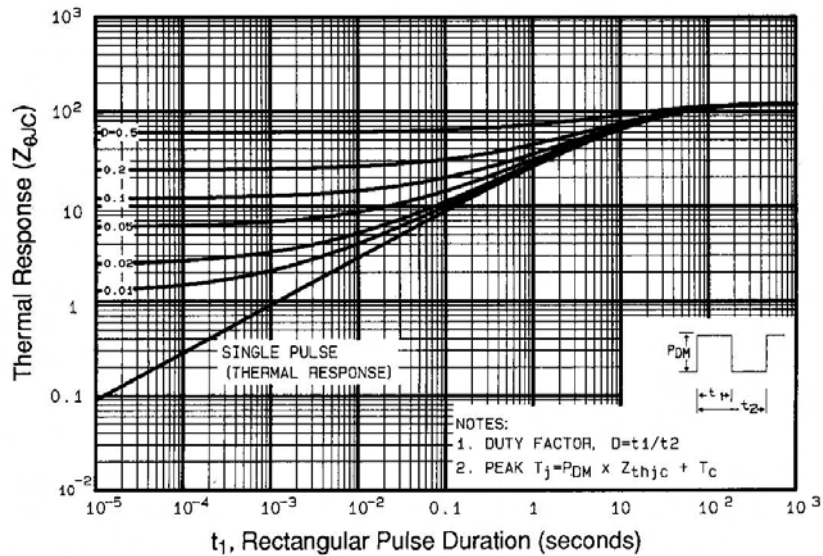
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



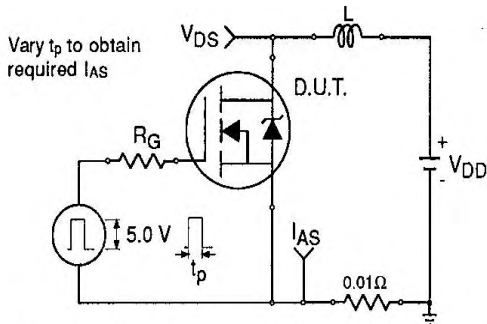
**Fig 10b.** Switching Time Waveforms



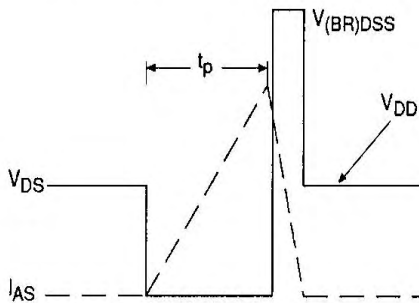
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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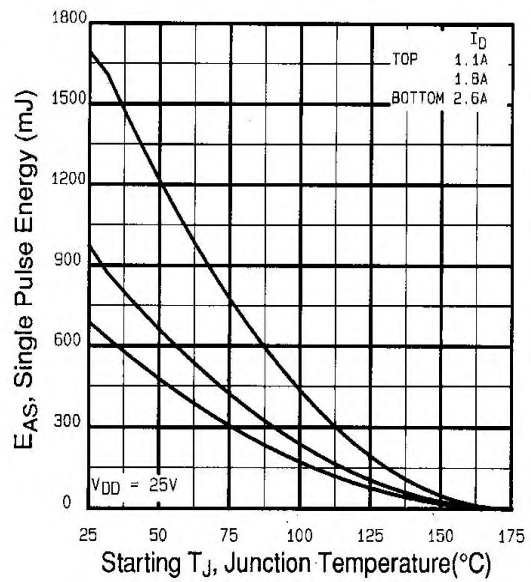
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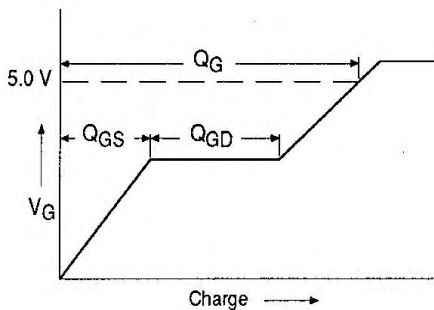
**Fig 12a.** Unclamped Inductive Test Circuit



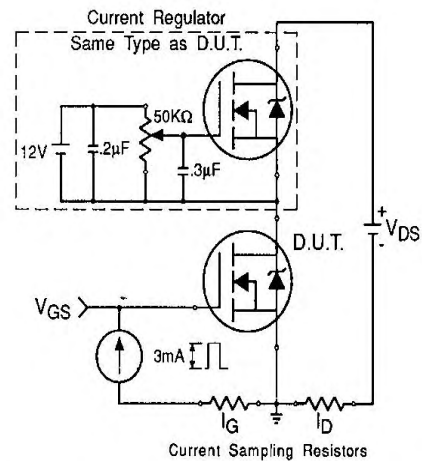
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

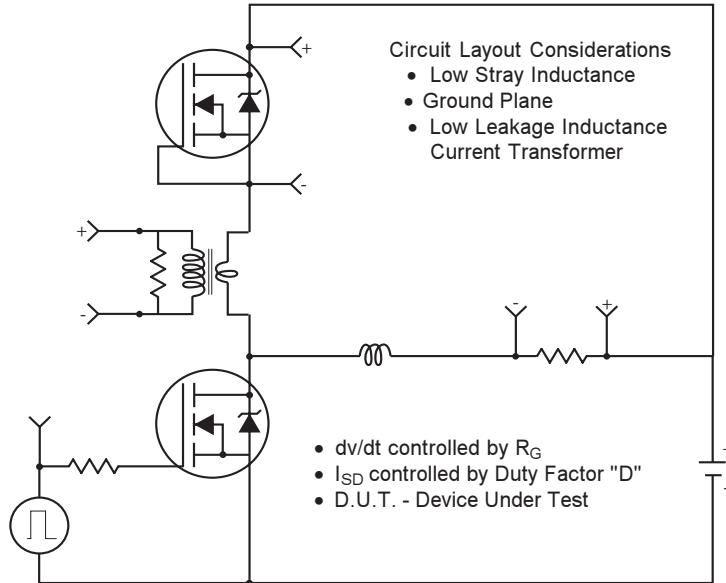


**Fig 13a.** Basic Gate Charge Waveform



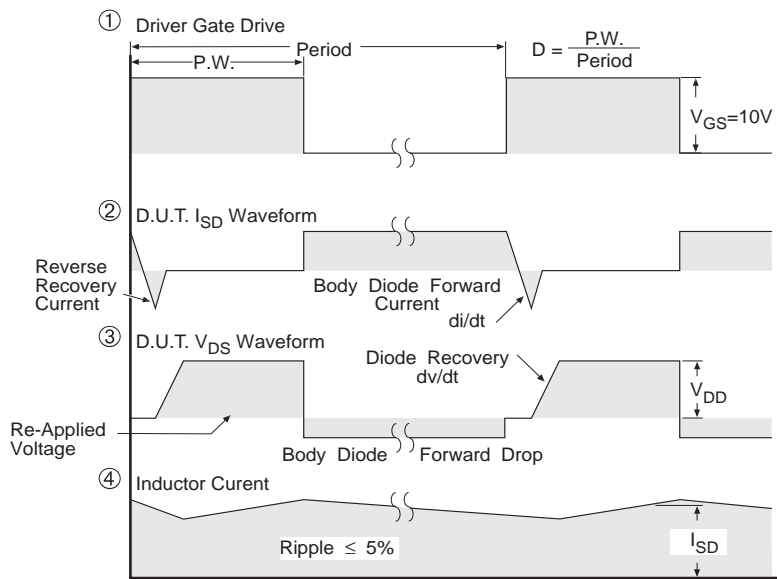
**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 14** For N Channel HEXFETS

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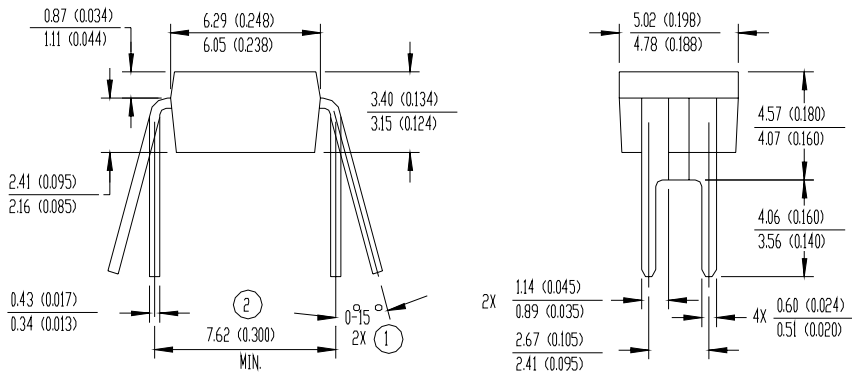
## Hexdip Package Outline

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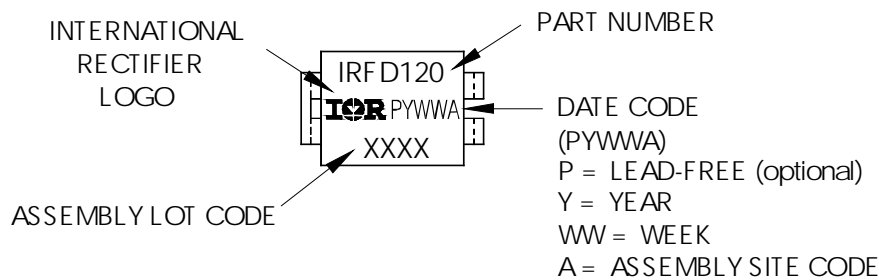
NOTES:

- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
- ② APPLIES TO INSTALLED LEAD CENTERS
- 3 CONTROLLING DIMENSION: INCH
- 4 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
- 5 CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
- 6 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP  
SOLDER DIP MAX. + 0.16 (0.006)



## Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



Data and specifications subject to change without notice.

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