

International IR Rectifier

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 5.0\text{V}$	76	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 5.0\text{V}$	54	
I_{DM}	Pulsed Drain Current ①⑥	470	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	63	W
	Linear Derating Factor	0.42	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②④	610	mJ
I_{AR}	Avalanche Current ①⑥	71	A
E_{AR}	Repetitive Avalanche Current ①	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw.	300 (1.6mm from case) 10 lbf·in (1.1N·m)	

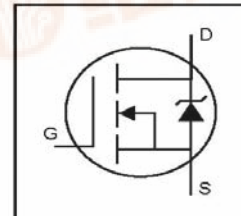
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

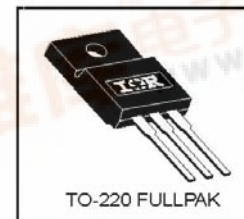
PD-95642

IRLI3803PbF

HEXFET® Power MOSFET



$V_{DS} = 30\text{V}$
$R_{DS(on)} = 0.006\Omega$
$I_D = 76\text{A}$



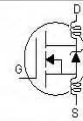
TO-220 FULLPAK

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C , $I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.006	Ω	$V_{GS} = 10V$, $I_D = 40A$ ④
		—	—	0.009		$V_{GS} = 4.5V$, $I_D = 34A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	55	—	—	S	$V_{DS} = 25V$, $I_D = 71A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	140	nC	$I_D = 71A$
Q_{gs}	Gate-to-Source Charge	—	—	41		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	78		$V_{GS} = 4.5V$, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	230	—		$I_D = 71A$
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		$R_G = 1.3\Omega$, $V_{GS} = 4.5V$
t_f	Fall Time	—	35	—		$R_D = 0.20\Omega$, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package and center of die contact
C_{iss}	Input Capacitance	—	5000	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1800	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	880	—		$f = 1.0MHz$, See Fig. 5⑥
C	Drain to Sink Capacitance	—	12	—		$f = 1.0MHz$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	76	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	470		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 40A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	$T_J = 25^\circ\text{C}$, $I_F = 71A$
Q_{rr}	Reverse Recovery Charge	—	450	680	nC	$di/dt = 100A/\mu s$ ④⑥

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 ② $V_{DD} = 15V$, starting $T_J = 25^\circ\text{C}$, $L = 180\mu H$
 $R_G = 25\Omega$, $I_{AS} = 71A$. (See Figure 12)
 ③ $I_{SD} \leq 71A$, $di/dt \leq 130A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
 ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
 ⑤ $t = 60s$, $f = 60Hz$
 ⑥ Uses IRL3803 data and test conditions

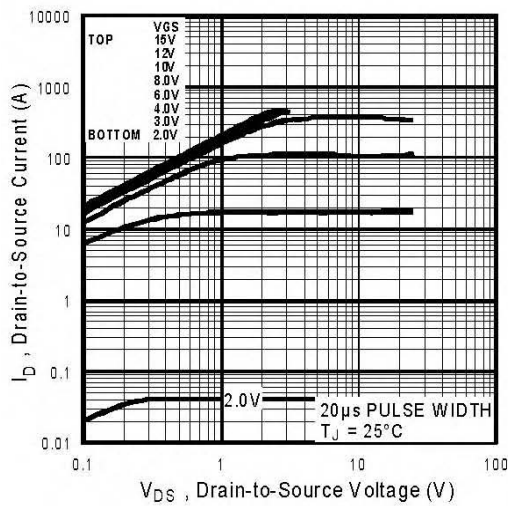


Fig 1. Typical Output Characteristics

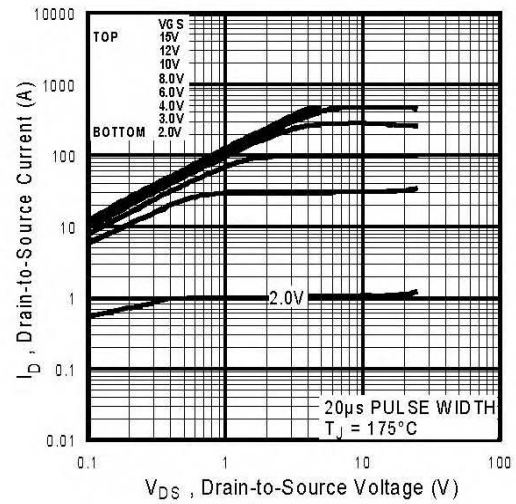


Fig 2. Typical Output Characteristics

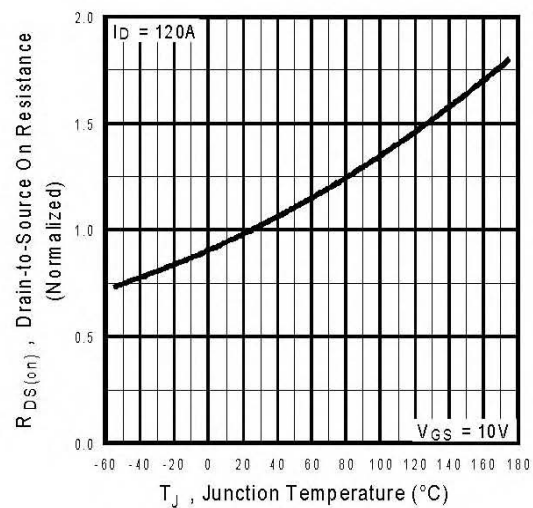
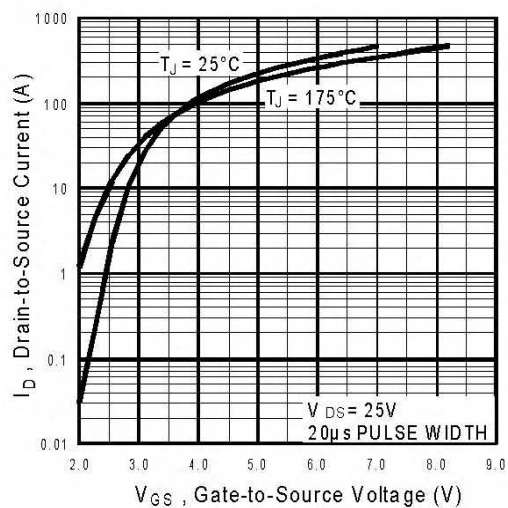


Fig 4. Normalized On-Resistance
Vs. Temperature

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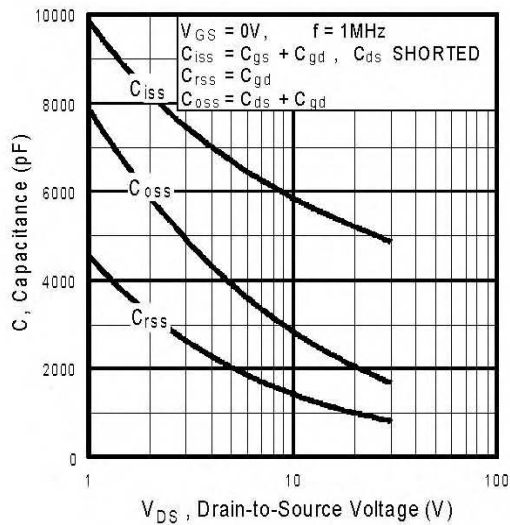


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

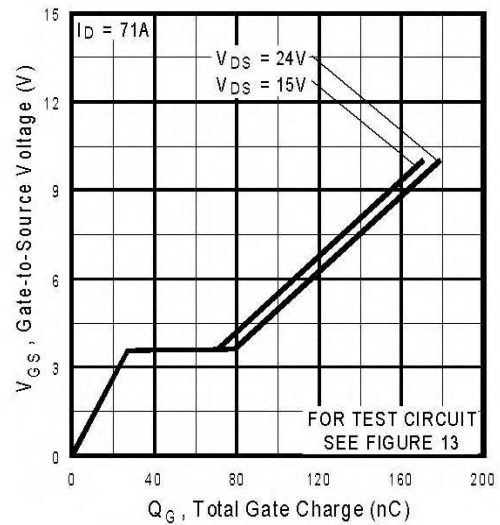


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

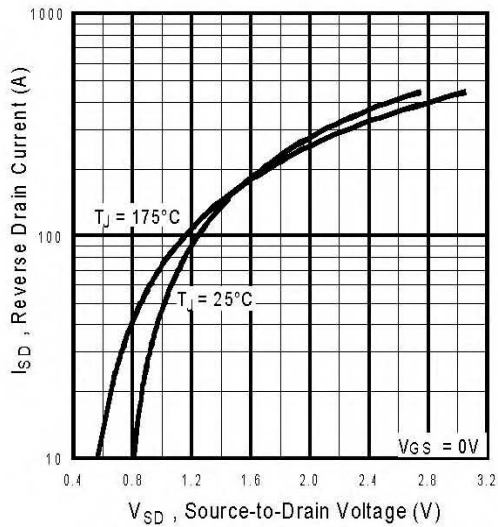


Fig 7. Typical Source-Drain Diode Forward Voltage

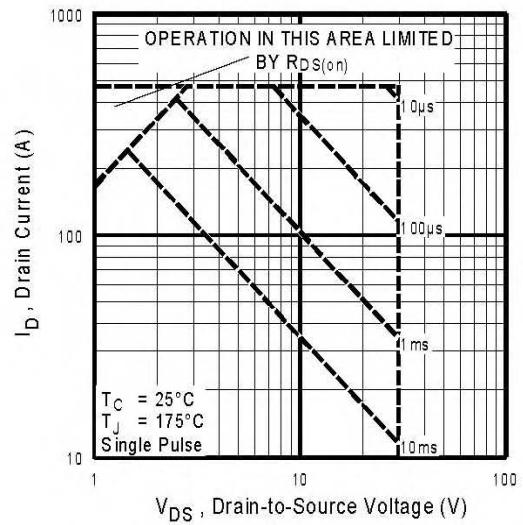


Fig 8. Maximum Safe Operating Area

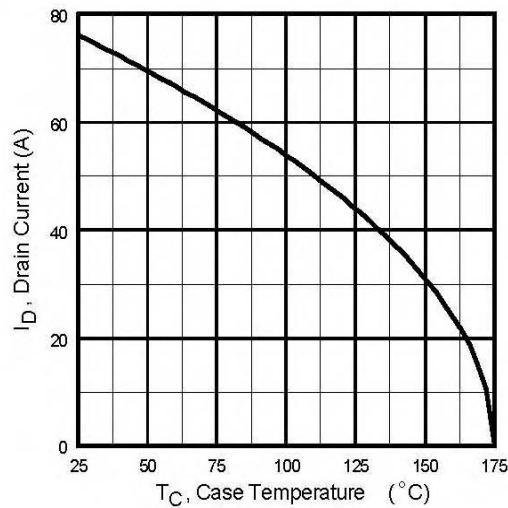


Fig 9. Maximum Drain Current Vs. Case Temperature

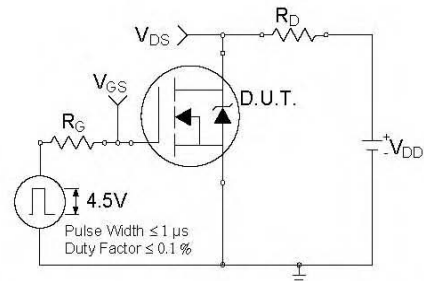


Fig 10a. Switching Time Test Circuit

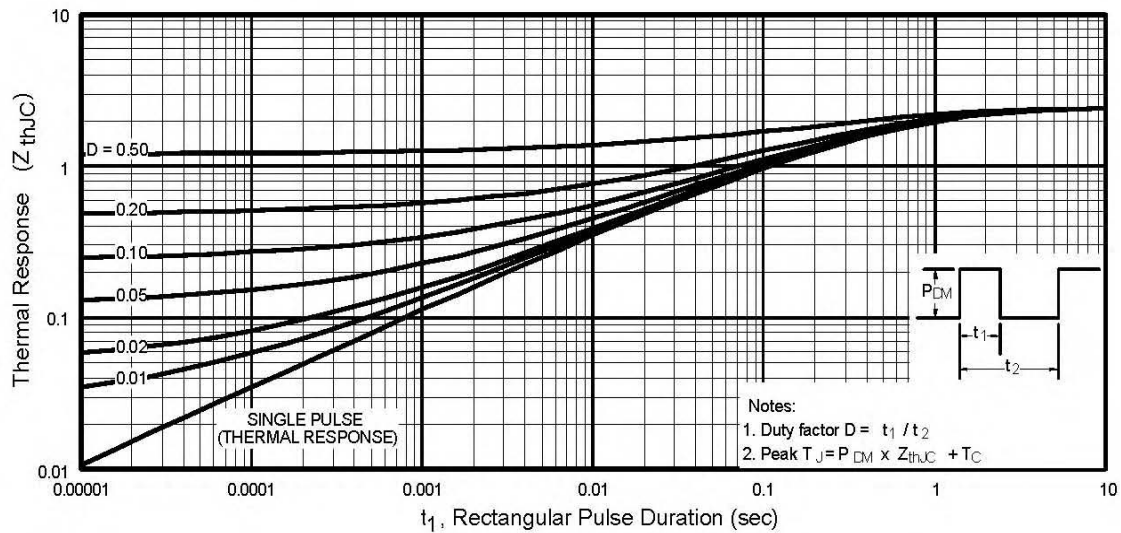
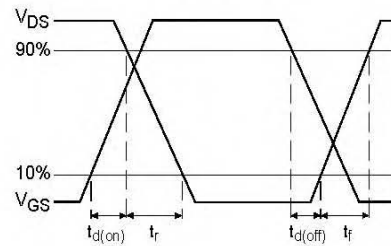


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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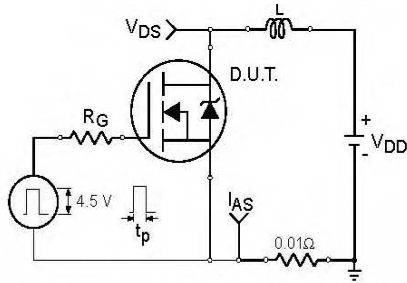


Fig 12a. Unclamped Inductive Test Circuit

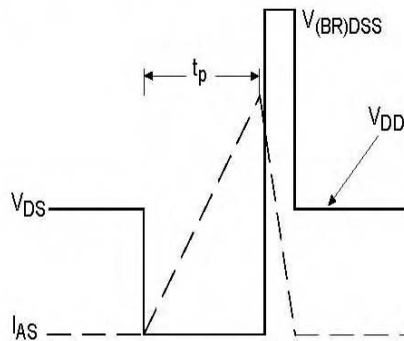


Fig 12b. Unclamped Inductive Waveforms

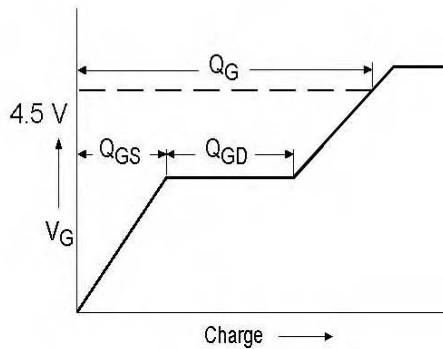


Fig 13a. Basic Gate Charge Waveform

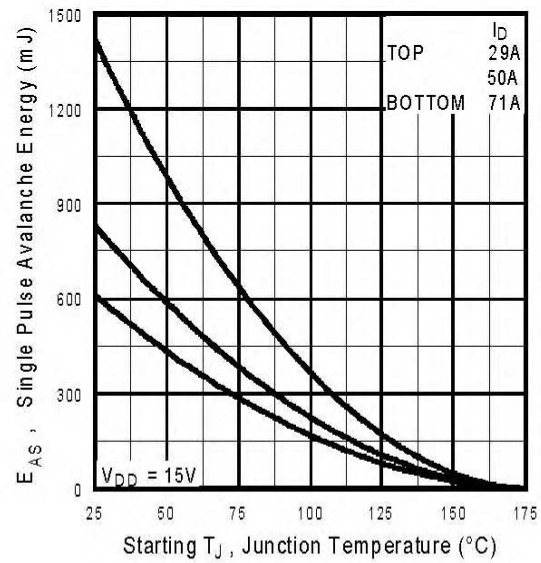


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

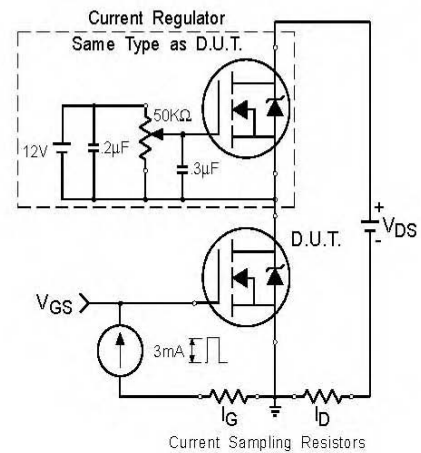
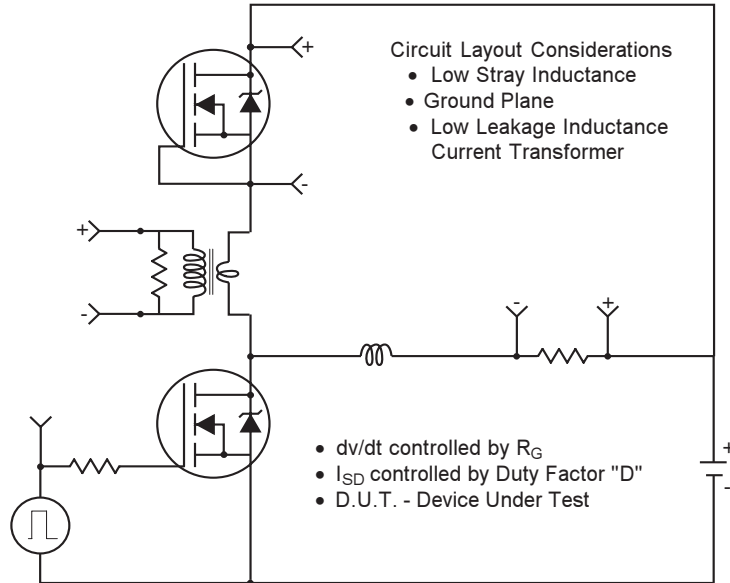


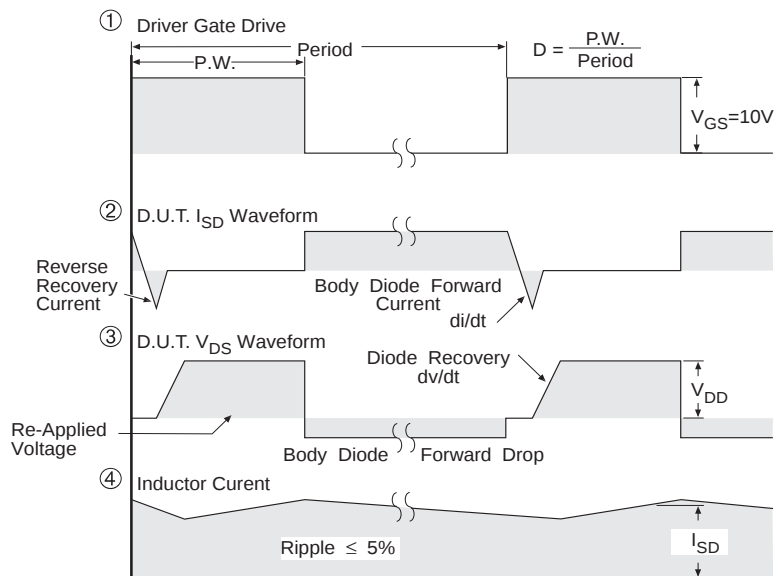
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

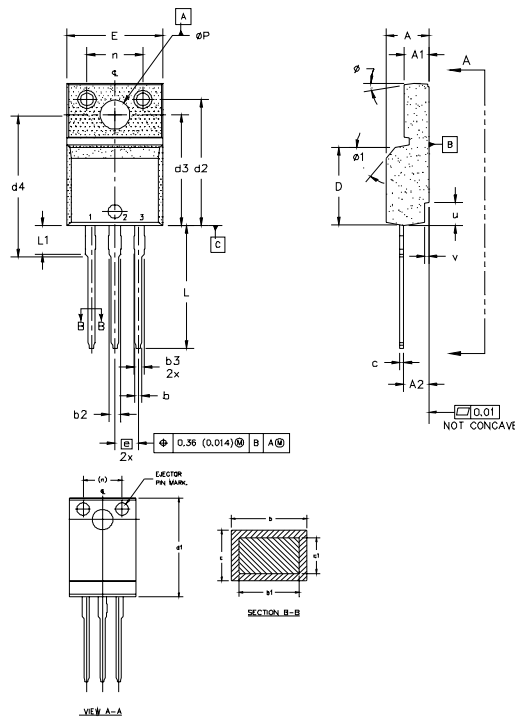
Fig -14 For N Channel HEXFETS

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TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



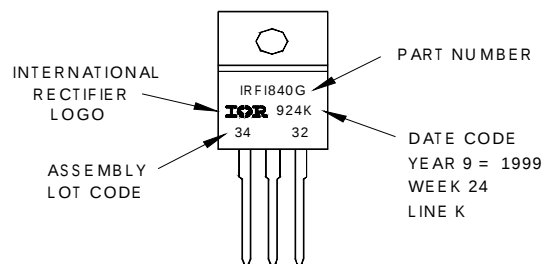
NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	0.180	0.190		
A1	2.57	2.83	0.101	0.114		HEXFET
A2	2.51	2.85	0.099	0.112		
b	0.622	0.89	0.024	0.035		1. - GATE
b1	0.622	0.838	0.024	0.033	5	2. - DRAIN
b2	1.229	1.400	0.048	0.055		3. - SOURCE
b3	1.229	1.400	0.048	0.055		
c	0.440	0.629	0.017	0.025		
c1	0.440	0.584	0.017	0.023		IGBTs, CoPAK
D	8.65	9.80	0.341	0.386	4	1. - GATE
d1	15.80	16.12	0.622	0.635		2. - COLLECTOR
d2	13.97	14.22	0.550	0.560		3. - EMITTER
d3	12.30	12.92	0.484	0.509		
d4	8.64	9.91	0.340	0.390		
E	10.36	10.63	0.408	0.419	4	
e	2.54 BSC		0.100 BSC			
L	13.20	13.73	0.520	0.541		
L1	3.10	3.50	0.122	0.138	3	
n	6.05	6.15	0.238	0.242		
øP	3.05	3.45	0.120	0.136		
u	2.40	2.50	0.094	0.098	6	
v	0.40	0.50	0.016	0.020	6	
ø	3"	7"	3"	7"		
ø1		45°		45°		

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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