

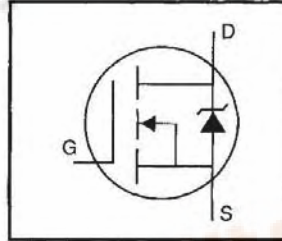
# International IR Rectifier

PD - 95601A

HEXFET® Power MOSFET

## IRLR110PbF IRLU110PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR110)
- Straight Lead (IRLU110)
- Available in Tape & Reel
- Logic-Level Gate Drive
- RDS(on) Specified at VGS=4V & 5V
- Lead-Free

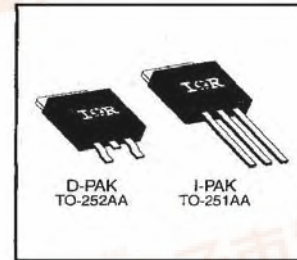


$V_{DSS} = 100V$   
 $R_{DS(on)} = 0.54\Omega$   
 $I_D = 4.3A$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	4.3	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	2.7	
$I_{DM}$	Pulsed Drain Current ①	17	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	25	
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.5	W/°C
	Linear Derating Factor	0.20	
	Linear Derating Factor (PCB Mount)**	0.020	
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	100	mJ
$I_{AR}$	Avalanche Current ①	4.3	A
$E_{AR}$	Repetitive Avalanche Energy ①	2.5	mJ
	Peak Diode Recovery dv/dt ③	5.5	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).

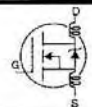
For recommended footprint and soldering techniques refer to application note #AN-994.

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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

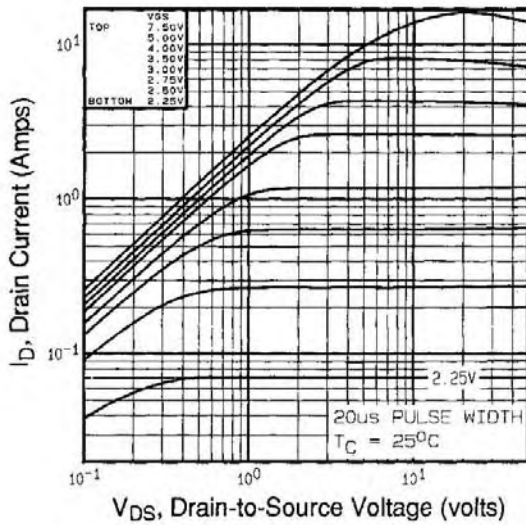
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.54	Ω	V <sub>GS</sub> =5.0V, I <sub>D</sub> =2.6A ④
		—	—	0.76		V <sub>GS</sub> =4.0V, I <sub>D</sub> =2.2A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	2.3	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =2.6A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =10V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> =-10V
Q <sub>g</sub>	Total Gate Charge	—	—	6.1	nC	I <sub>D</sub> =5.6A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	2.0		V <sub>DS</sub> =80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	3.3		V <sub>GS</sub> =5.0V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.3	—	ns	V <sub>DD</sub> =50V
t <sub>r</sub>	Rise Time	—	47	—		I <sub>D</sub> =5.6A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	16	—		R <sub>G</sub> =12Ω
t <sub>f</sub>	Fall Time	—	17	—		R <sub>D</sub> =8.4Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	250	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	80	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

## Source-Drain Ratings and Characteristics

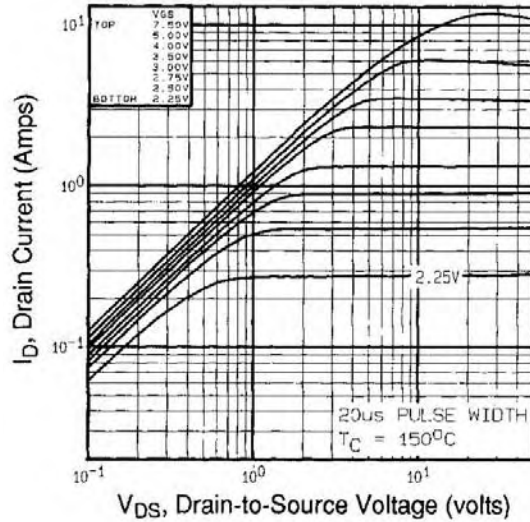
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	4.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	17		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =4.3A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	100	130	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =5.6A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.50	0.65	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

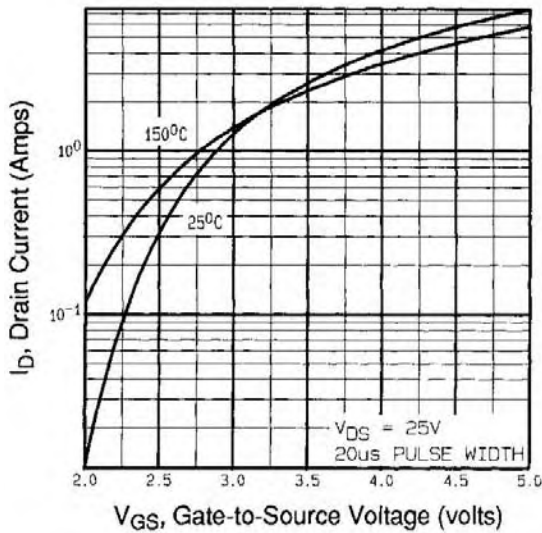
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=8.1mH R<sub>G</sub>=25Ω, I<sub>AS</sub>=4.3A (See Figure 12)
- ③ I<sub>SD</sub>≤5.6A, di/dt≤140A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



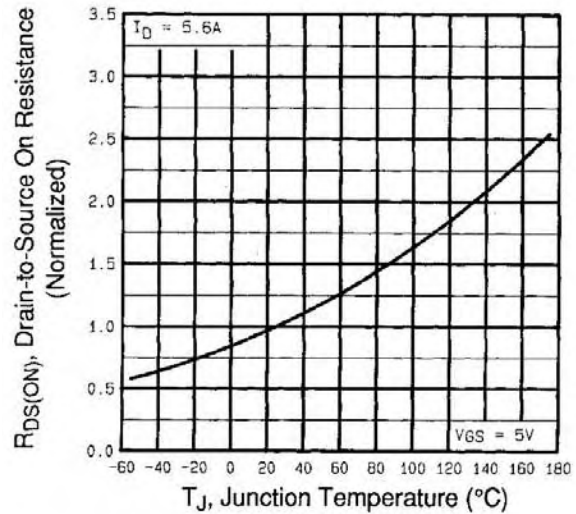
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



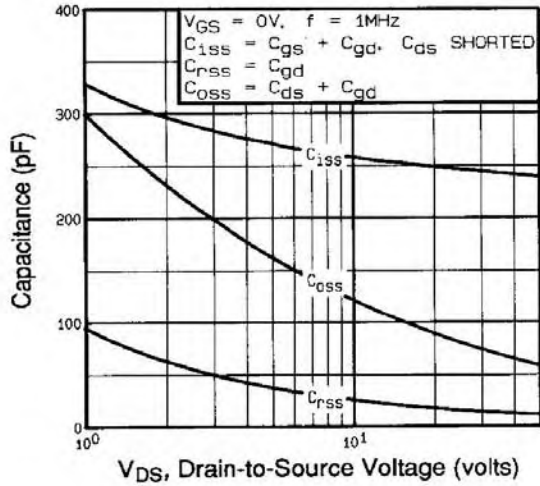
**Fig 3.** Typical Transfer Characteristics



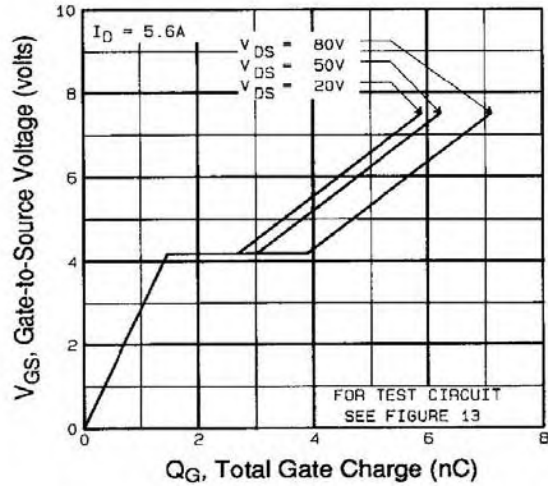
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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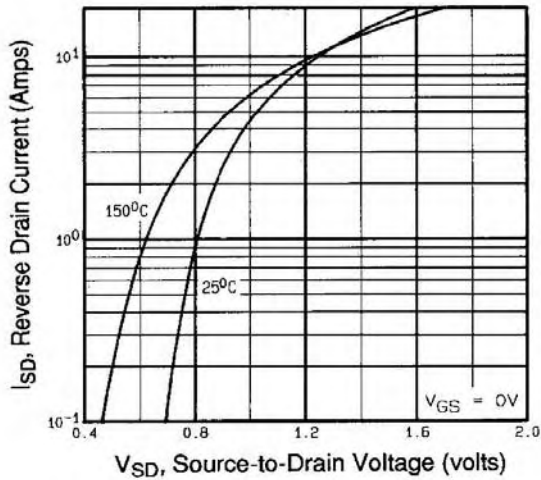
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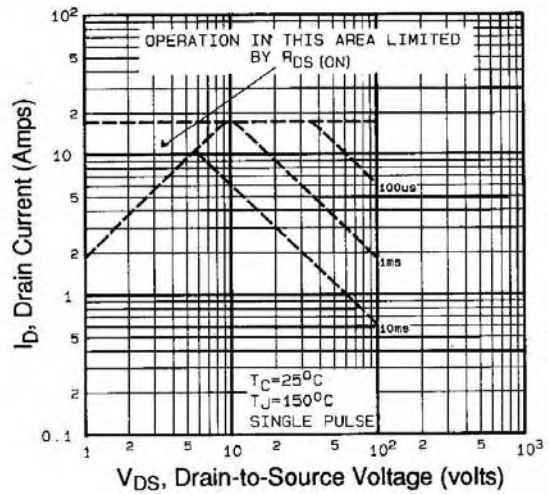
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



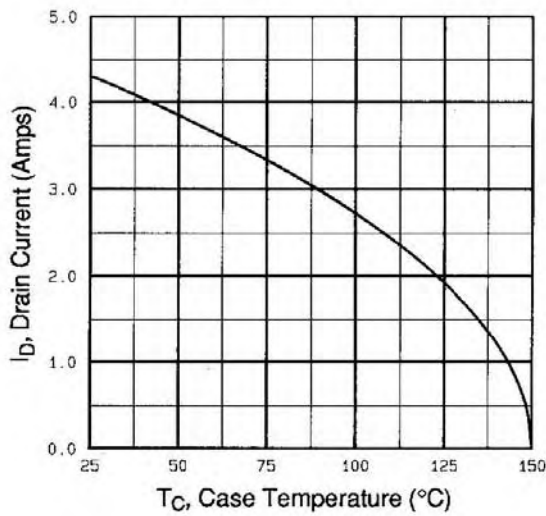
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



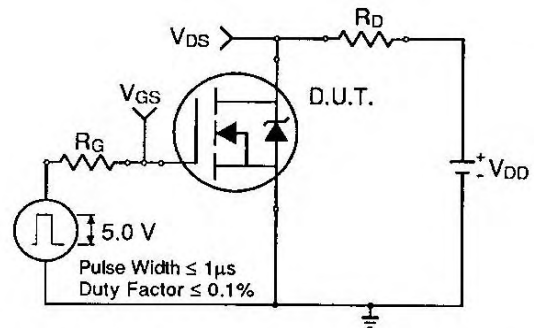
**Fig 7.** Typical Source-Drain Diode Forward Voltage



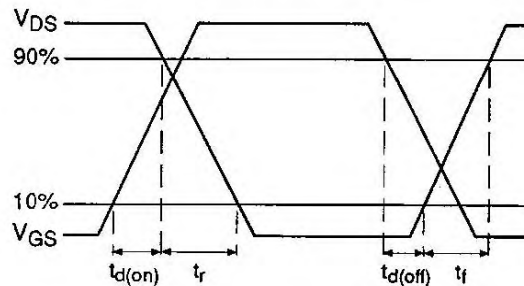
**Fig 8.** Maximum Safe Operating Area



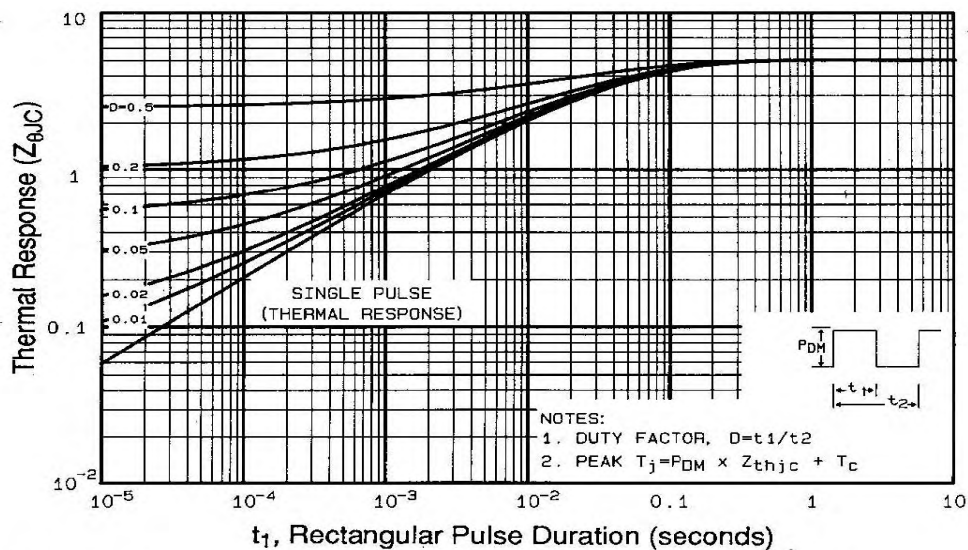
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



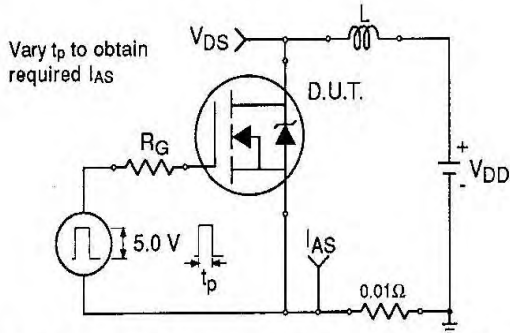
**Fig 10b.** Switching Time Waveforms



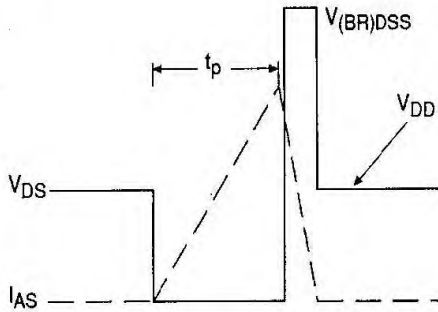
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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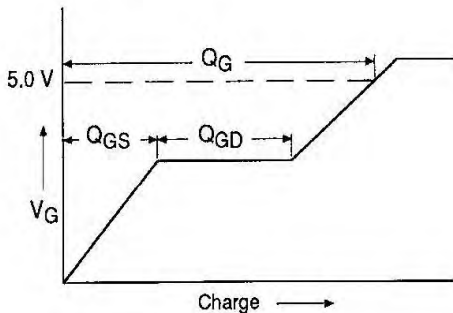
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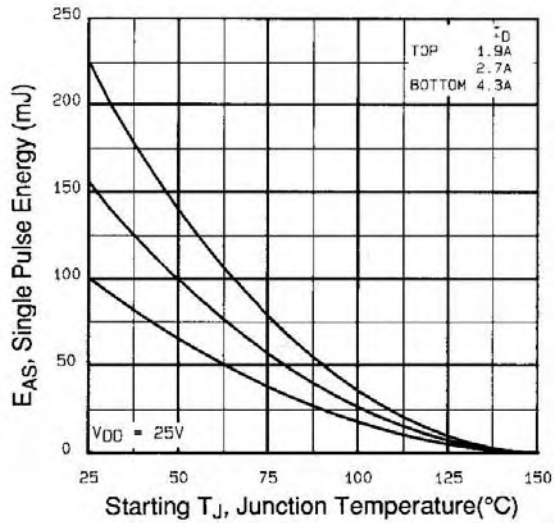
**Fig 12a.** Unclamped Inductive Test Circuit



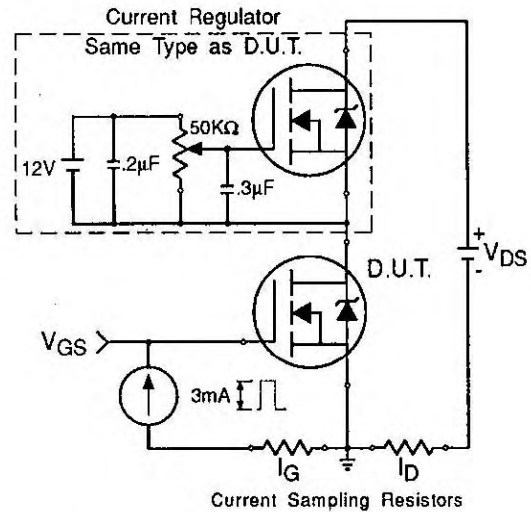
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

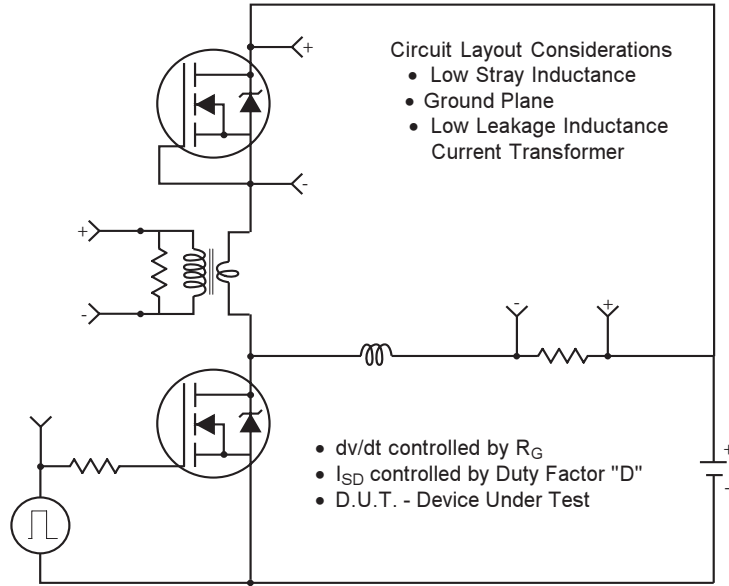


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

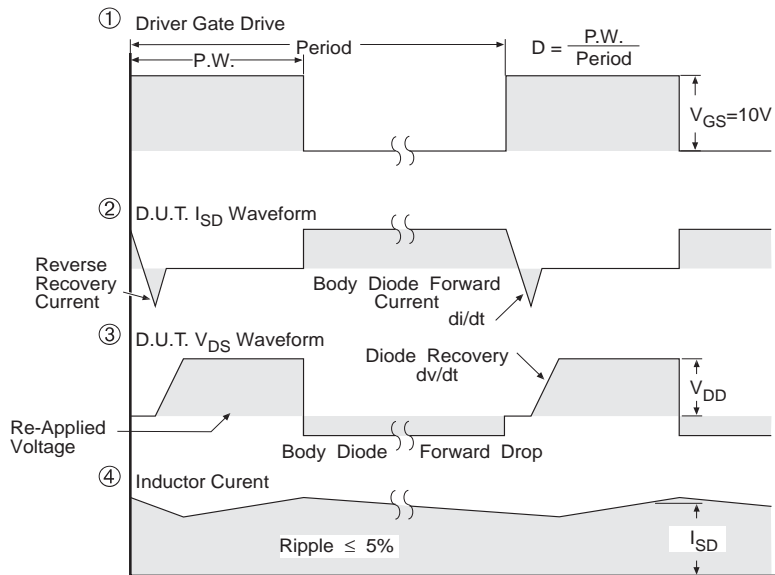


**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\* Reverse Polarity for P-Channel  
\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

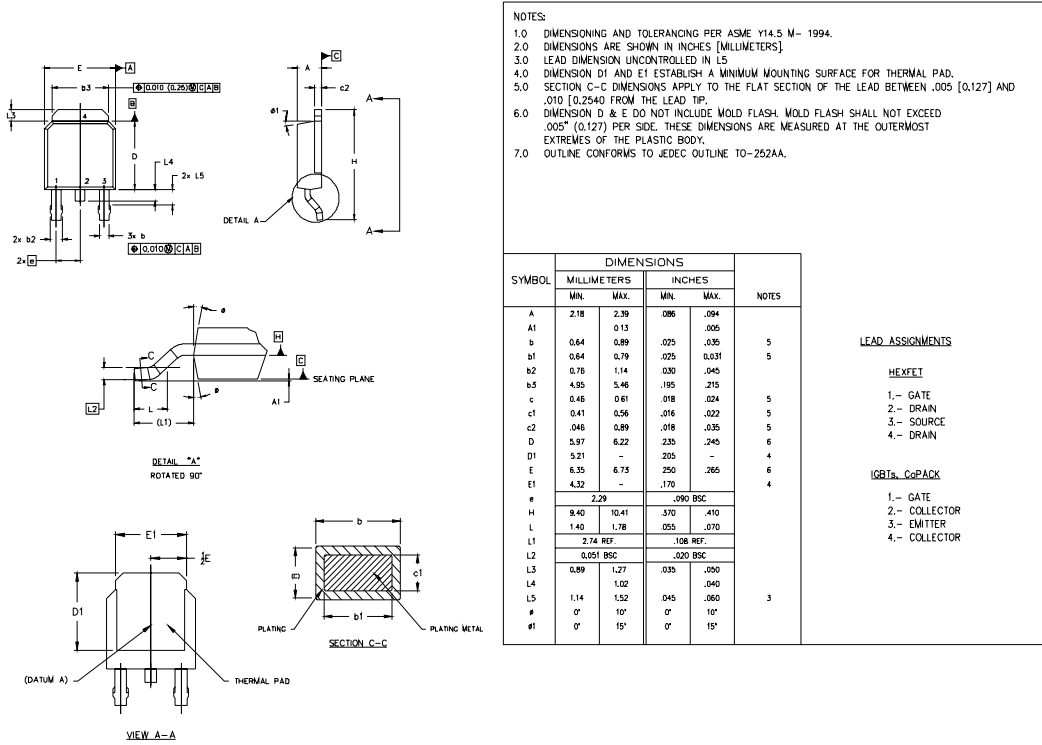
**Fig. 14 For N Channel HEXFETS**

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## D-Pak (TO-252AA) Package Outline

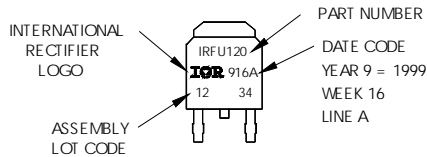
Dimensions are shown in millimeters (inches)



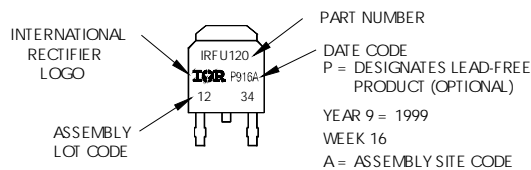
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON VWV16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



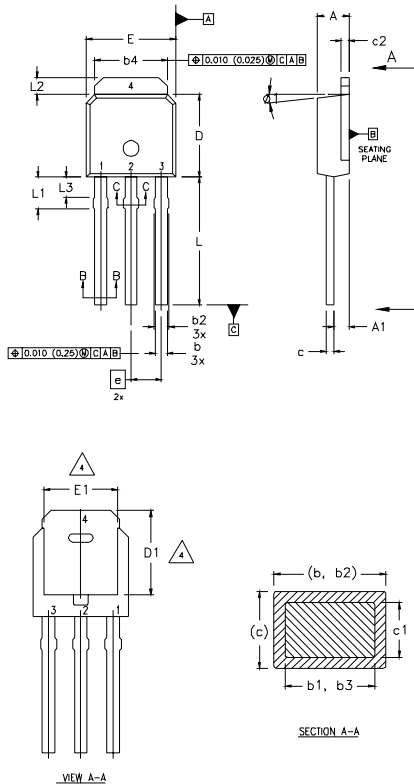
OR





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

**LEAD ASSIGNMENTS**

**HEXFET**

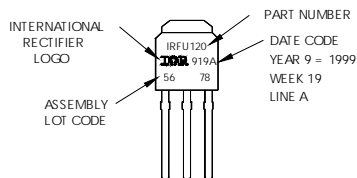
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15'	Ø	15'	

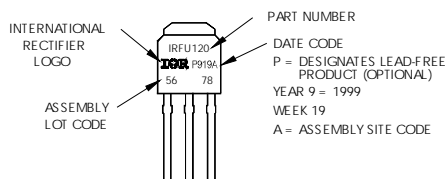
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"

**Note:** "P" in assembly line  
position indicates "Lead-Free"



**OR**

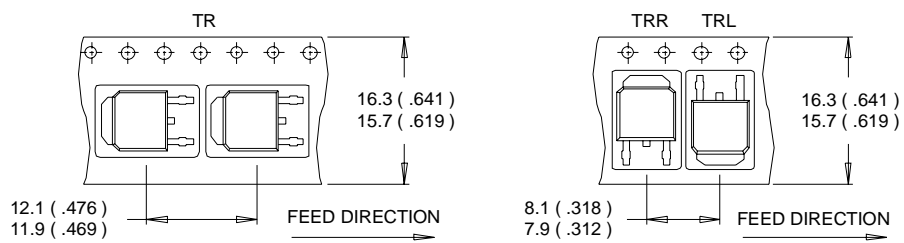


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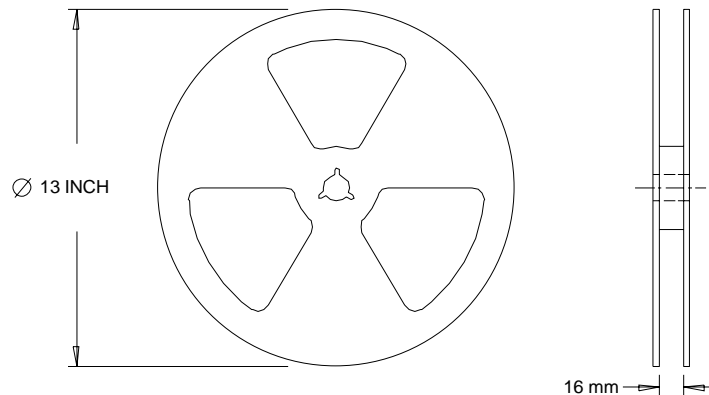
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

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TAC Fax: (310) 252-7903

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