VISHAY

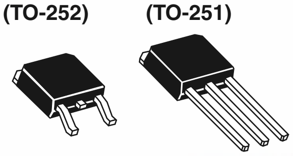
IRLR120, IRLU120, SiHLR120, SiHLU120

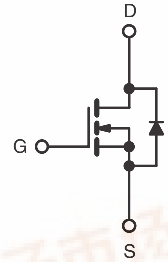
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 5.0 V	0.27
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.1	
Configuration	Single	

DPAK (TO-252) IPAK (TO-251)





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR120/SiHLR120)
- Straight Lead (IRLU120/SiHLU120)
- Available in Tape and Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS} = 4 V and 5 V
- Lead (Pb)-free Available

Pb Available

RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU/SiHLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRLR120PbF	IRLR120TRLPbF[a]	IRLR120TRPbF[a]	IRLR120TRRPbF[a]	IRLU120PbF
	SiHLR120-E3	SiHLR120TL-E3[a]	SiHLR120T-E3[a]	SiHLR120TR-E3[a]	SiHLU120-E3
SnPb	IRLR120	IRLR120TRL[a]	IRLR120TR[a]	-	-
	SiHLR120	SiHLR120TL[a]	SiHLR120T[a]	-	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5.0 V	T_C = 25 °C	I_D	7.7	A
		T_C = 100 °C		4.9	
Pulsed Drain Current[a]			I_{DM}	31	
Linear Derating Factor				0.33	W/°C
Linear Derating Factor (PCB Mount)[e]				0.020	
Single Pulse Avalanche Energy[b]			E_{AS}	210	mJ
Repetitive Avalanche Current[a]			I_{AR}	7.7	A
Repetitive Avalanche Energy[a]			E_{AR}	4.2	mJ
Maximum Power Dissipation		T_C = 25 °C	P_D	42	W
Maximum Power Dissipation (PCB Mount)[e]		T_A = 25 °C		2.5	
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			260[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 25 V, starting T_J = 25 °C, L = 5.3 mH, R_G = 25 Ω, I_{AS} = 7.7 A (see fig. 12).

c. $I_{SD} \le 9.2$ A, dI/dt ≤ 110 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.

d. 1.6 mm from case.

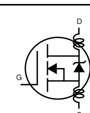
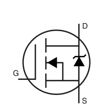
e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5.0 V	I_D = 4.6 A[b]	-	-	0.27	Ω
		V_{GS} = 4.0 V	I_D = 3.9 A[b]	-	-	0.38	
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 4.6 A[b]		4.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	490	-	pF
Output Capacitance	C_{oss}			-	150	-	
Reverse Transfer Capacitance	C_{rss}			-	30	-	
Total Gate Charge	Q_g	V_{GS} = 5.0 V	I_D = 9.2 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	12	nC
Gate-Source Charge	Q_{gs}			-	-	3.0	
Gate-Drain Charge	Q_{gd}			-	-	7.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 9.2 A, R_G = 9.0 Ω, R_D = 5.2 Ω, see fig. 10[b]		-	9.8	-	ns
Rise Time	t_r			-	64	-	
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	
Fall Time	t_f			-	27	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact[c] 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7.7	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	31	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 7.7 A, V_{GS} = 0 V[b]		-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 9.2 A, dI/dt = 100 A/µs[b]		-	110	140	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.80	1.0	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

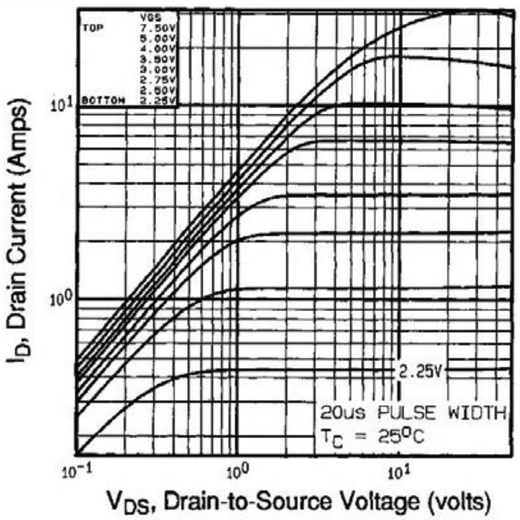


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

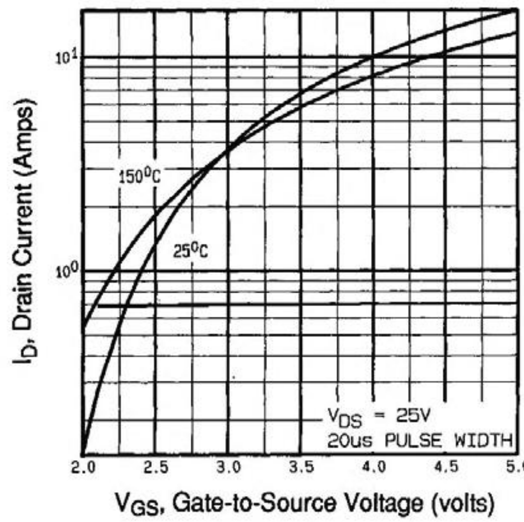


Fig. 3 - Typical Transfer Characteristics

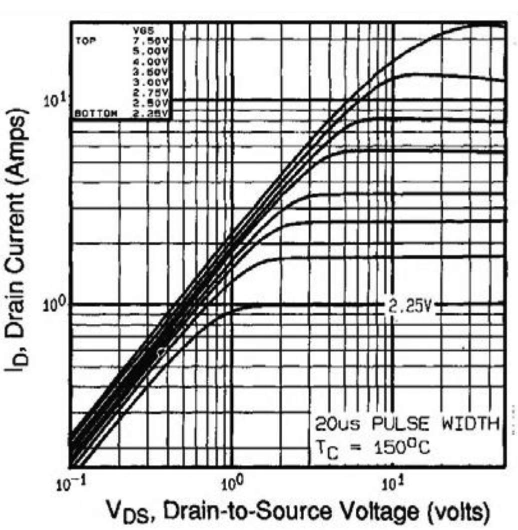


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

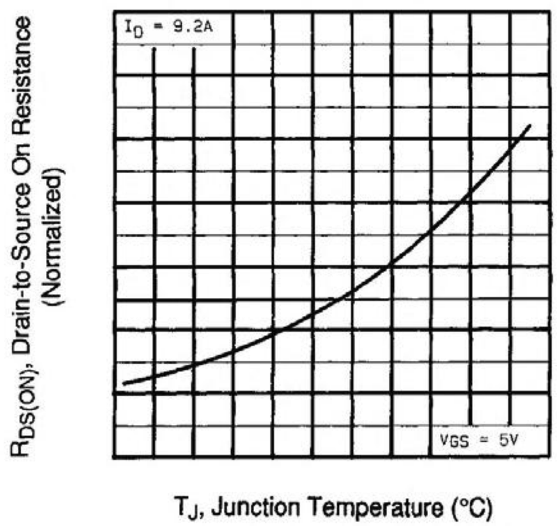


Fig. 4 - Normalized On-Resistance vs. Temperature

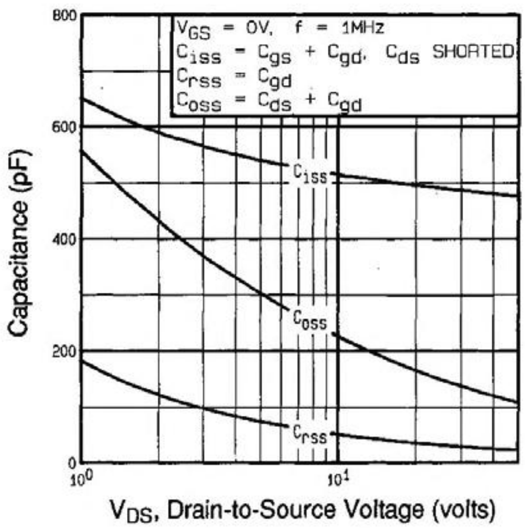


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

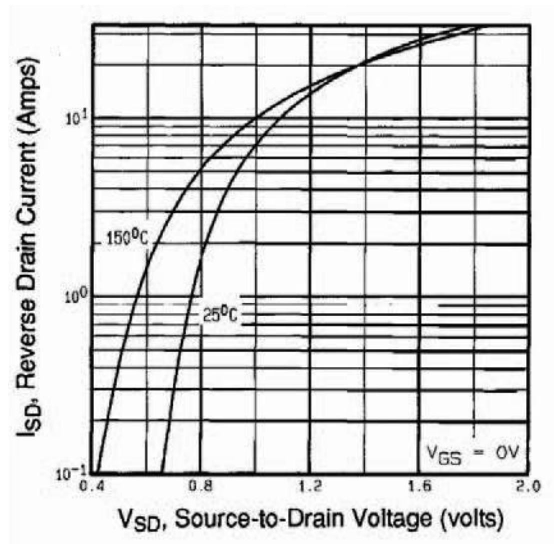


Fig. 7 - Typical Source-Drain Diode Forward Voltage

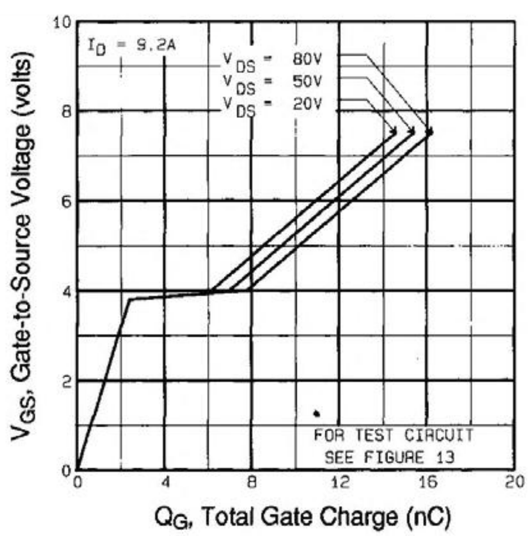


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

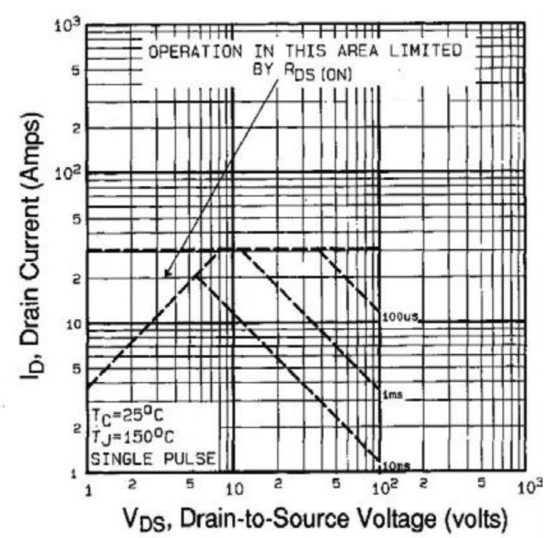


Fig. 8 - Maximum Safe Operating Area

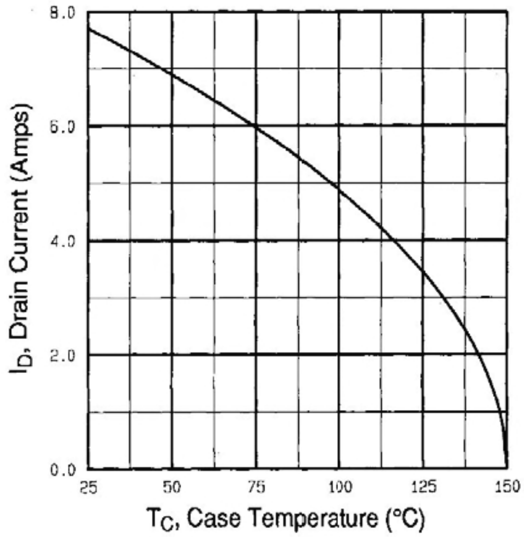


Fig. 9 - Maximum Drain Current vs. Case Temperature

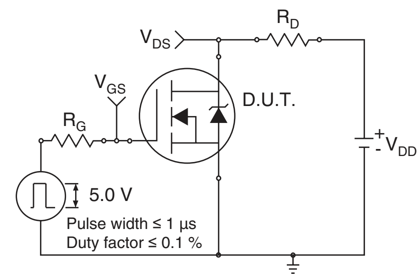


Fig. 10a - Switching Time Test Circuit

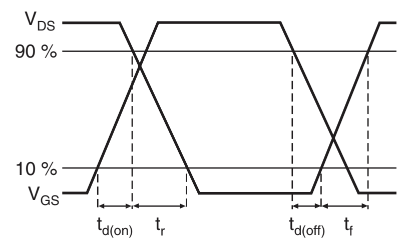


Fig. 10b - Switching Time Waveforms

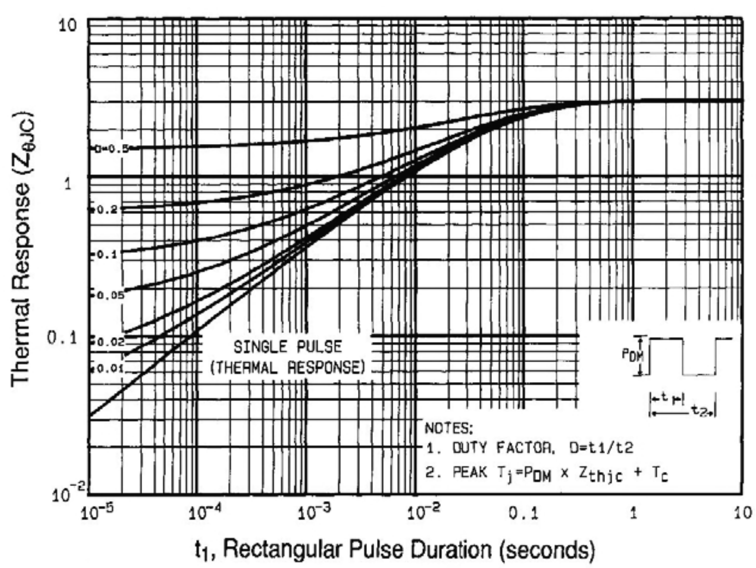


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

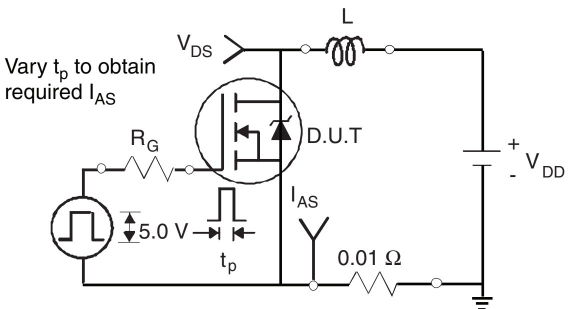


Fig. 12a - Unclamped Inductive Test Circuit

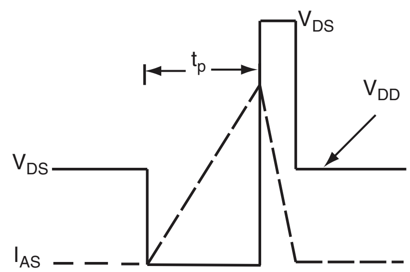


Fig. 12b - Unclamped Inductive Waveforms

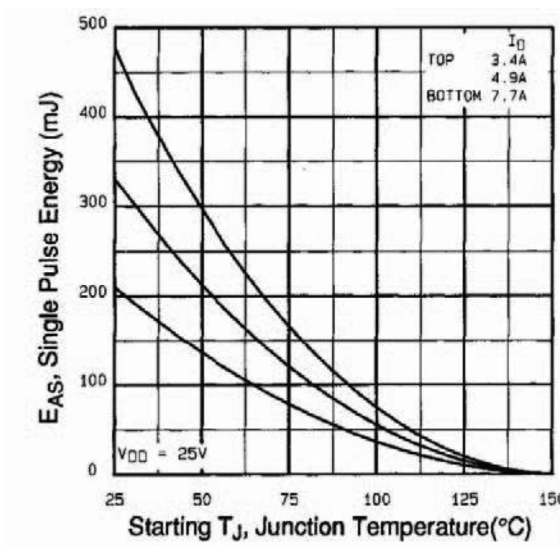


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

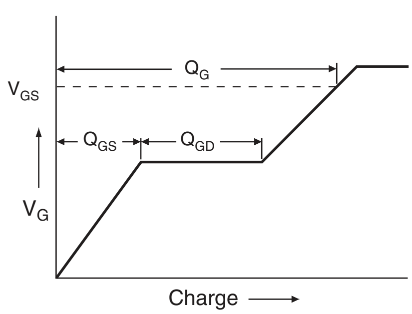


Fig. 13a - Basic Gate Charge Waveform

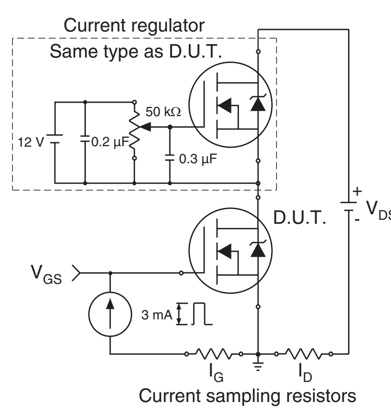
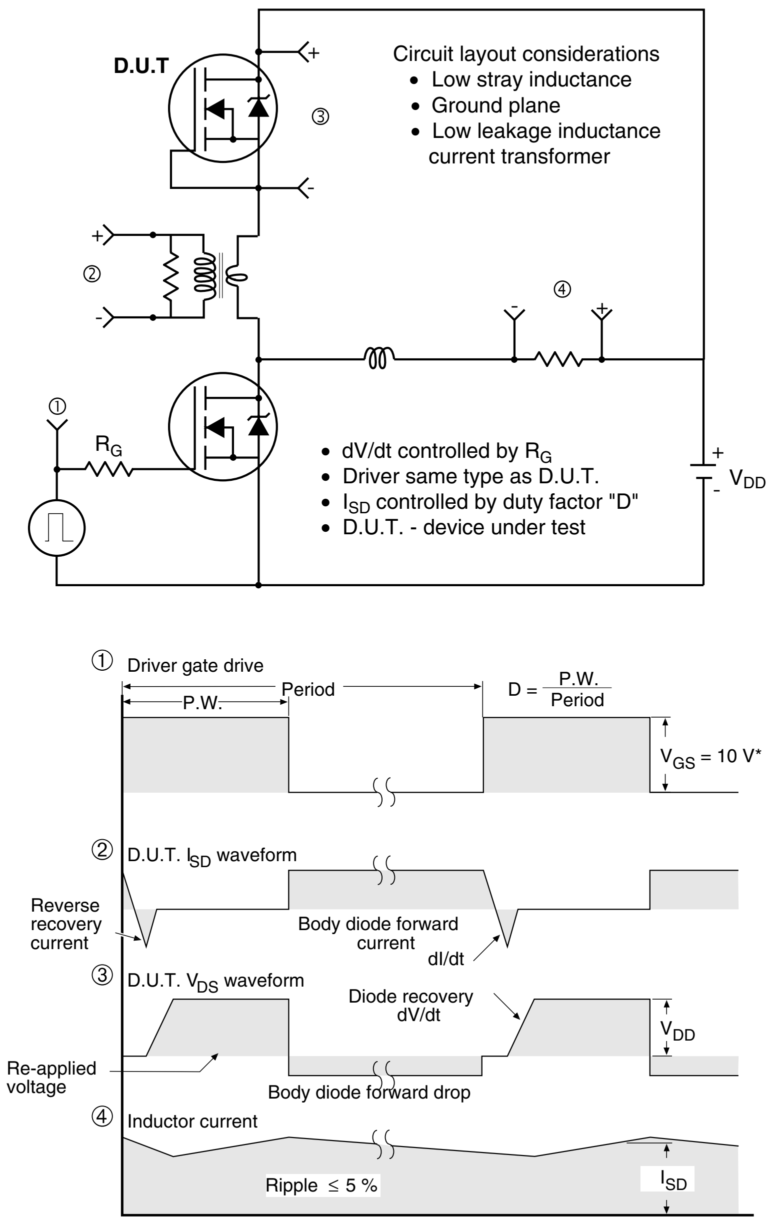


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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