Data Sheet No. PD60278

International
IOR Rectifier

IRS4426/IRS4427/IRS4428(S)PbF

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 V to 20 V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IRS4426)
- Outputs in phase with inputs (IRS4427)
- OutputA out of phase with inputA and outputB in phase with inputB (IRS4428)
- RoHS compliant

Descriptions

The IRS4426/IRS4427/IRS4428 are low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Product Summary

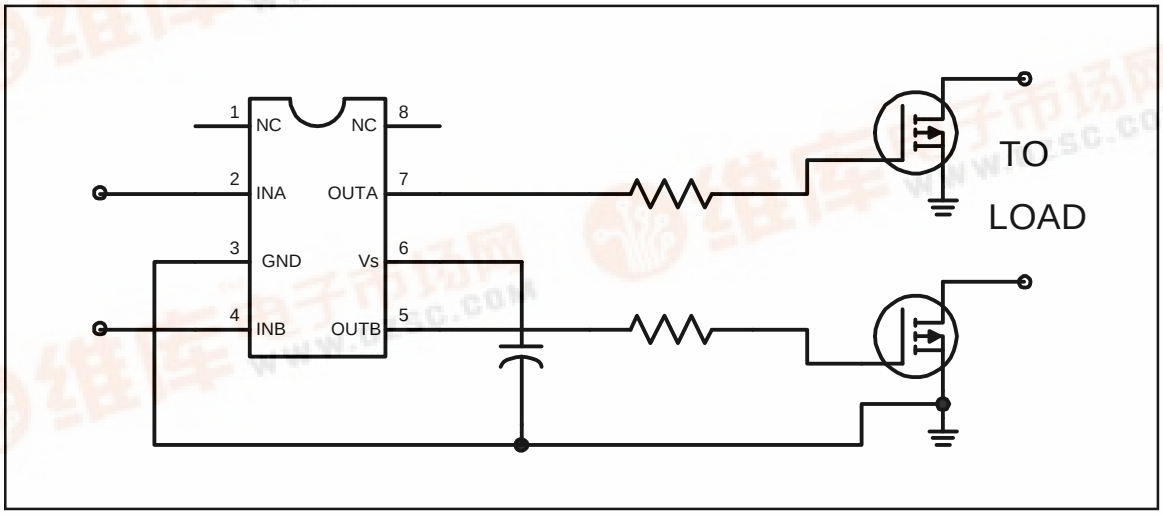
I_O+/-	1.5 A / 1.5 A
V_{OUT}	6 V - 20 V
$t_{on/off}$ (typ.)	50 ns & 50 ns

Packages

8 Lead PDIP

8-Lead SOIC

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	Fixed supply voltage		-0.3	20 (Note 1)	V
V_O	Output voltage		-0.3	V_S + 0.3	
V_{IN}	Logic input voltage		-0.3	V_S + 0.3	
P_D	Package power dissipation @ $T_A \leq +25$ °C	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15 V, T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” input voltage (OUTA=LO, OUTB=LO) (IRS4426) Logic “1” input voltage (OUTA=HI, OUTB=HI) (IRS4427) Logic “0” input voltage (OUTA=LO), Logic “1” input voltage (OUTB=HI) (IRS4428)	2.5	—	—	V	

DC Electrical Characteristics cont.

V_{BIAS} (V_S) = 15 V, T_A = 25 °C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

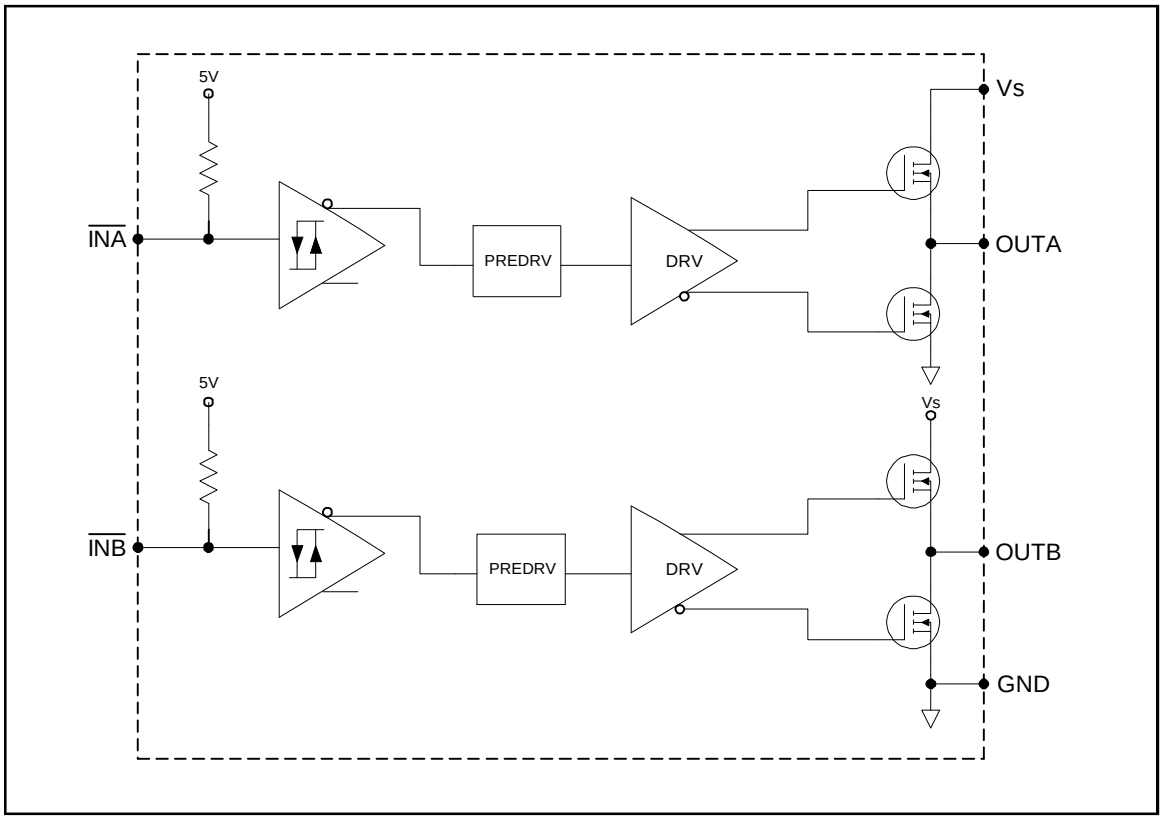
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IRS4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IRS4427) Logic "I" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IRS4428)	—	—	0.6	V	
V_{OH}	High level output voltage, V_{BIAS}-V_O	—	—	1.4		I_o = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.15		I_o = 20 mA
I_{IN+}	Logic "1" input bias current (OUT=HI)	—	5	15	µA	V_{IN} = 0 V (IRS4426) V_{IN} = V_S (IRS4427) V_{INA} = 0 V (IRS4428) V_{INB} = V_S (IRS4428)
I_{IN-}	Logic "0" input bias current (OUT=LO)	—	-10	-30		V_{IN} = V_S (IRS4426) V_{IN} = 0 V (IRS4427) V_{INA} = V_S (IRS4428) V_{INB} = 0 V (IRS4428)
I_{QS}	Quiescent V_S supply current	—	100	200		V_{IN} = 0 V or V_S
I_{O+}	Output high short circuit pulsed current	---	2.3	—	A	V_O = 0 V, V_{IN} = 0 V (IRS4426) V_O = 0 V, V_{IN} = V_S (IRS4427) V_O = 0 V, V_{INA} = 0 V (IRS4428) V_O = 0 V, V_{INB} = V_S (IRS4428) PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	---	3.3	—		V_O = 15 V, V_{IN} = V_S (IRS4426) V_O = 15 V, V_{IN} = 0 V (IRS4427) V_O = 15 V, V_{INA} = V_S (IRS4428) V_O = 15 V, V_{INB} = 0 V (IRS4428) PW ≤ 10 µs

AC Electrical Characteristics

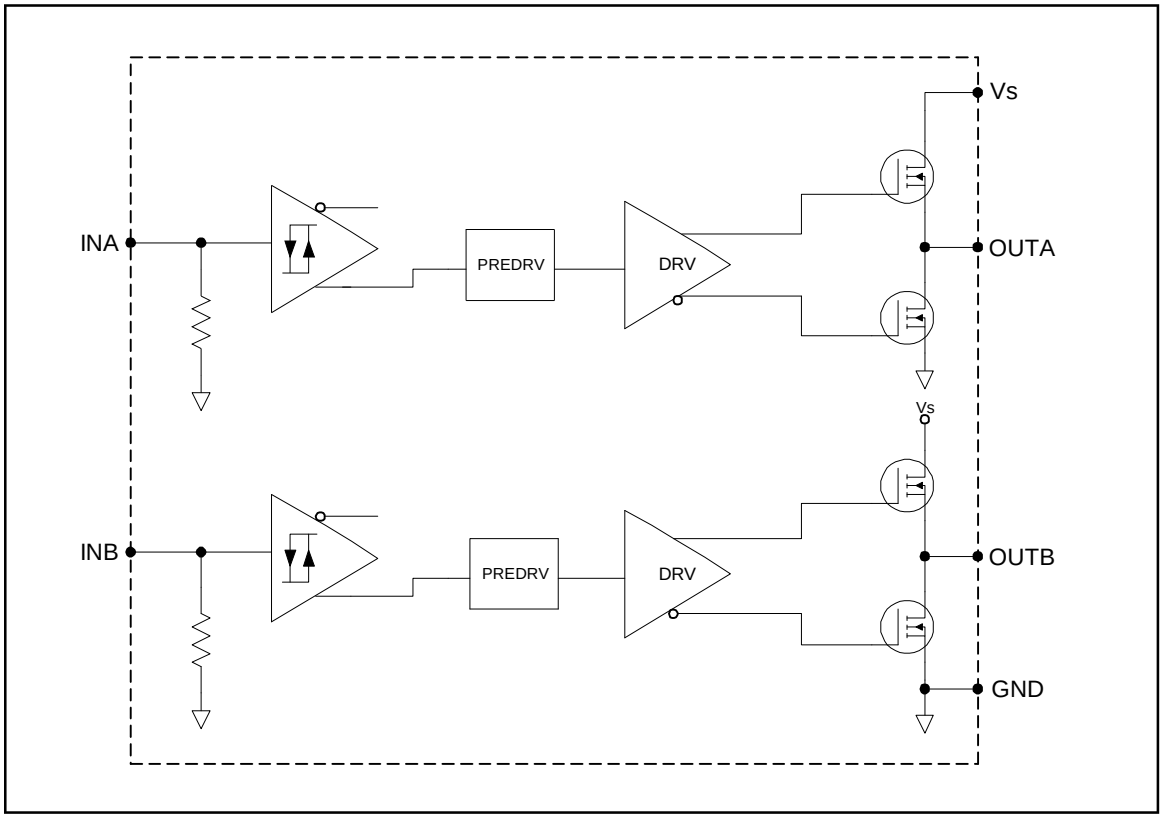
V_{BIAS} (V_S) = 15 V, CL = 1000 pF, T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	50	95	ns	Fig. 4
t_{d2}	Turn-off propagation delay	—	50	95		
t_r	Turn-on rise time	—	25	55		
t_f	Turn-off fall time	—	25	55		

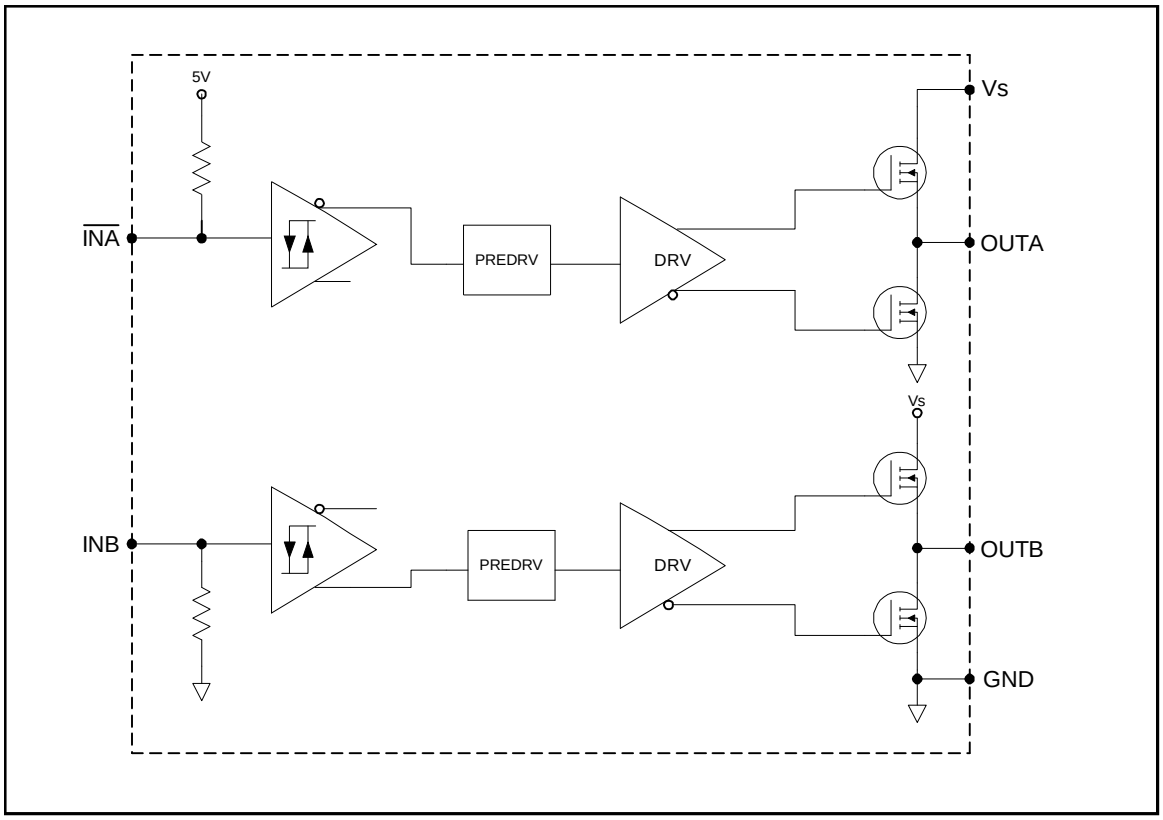
Functional Block Diagram IRS4426



Functional Block Diagram IRS4427



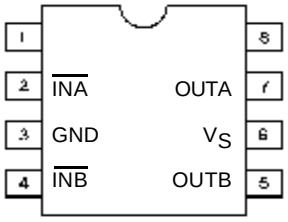
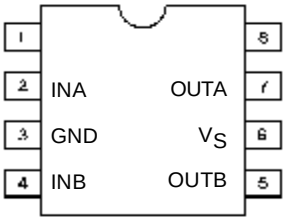
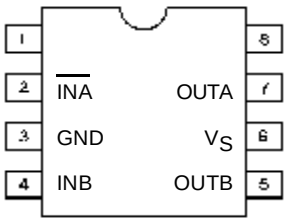
Functional Block Diagram IRS4428



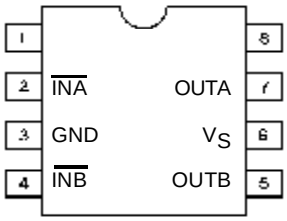
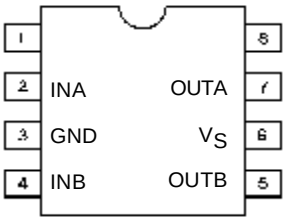
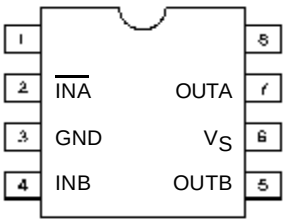
Lead Definitions

Symbol	Description
V_S	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IRS4426, IRS4428), in phase (IRS4427)
INB	Logic input for gate driver output (OUTB), out of phase (IRS4426), in phase (IRS4427, IRS4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

Lead Assignments

 8 Lead PDIP	 8 Lead PDIP	 8 Lead PDIP
IRS4426	**IRS4427**	**IRS4428**
Part Number		

Lead Assignments

 8 Lead SOIC	 8 Lead SOIC	 8 Lead SOIC
IRS4426S	**IRS4427S**	**IRS4428S**
Part Number		

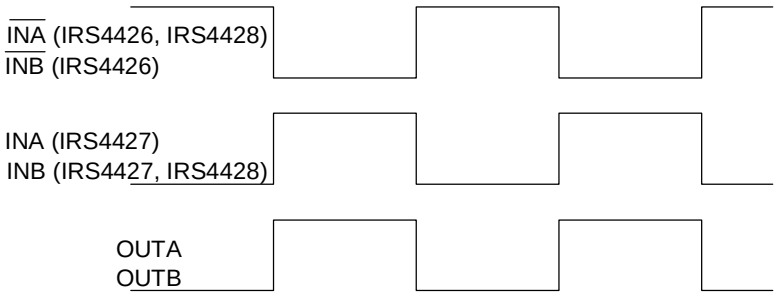


Figure 1. Timing Diagram

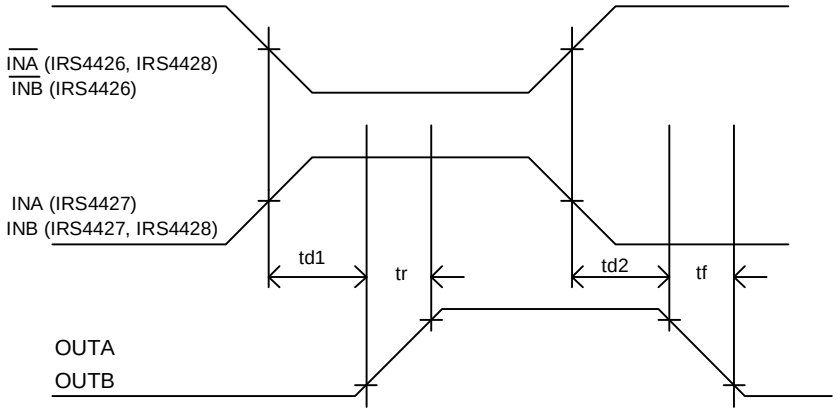


Figure 2. Switching Time Waveforms

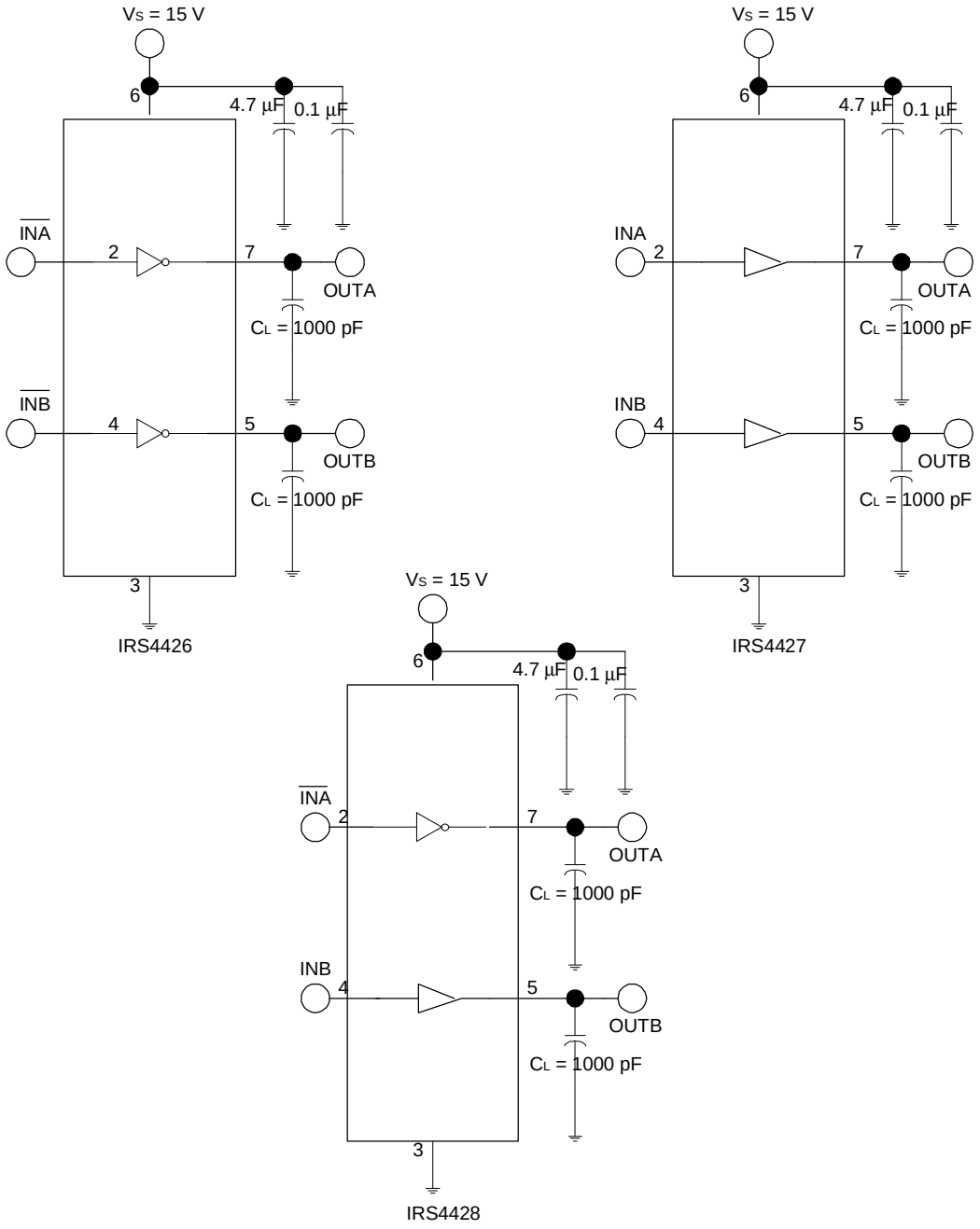


Figure 3. Switching Time Test Circuits

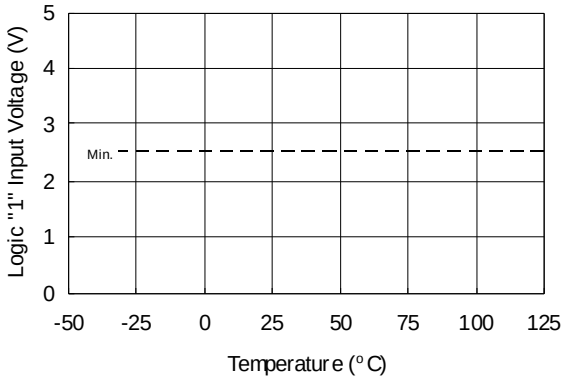


Figure 4A. Logic "1" Input Voltage vs. Temperature

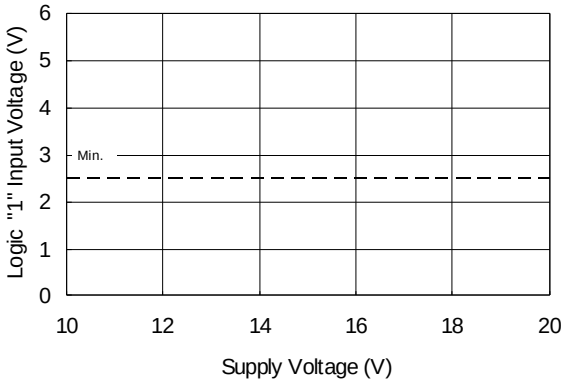


Figure 4B. Logic "1" Input Voltage vs. Supply Voltage

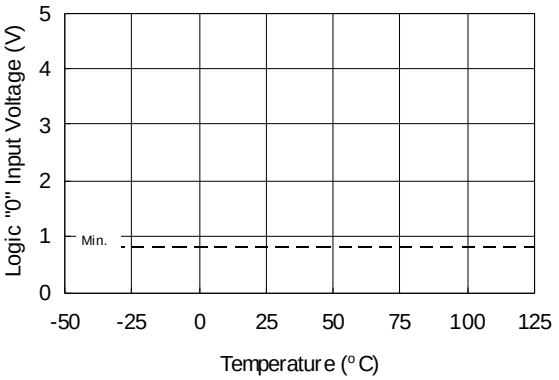


Figure 5A. Logic "0" Input Voltage vs. Temperature

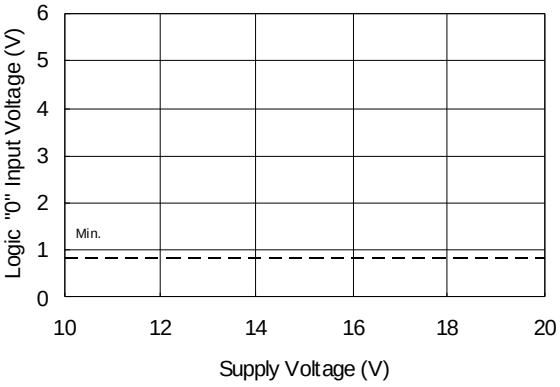


Figure 5B. Logic "0" Input Voltage vs. Supply Voltage

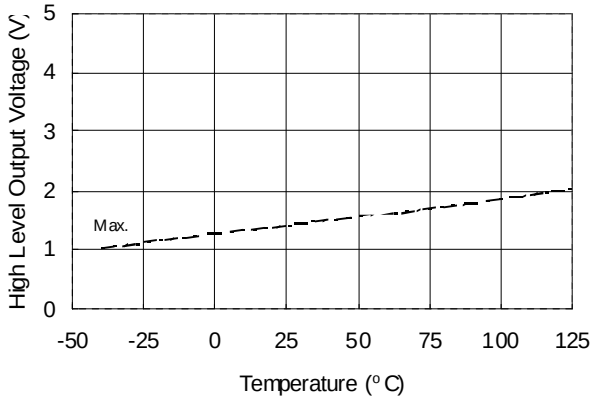


Figure 6A. High Level Output Voltage vs. Temperature (I_O = 0 mA)

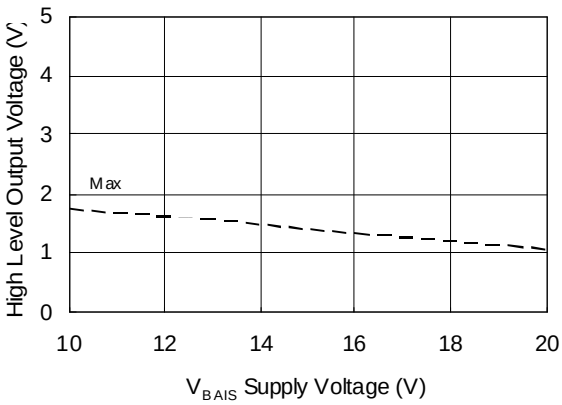


Figure 6B. High Level Output Voltage vs. Supply Voltage (I_O = 0 mA)

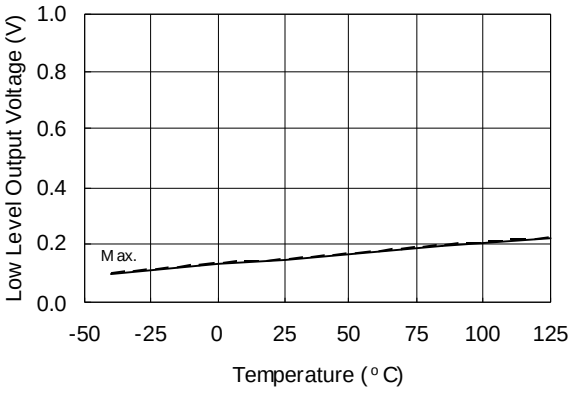


Figure 7A. Low Level Output Voltage vs. Temperature (I_O = 20 mA)

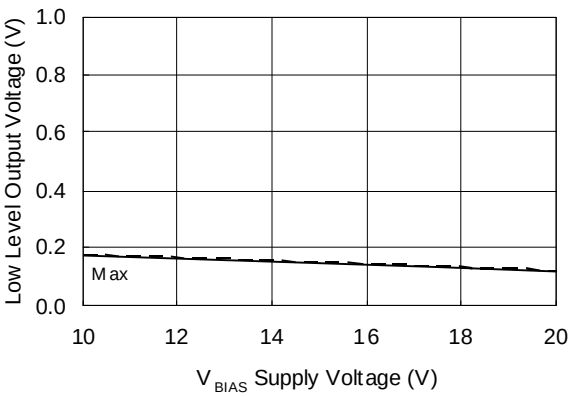


Figure 7B. Low Level Output vs. Supply Voltage (I_O = 20 mA)

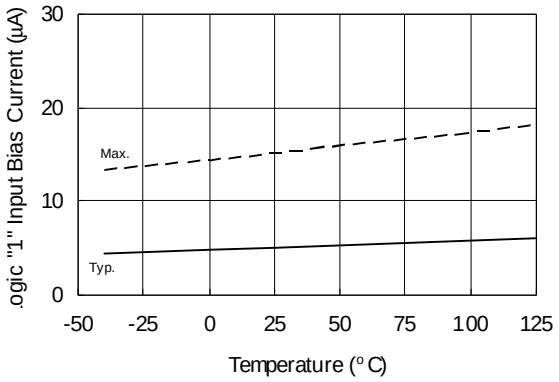


Figure 8A. Logic "1" Input Bias Current vs. Temperature

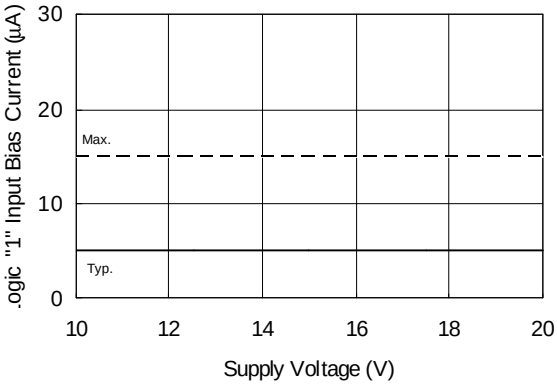


Figure 8B. Logic "1" Input Bias Current vs. Supply Voltage

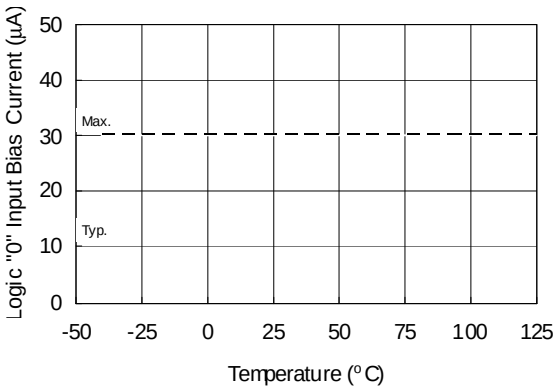


Figure 9A. Logic "0" Input Bias Current vs. Temperature

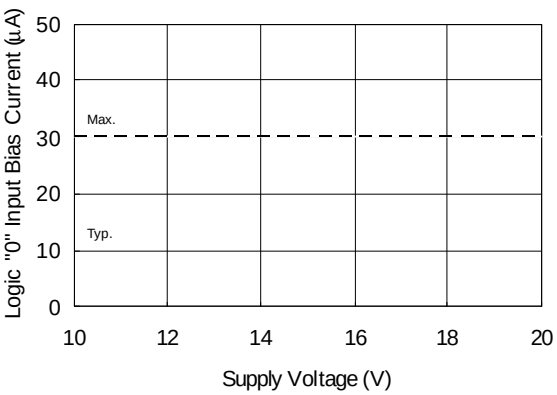


Figure 9B. Logic "0" Input Bias Current vs. Supply Voltage

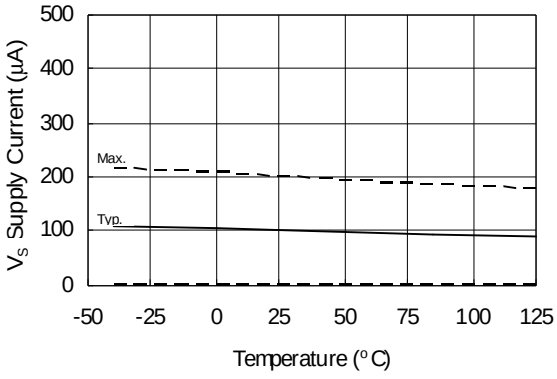


Figure 10A. V_S Supply Current vs. Temperature

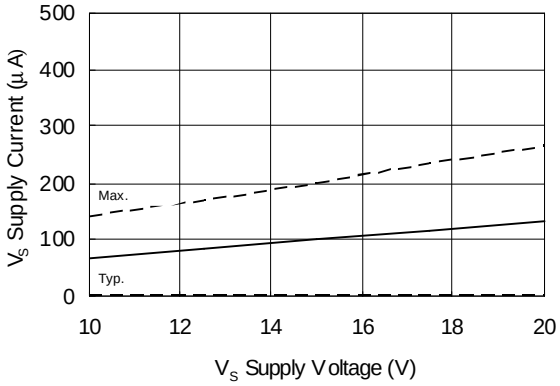


Figure 10B. V_S Supply Current vs. V_S Supply Voltage

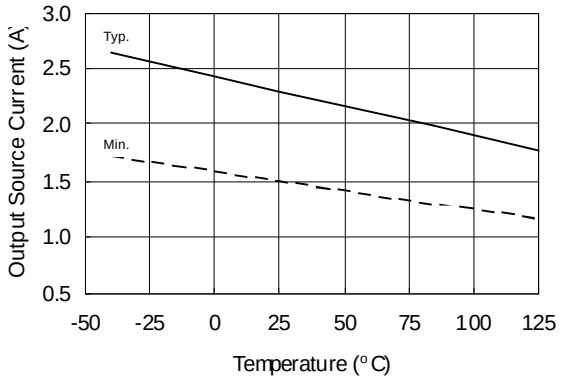


Figure 11A. Output Source Current vs. Temperature

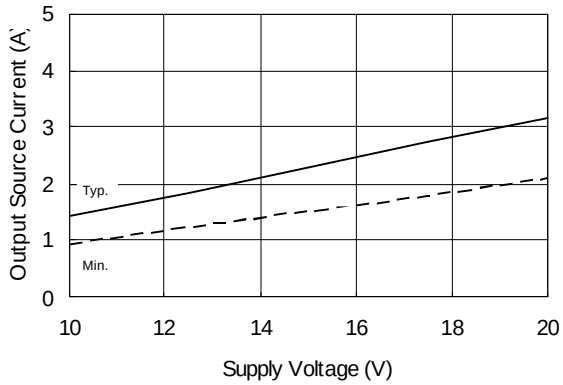


Figure 11B. Output Source Current vs. Supply Voltage

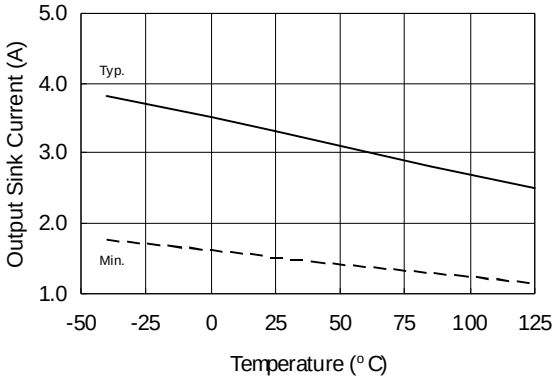


Figure 12A. Output Sink Current vs. Temperature

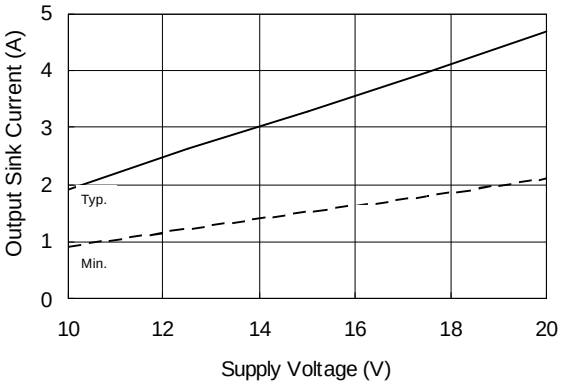


Figure 12B. Output Sink Current vs. Supply Voltage

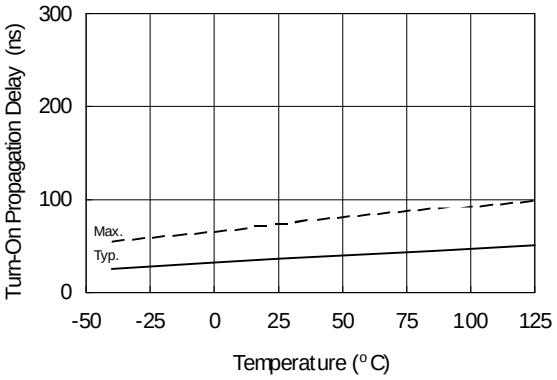


Figure 13A. Turn-On Propagation Delay vs. Temperature

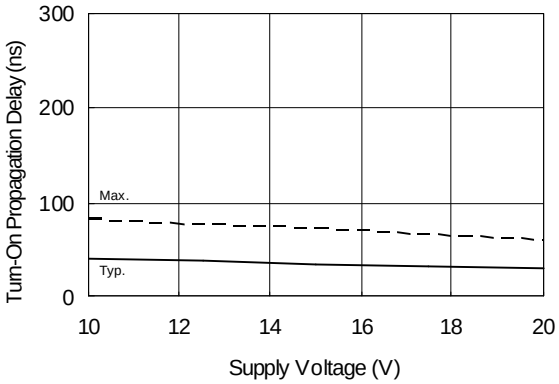


Figure 13B. Turn-On Propagation Delay vs. Supply Voltage

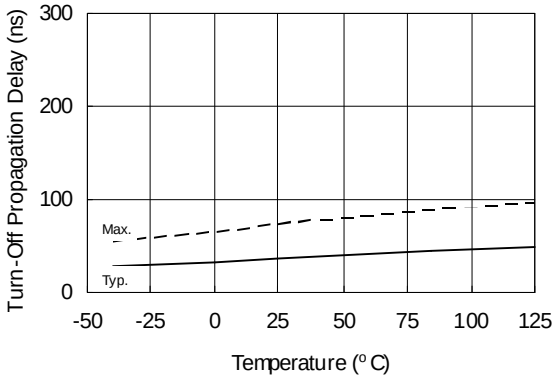


Figure 14A. Turn-Off Propagation Delay vs. Temperature

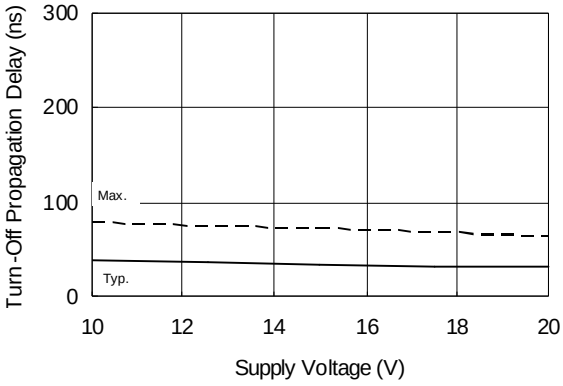


Figure 14B. Turn-Off Propagation Delay vs. Supply Voltage

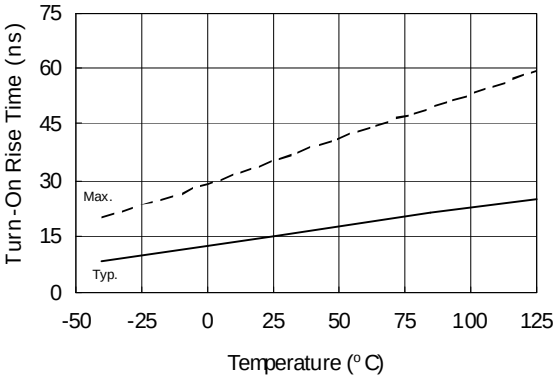


Figure 15A. Turn-On Rise Time vs. Temperature

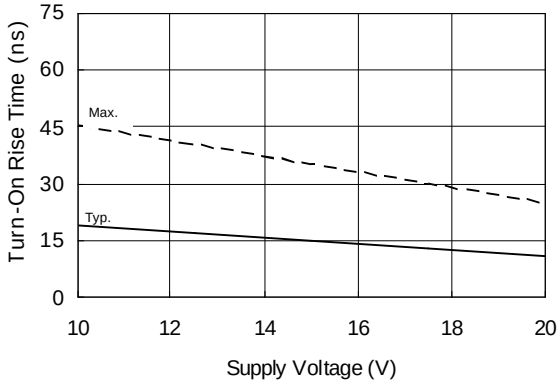


Figure 15B. Turn-On Rise Time vs. Supply Voltage

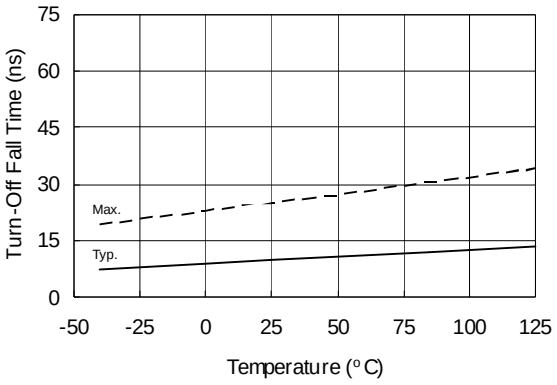


Figure 16A. Turn-Off Fall Time vs. Temperature

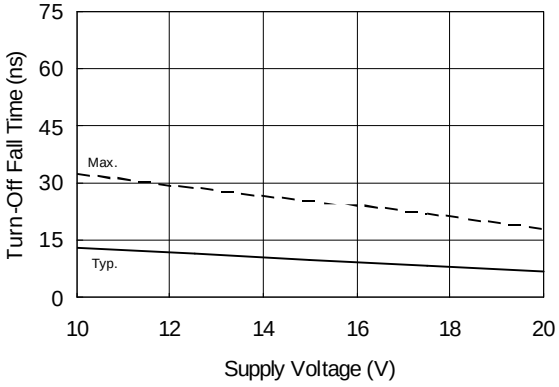
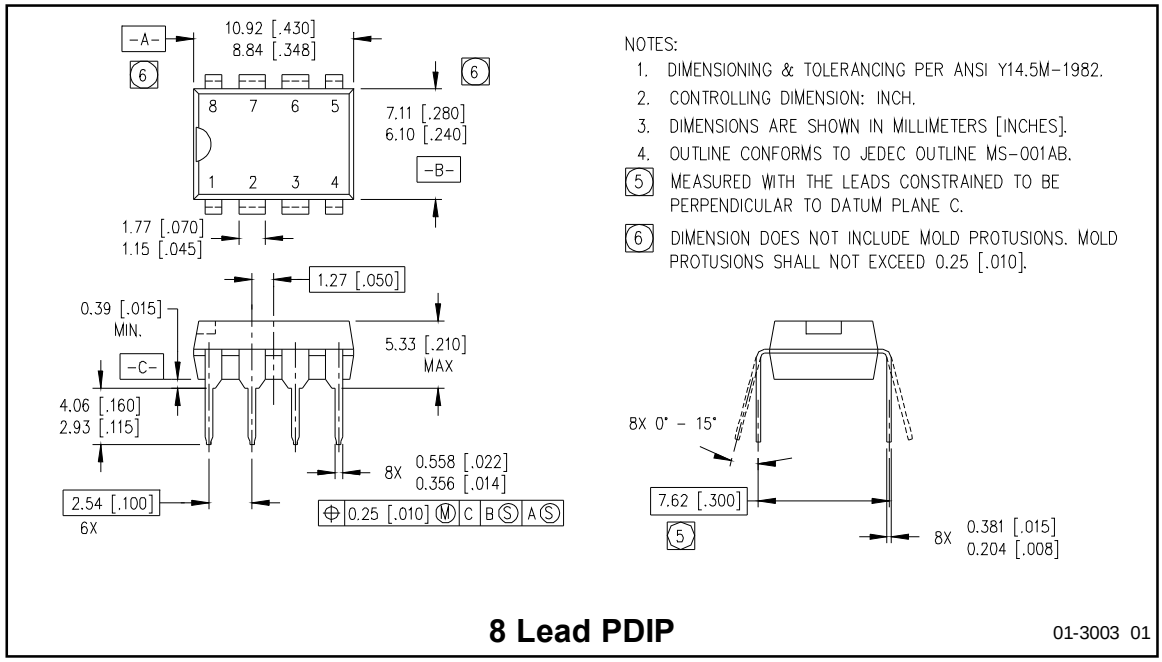


Figure 16B. Turn-Off Fall Time vs. Supply Voltage

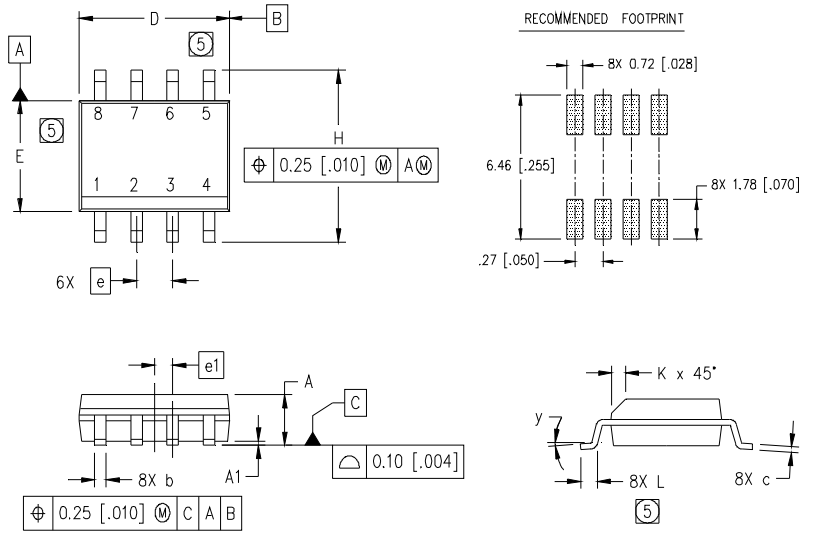
Caseoutline



8 Lead PDIP

01-3003 01

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

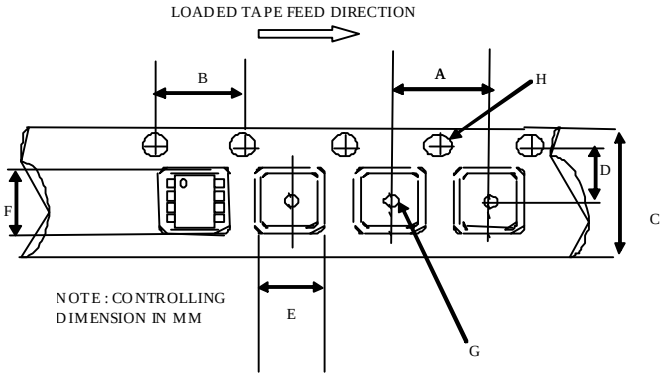
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

6 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

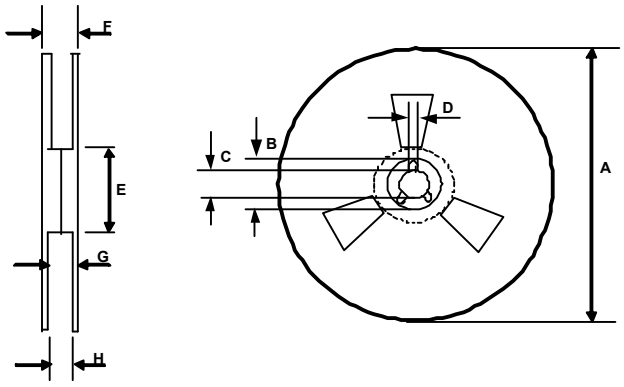
(MS-012AA) 01-0021 09

Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

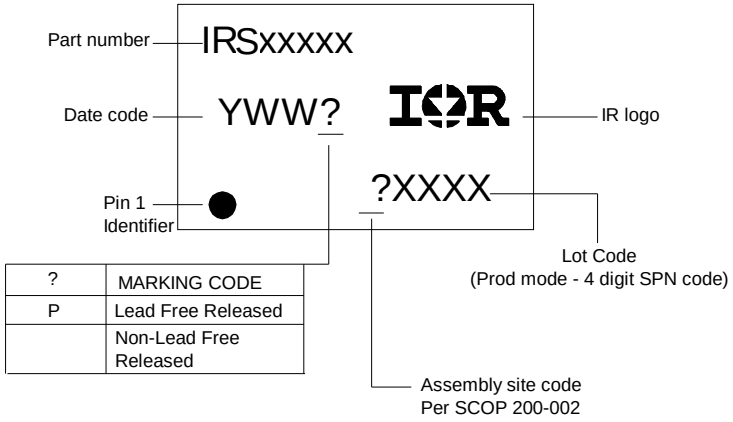
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

8-Lead PDIP IRS4426PbF
8-Lead SOIC IRS4426SPbF
8-Lead PDIP IRS4427PbF
8-Lead SOIC IRS4427SPbF
8-Lead PDIP IRS4428PbF
8-Lead SOIC IRS4428SPbF

The SOIC-8 is MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 11/20/2006