

International IOR Rectifier

Data Sheet No. PD60170-G

IR2137/IR2237(J)(Q)

Features

- Floating channel up to +600V or +1200V
- "soft" over-current shutdown turns off all six outputs
- Integrated high side desaturation circuit
- Controlled "soft" turn on for EMI reduction
- Integrated brake IGBT driver
- Three independent low side COM pins
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- 3.3V logic compatible
- Under voltage lockout with hysteresis band

Description

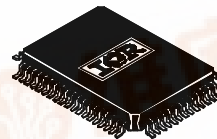
The IR2137/IR2237(J)(Q) are a high voltage, high speed 3-phase IGBT driver best suited for AC motor drive applications. Integrated desaturation logic provides ground fault protection as well as other mode of over current protection. Soft shutdown is initiated in the event of any overcurrent/ground fault conditions, and all six outputs are simultaneously turned off. Output drivers have separate turn on/off pins to facilitate independent gate drive impedance with EMI soft turn on. Optimum matched delays between phases, and between high/low side enables small deadtime, thus improving low speed performance. The brake driver eliminates additional circuits.

3-PHASE BRIDGE DRIVER

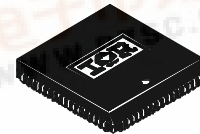
Product Summary

V _{OFFSET}	600V max. or 1200V max.
I _{O+/-}	220mA / 460mA
V _{OUT}	12.5V - 20V
Brake I _{O+/-}	40mA/80mA
Matched delay	75nsec
Deadtime (typ.)	300 nsec
DESAT Blanking time (typ.)	2.0usec
DESAT input voltage threshold (typ.)	V _{t+} = 5.0V

Packages

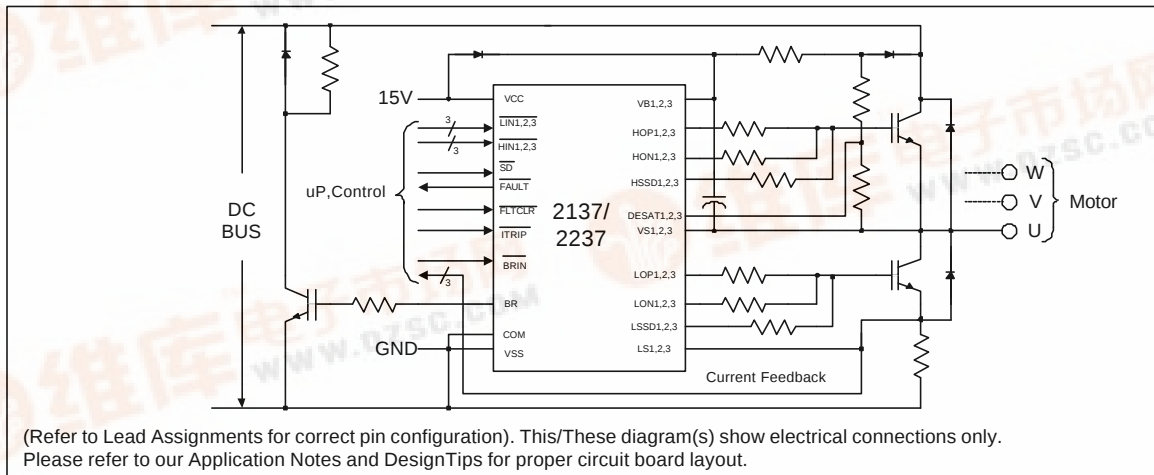


64-Lead MQFP



68-Lead PLCC

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _{S1,2,3}	High side offset voltage	V _{B1,2,3} - 25	V _{B1,2,3} + 0.3	V
V _{B1,2,3}	High side floating supply voltage (IR2137)	-0.3	625	
	(IR2237)	-0.3	1225	
V _{HO}	High side floating output voltage (HOP, HON, HSSD)	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3	
V _{CC}	Low side and logic fixed supply voltage	-0.3	25	
V _{SS}	Logic ground	V _{CC} - 25	V _{CC} + 0.3	
V _{LO1,2,3}	Low side output voltage (LOP, LON, LSSD)	V _{LS1,2,3} - 0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN, SD, ITRIP, FLTCLR, BRIN)	V _{SS} - 0.3	(V _{SS} + 15) or (V _{CC} + 0.3) which ever is lower	
V _{FLT}	FAULT output voltage	V _{SS} - 0.3	V _{CC} + 0.3	
V _{DESAT}	DESAT input voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3	
V _{BR}	BRAKE output voltage	- 0.3	V _{CC} + 0.3	V/ins
V _{LS1,2,3}	Low side output return voltage	V _{CC} - 25	V _{CC} + 0.3	
dV/dt	Allowable offset supply voltage slew rate	—	50	W
P _D	Package power dissipation @ T _A ≤ +25°C (MQFP64)	—	2.0	
	(PLCC68)	—	3.0	°C/W
R _{thJA}	Thermal resistance, junction to ambient (MQFP64)	—	60	
	(PLCC68)	—	40	°C
T _J	Junction temperature	—	150	
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _{B1,2,3}	High side floating supply voltage	V _{S1,2,3} + 13	V _{S1,2,3} + 20	V
V _{S1,2,3}	High side floating supply offset voltage (IR2137)	Note 1	600	
	(IR2237)	Note 1	1200	
V _{HO1,2,3}	High side output voltage (HOP, HON, HSSD)	V _{S1,2,3}	V _{S1,2,3} + 20	
V _{LO1,2,3}	Low side output voltage (LOP, LON, LSSD)	V _{LS1,2,3}	V _{CC}	
V _{CC}	Low side and logic fixed supply voltage	12.5	20	
V _{SS}	Logic ground	-5	+5	
V _{IN}	Logic input voltage (HIN, LIN, SD, ITRIP, FLTCLR, BRIN)	V _{SS}	V _{SS} + 5	
V _{BR}	BRAKE output voltage	0	V _{CC}	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	V
$V_{LS1,2,3}$	Low side output return voltage	-5.0	+5.0	
V_{DESAT}	DESAT pin input voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V/+1200V. Logic state held for V_S of COM -5V to -COM V_{BS} .

Note 2: All input pins are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to $V_{LS1,2,3}$ and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.3	11.4	12.5	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{CCUVH}	V_{CC} supply undervoltage lockout hysteresis	—	1.0	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.3	11.4	12.5		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	—	1.0	—		
I_{LK}	Offset supply leakage current (IR2137)	—	—	50	μA	$V_{B1,2,3} = V_{S1,2,3} = 600V$
	(IR2237)	—	—	50		$V_{B1,2,3} = V_{S1,2,3} = 1200V$
I_{QBS}	Quiescent V_{BS} supply current	—	120	200	V	$V_{CC} = 12.5$ to $20V$
I_{QCC}	Quiescent V_{CC} supply current	—	2	6		
V_{IH}	Logic "0" input voltage (OUT=LO) ($\overline{HIN}$, $\overline{LIN}$, $\overline{ITRIP}$, $\overline{SD}$, $\overline{BRIN}$, $\overline{FLTCLR}$)	3.15	—	—		
V_{IL}	Logic "1" input voltage (OUT=HI) ($\overline{HIN}$, $\overline{LIN}$, $\overline{ITRIP}$, $\overline{SD}$, $\overline{BRIN}$, $\overline{FLTCLR}$)	—	—	0.8		
V_{t+}	Logic input positive going threshold ($\overline{HIN}$, $\overline{LIN}$, $\overline{ITRIP}$, $\overline{SD}$, $\overline{BRIN}$, $\overline{FLTCLR}$)	1.6	2.5	3.1		
V_{t-}	Logic input negative going threshold ($\overline{HIN}$, $\overline{LIN}$, $\overline{ITRIP}$, $\overline{SD}$, $\overline{BRIN}$, $\overline{FLTCLR}$)	0.9	1.5	2.4		
V_T	Logic input hysteresis ($\overline{HIN}$, $\overline{LIN}$, $\overline{ITRIP}$, $\overline{SD}$, $\overline{BRIN}$, $\overline{FLTCLR}$)	0.7	1.0	—		

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Static Electrical Characteristics - cont.

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to $V_{LS1,2,3}$ and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{OH}	High level output voltage, $V_{BIAS} - V_O$ (normal switching) HOP, LOP	—	—	100	mV	$I_O = 1\text{ mA}$
V_{OL}	Low level output voltage, V_O (normal switching) HON, LON	—	—	100		
I_{IN+}	Logic "1" input bias current	—	150	—	μA	$V_{IN} = 0\text{V}$
I_{IN-}	Logic "0" input bias current	—	80	—		$V_{IN} = 5\text{V}$
I_{DESAT+}	"high" DESAT input bias current	—	—	15		$V_{DESAT} = 15\text{V}$
I_{DESAT-}	"low" DESAT input bias current	—	—	.1		$V_{DESAT} = 0\text{V}$
I_{O+}	Output high short circuit pulsed current	220	300	—	mA	$V_O = 0\text{V}$, $V_{IN} = 0\text{V}$ $PW \leq 10\text{ }\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	460	550	—		$V_O = 15\text{V}$, $V_{IN} = 5\text{V}$ $PW \leq 10\text{ }\mu\text{s}$
I_{OBR+}	BR output high short circuit pulsed current	40	75	—		$V_{BR}=0\text{V}$, $V_{BRIN}=0\text{V}$ $PW \leq 10\text{ }\mu\text{s}$
I_{OBR-}	BR output low short circuit pulsed current	80	120	—		$V_{BR}=15\text{V}$, $V_{BRIN}=5\text{V}$ $PW \leq 10\text{ }\mu\text{s}$
V_{OHB}	BR high level output voltage, $V_{BIAS}-V_{BR}$	—	—	300	mV	$I_{BR} = 1\text{mA}$
V_{OLB}	BR low level output voltage, V_{BR}	—	—	150		
$R_{ON,SS}$	Soft shutdown on resistance	—	500	—	Ω	$I_{TRIP} = 0\text{V}$
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		
V_{DESAT+}	High DESAT input threshold voltage	—	5.2	—	V	

AC Electrical Characteristics

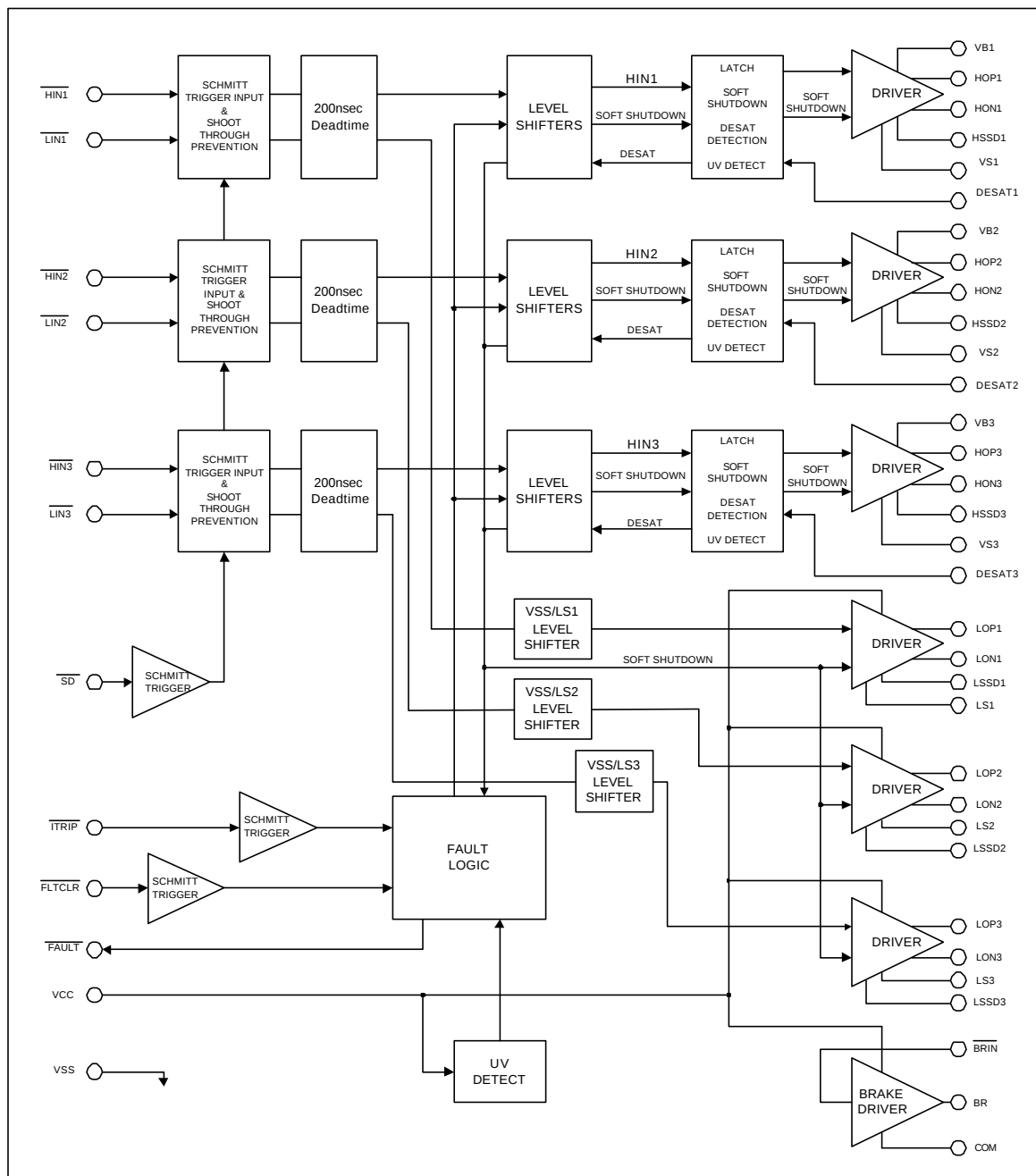
$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $V_{S1,2,3} = V_{SS}$, $T_A = 25^\circ C$ and $C_L = 1000$ pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions											
Propagation Delay Characteristics																	
t _{on}	Turn-on propagation delay	150	400	600	ns	V _{IN} = 0 & 5V V _{S1,2,3} = 0 to 600V or 1200V HOP=HON,LOP=LON Figure 4											
t _{off}	Turn-off propagation delay	150	400	600		V _{IN} ,V _{DESAT} =0 V _{SD} = 5V											
t _r	Turn-on rise time	—	115	—			V _{IN} ,V _{DESAT} = 0 V _{ITRIP} = 5V, fig. 7										
t _f	Turn-off fall time	—	25	—				V _{S1,2,3} = 0 to 600V or 1200V V _{HIN} = 0V, V _{SD} , V _{ITRIP} = 5V, V _{DESAT} = 15V, fig. 5									
t _{ITRIP}	ITRIP to output shutdown propagation delay	—	1000	1400					V _{IN} ,V _{ITRIP} =0V, V _{SD} = 5V, V _{DESAT} = 0V, fig. 7								
t _{SD}	SD to output shutdown propagation delay	—	1200	1500						V _{SD} = 5V, V _{DESAT} = 0V, fig. 7							
t _{DESAT1}	DESAT to output shutdown propagation delay at HOPx turn-on	1400	2800	4200							V _{S1,2,3} = 0 to 600V or 1200V V _{IN} = 0V, V _{SD} , V _{ITRIP} = 5V, V _{DESAT} = 15V, Figure 5						
t _{DESAT2}	DESAT to output shutdown propagation delay after blanking	600	1150	1700								Figure 4					
t _{FLT, IT}	ITRIP to FAULT output delay	—	800	1100													
t _{FLTCLR}	FLTCLR to FAULT output delay	—	1100	1400													
t _{FLT,DESAT1}	DESAT to FAULT output delay propagation delay at HOPx turn-on	—	2500	—													
t _{FLT,DESAT2}	DESAT to FAULT output delay propagation delay after blanking	—	850	—													
t _{BL}	DESAT blanking time at turn-on	—	2000	—													
t _{onBR}	BR output turn-on propagation delay	—	120	200													
t _{offBR}	BR output turn-off propagation delay	—	85	150													
t _{rBR}	BR output turn-on rise time	—	300	—													
t _{fBR}	BR output turn-off fall time	—	150	—													
Deadtime/Delay Matching Characteristics																	
DT	Deadtime	—	300	—	ns	Figure 6											
MDT	Matching delay, max (t _{on} ,t _{off}) - min (t _{on} ,t _{off}), (t _{on} ,t _{off} are applicable to all six channels)	—	0	75		External dead time >400nsec											
PM	Output pulse width matching, IPW _{in} - PW _{outl} (exclude BR _{IN} /BR)	—	0	75		External dead time >400nsec, Fig. 4											

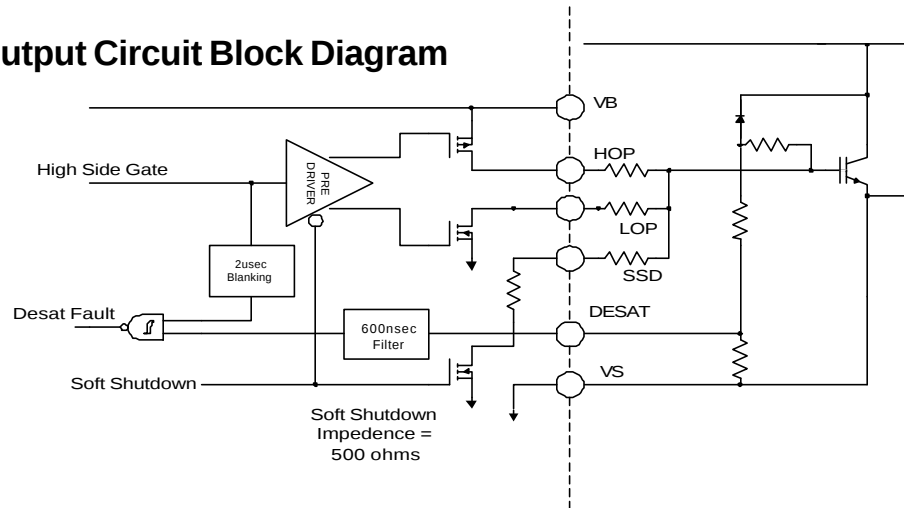
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Functional Block Diagram



Driver Output Circuit Block Diagram



Lead Definitions

Symbol	Description
V _{CC}	Low side and logic supply voltage
V _{SS}	Logic Ground
HIN1,2,3	Logic inputs for high side gate driver outputs (HOP1,2,3/HON1,2,3, out of phase)
LIN1,2,3	Logic inputs for low side gate driver outputs (LOP1,2,3/LON1,2,3, out of phase)
SD	Logic input for shutdown (hard shutdown, level sensitive signal, negative logic)
ITRIP	Logic input for overcurrent shutdown (soft shutdown, edge sensitive, negative signal)
FLTCLR	Logic input for FAULT clear (edge sensitive, negative signal)
BRIN	Logic input for brake driver, out of phase with BR
FAULT	Fault output indicates over current and desaturation shutdown (open drain)
BR	Brake driver output
COM	Brake driver return
VB1,2,3	High side gate drive floating supply
HOP1,2,3	High side driver pull up output
HON1,2,3	High side driver pull down output
HSSD1,2,3	High side soft shutdown output
DESAT1,2,3	IGBT desaturation protection input
VS1,2,3	High voltage floating supply return
LOP1,2,3	Low side driver pull up output
LON1,2,3	Low side driver pull down output
LSSD1,2,3	Low side soft shutdown output
LS1,2,3	Low side driver returns

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Lead Assignments

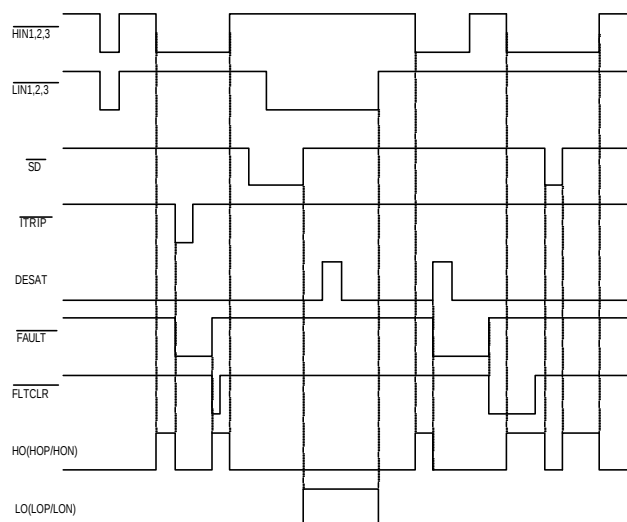
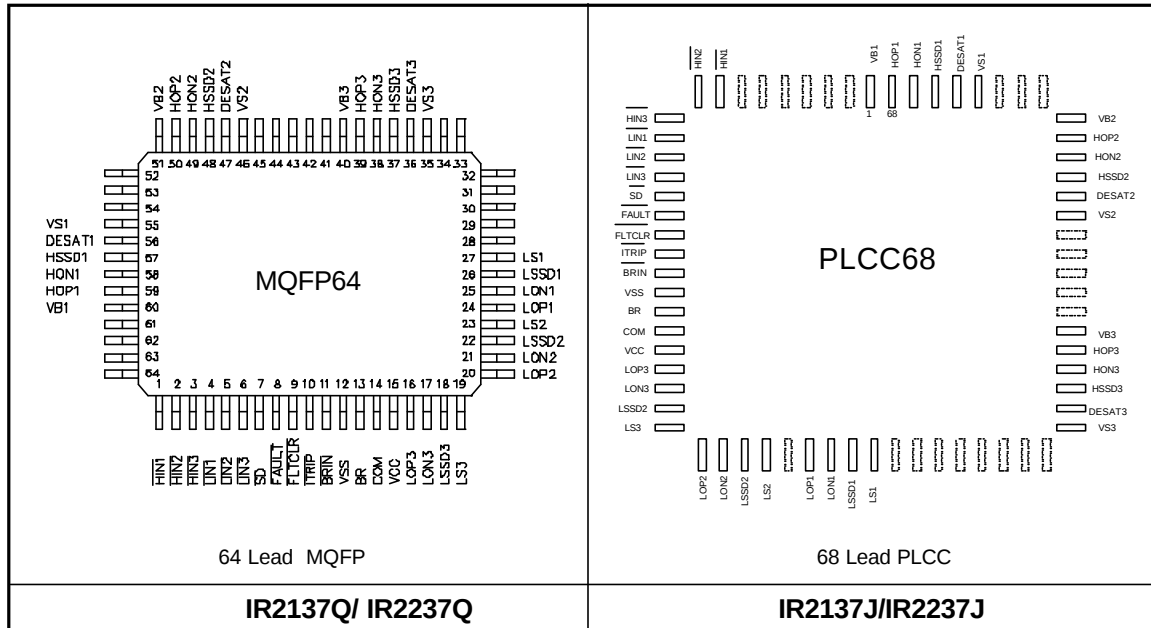


Figure 3. Timing Diagram



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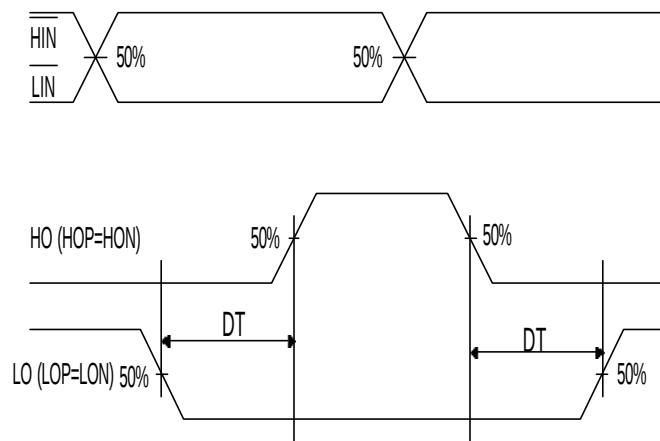


Figure 6. Internal Deadtime Timing

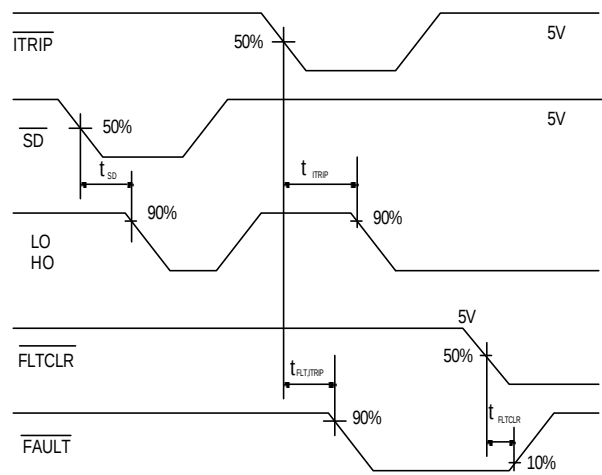
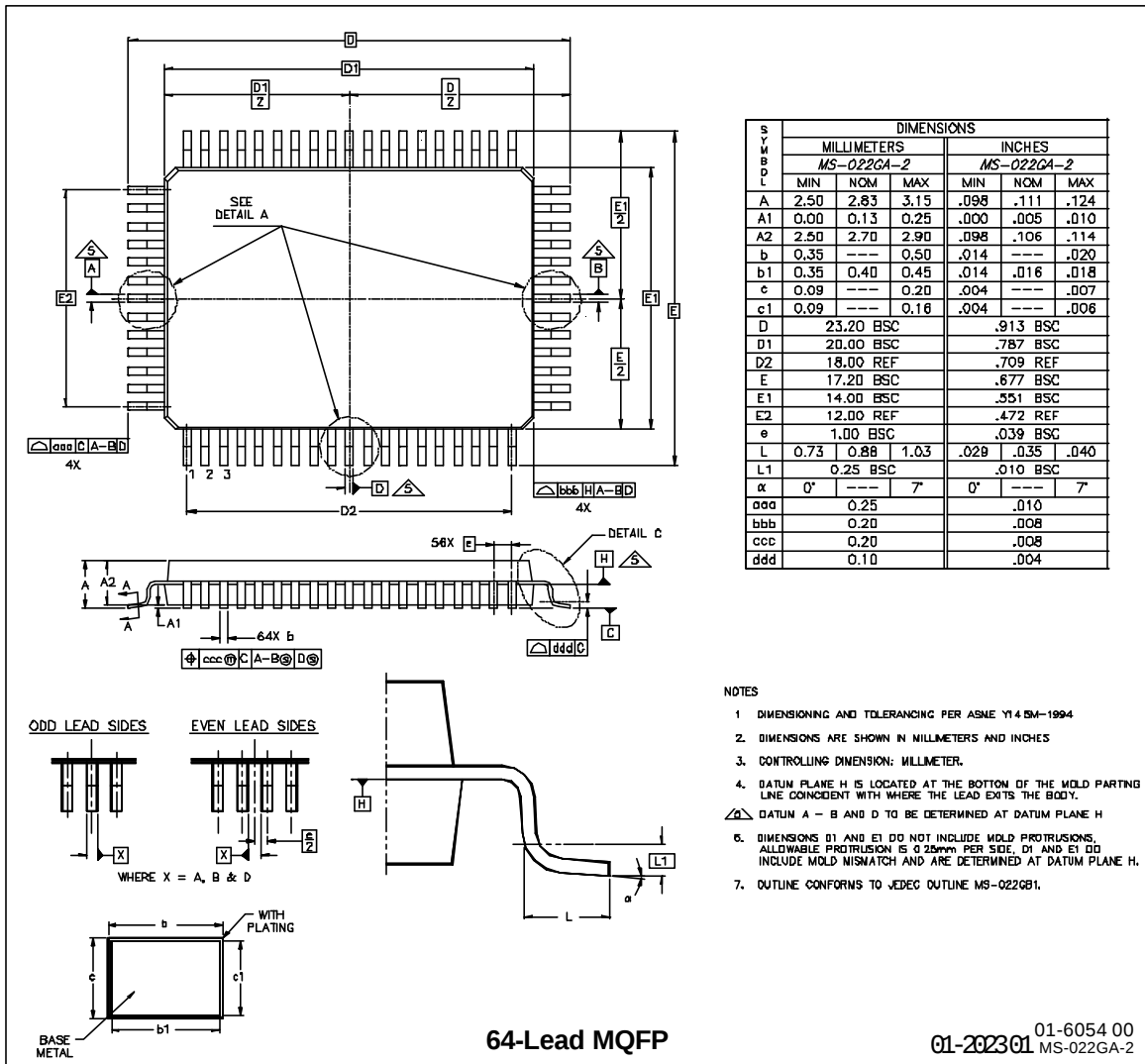


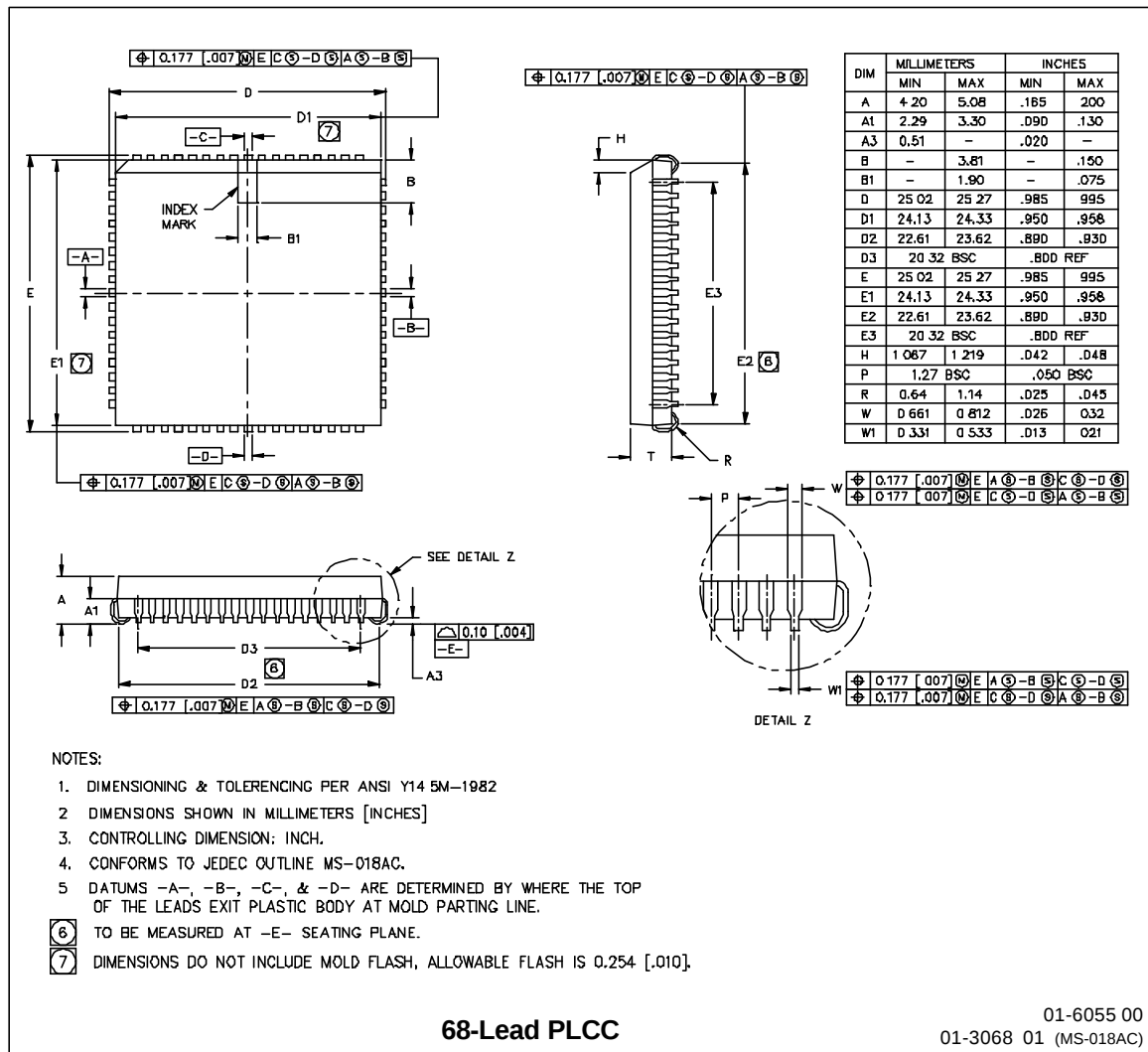
Figure 7. SD, ITRIP Timing

Case outlines



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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
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