ISSI®

IS61C25616

256K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 5V SUPPLY

ADVANCE INFORMATION
FEBRUARY 1999

FEATURES

- High-speed access time: 10, 12, and 15 ns
- CMOS low power operation
- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- 2V data retention (optional)
- Available 44-pin TSOP (Type II) and 44-pin SOJ

DESCRIPTION

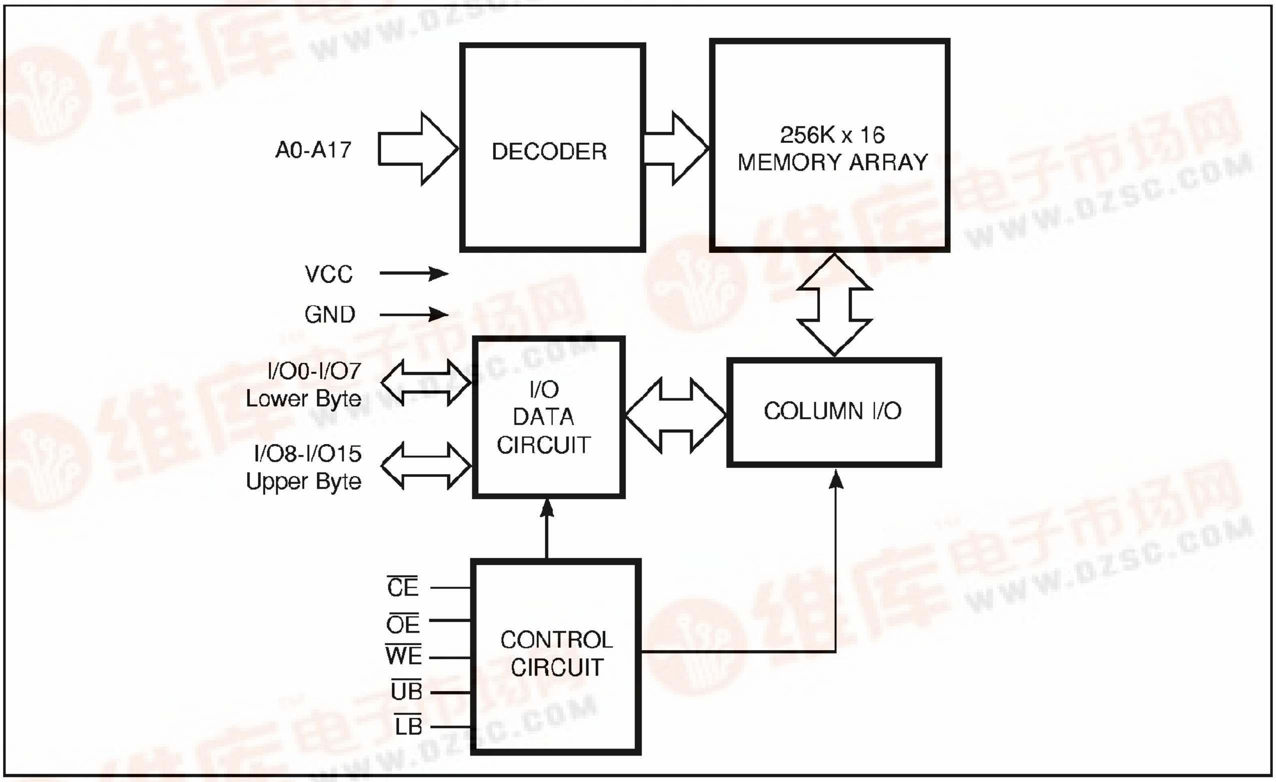
The *ISSI* IS61C25616 is a high-speed, 4,194,304-bit static RAM organized as 262,144 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

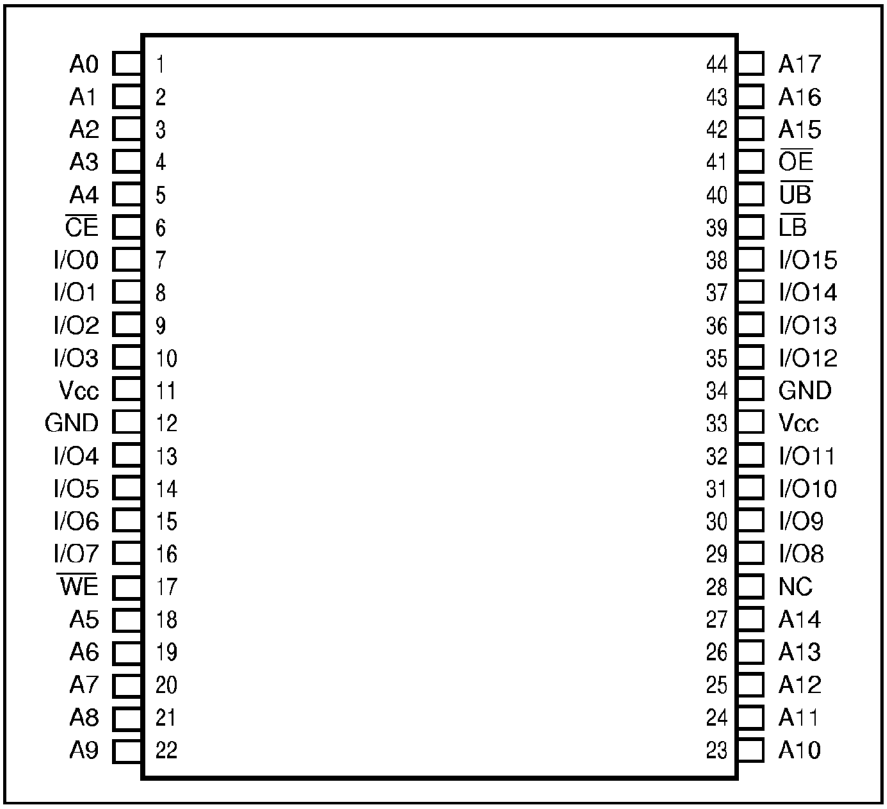
The IS61C25616 is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

44-Pin TSOP (Type II) and SOJ



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

						I/O PIN		
Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	**I/O0-I/O7**	**I/O8-I/O15**	**Vcc Current**
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	–45 to +90	°C
V_{CC}	Vcc Related to GND	–0.3 to +4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

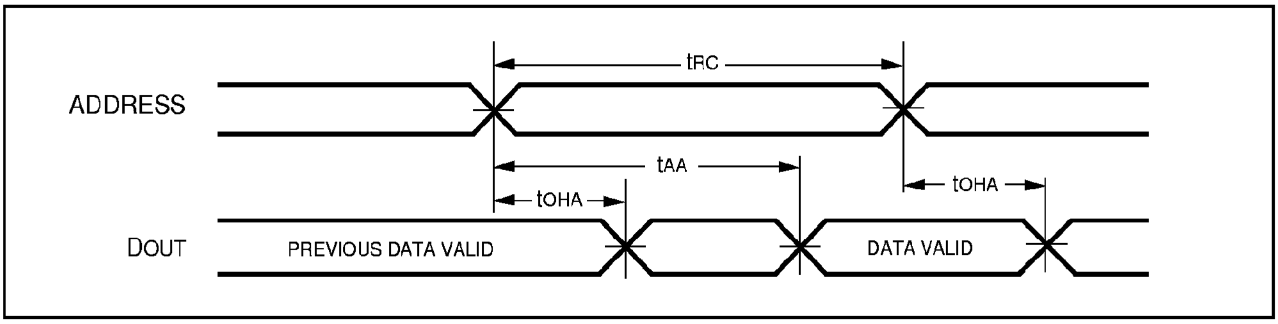
POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

				-10		-12		-15		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC1}	Vcc Dynamic Operating Supply Current	V_{CC} = 2.5V, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	215	—	200	—	180	mA
			Ind.	—	230	—	215	—	195	
I_{CC2}	Vcc Static Operating Supply Current	V_{CC} = Max, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = 0	Com.	—	115	—	115	—	115	mA
			Ind.	—	130	—	130	—	130	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH} , f = max.	Com.	—	55	—	50	—	45	mA
			Ind.	—	60	—	55	—	50	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	

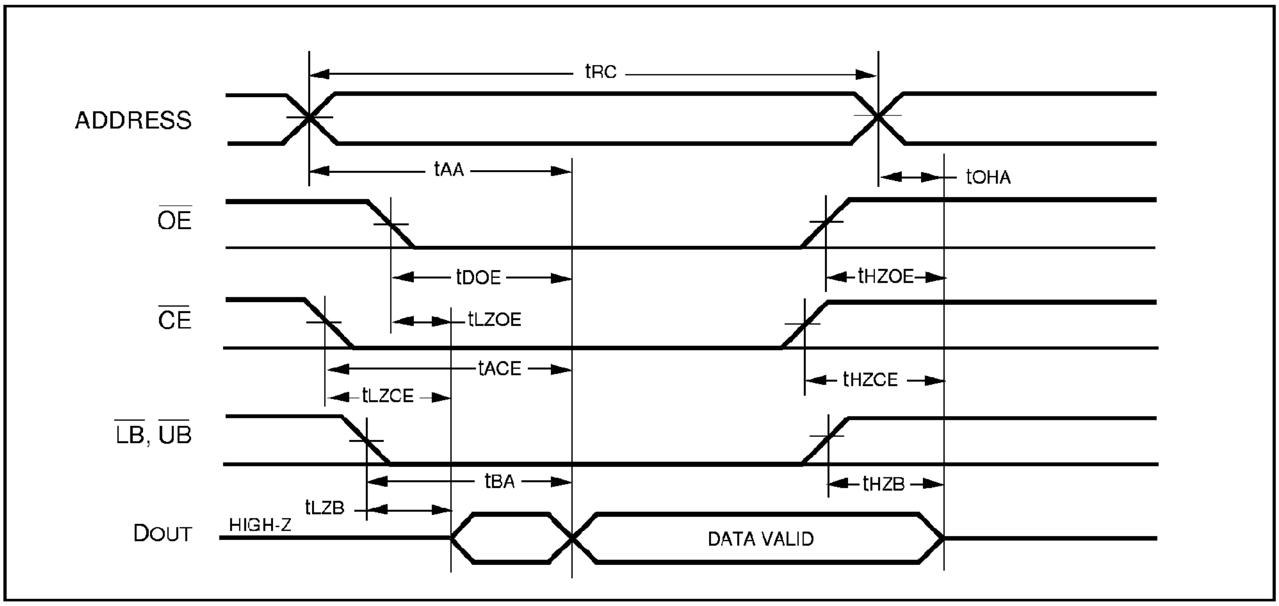
Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

AC WAVEFORMS

READ CYCLE NO. 1(1,2) (Address Controlled) ($\overline{\text{CE}}$ = $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{UB}}$ or $\overline{\text{LB}}$ = V_{IL})



READ CYCLE NO. 2(1,3)



Notes:
1. $\overline{\text{WE}}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$, $\overline{\text{UB}}$, or $\overline{\text{LB}}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

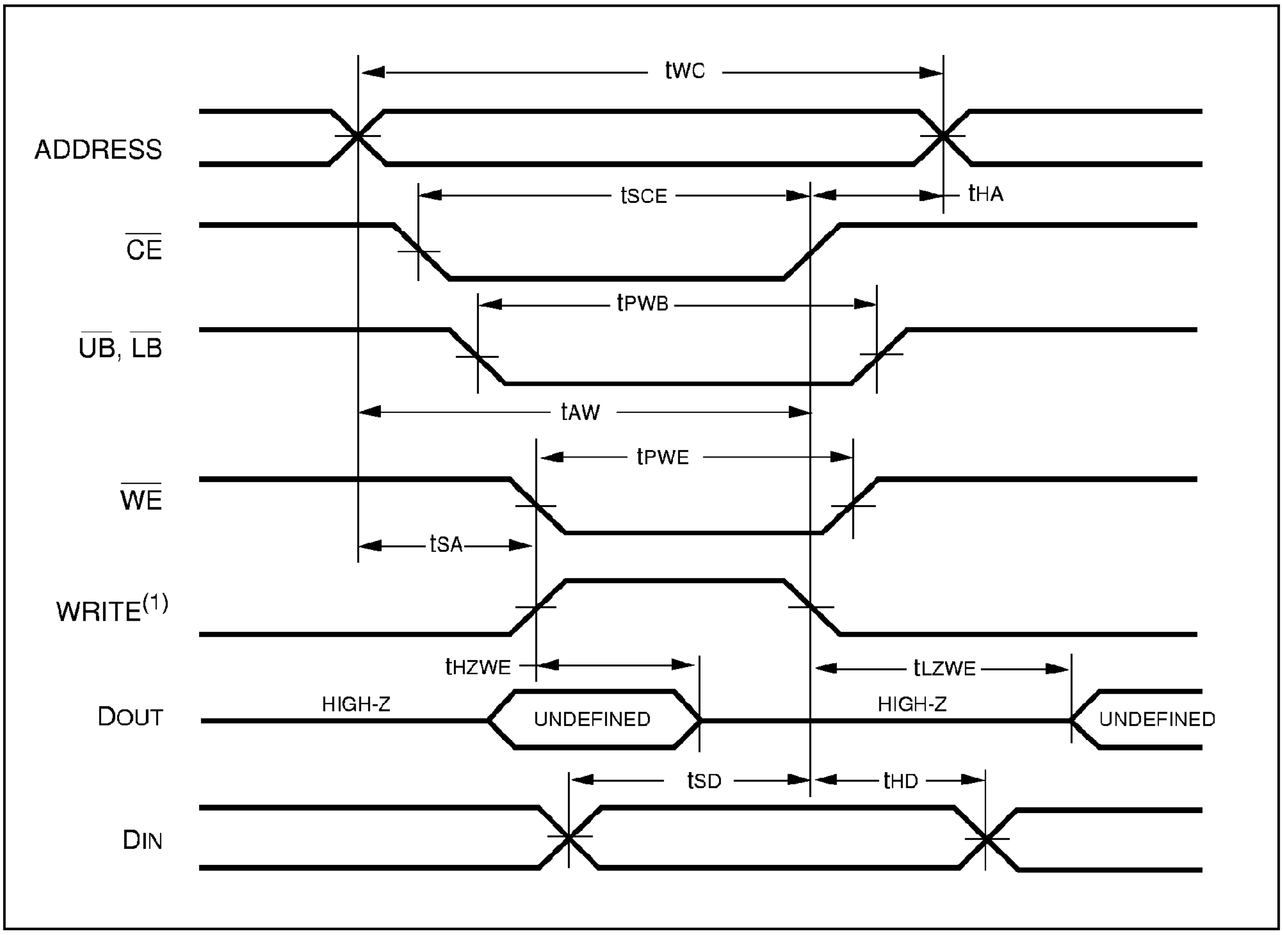
		-10		-12		-15		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	8	—	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	8	—	9	—	10	—	ns
t_{BW}	Byte Write Valid	8	—	8	—	10	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	8	—	9	—	10	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	10	—	12	—	12	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}(2)	$\overline{WE}$ LOW to High-Z Output	—	5	—	6	—	7	ns
t_{LZWE}(2)	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ Controlled)(1,2)

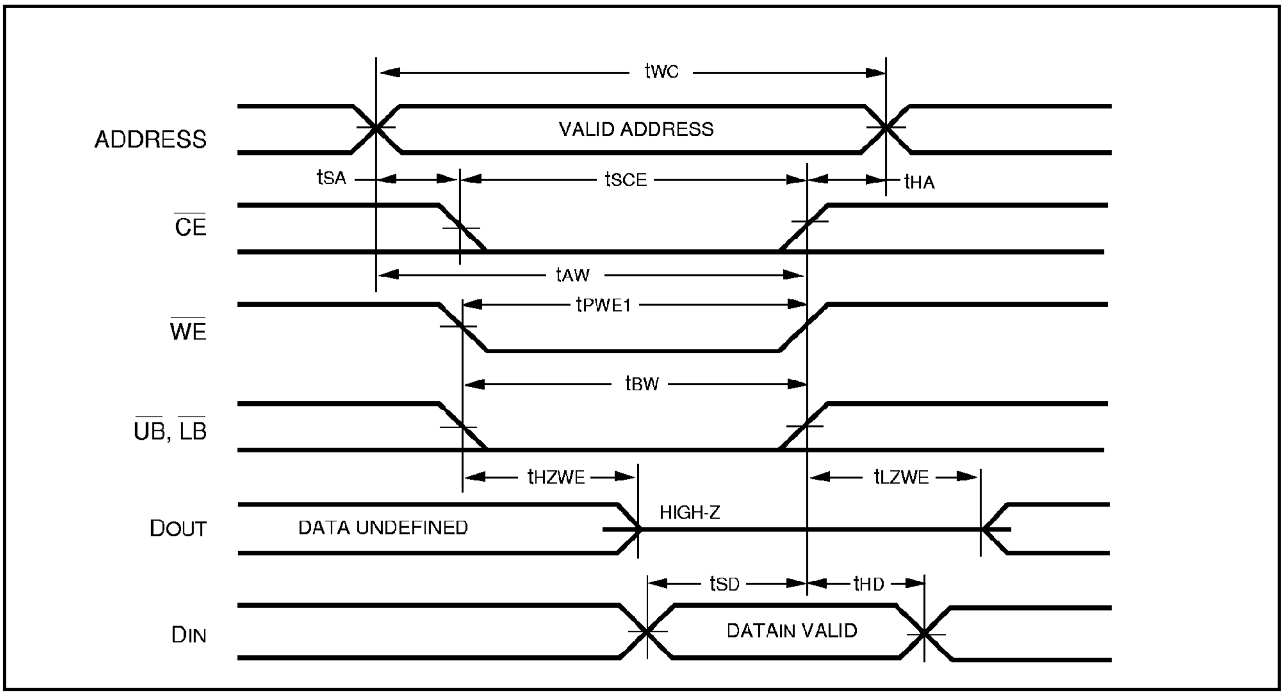


Notes:

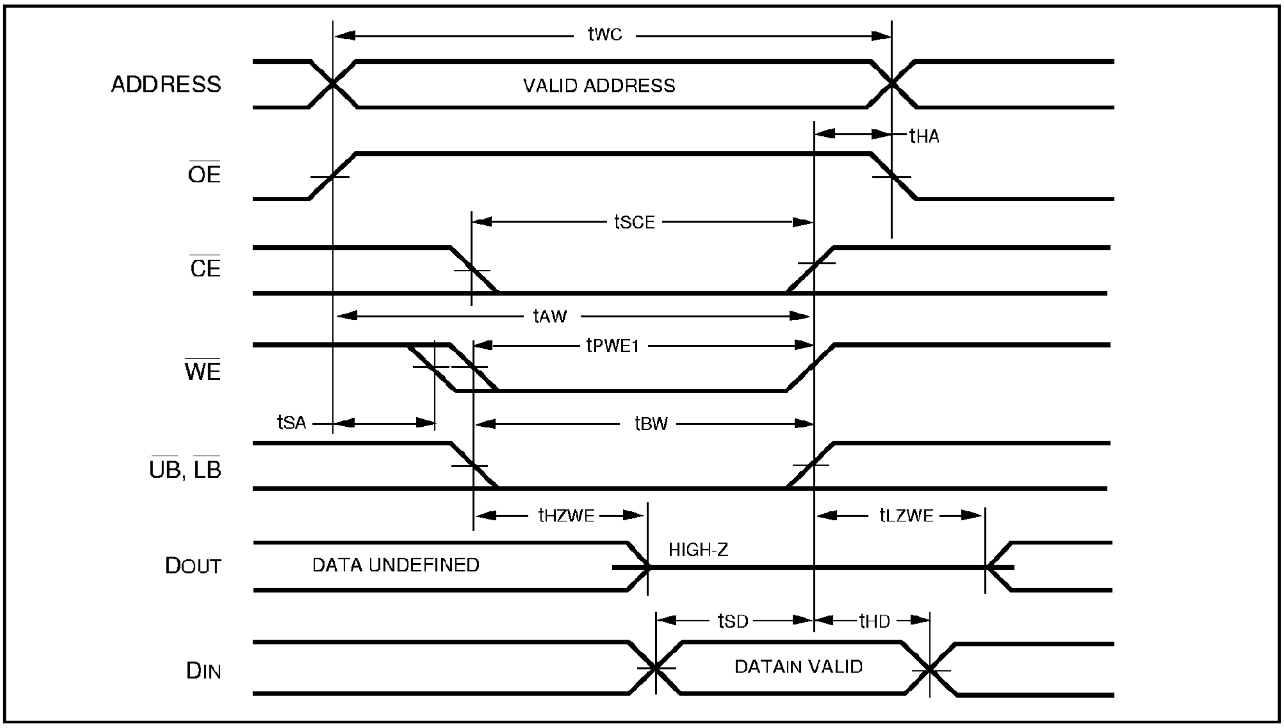
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ inputs and at least one of the $\overline{\text{LB}}$ and $\overline{\text{UB}}$ inputs being in the LOW state.
2. WRITE = ($\overline{\text{CE}}$) [($\overline{\text{LB}}$) = ($\overline{\text{UB}}$)] ($\overline{\text{WE}}$).

AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW)

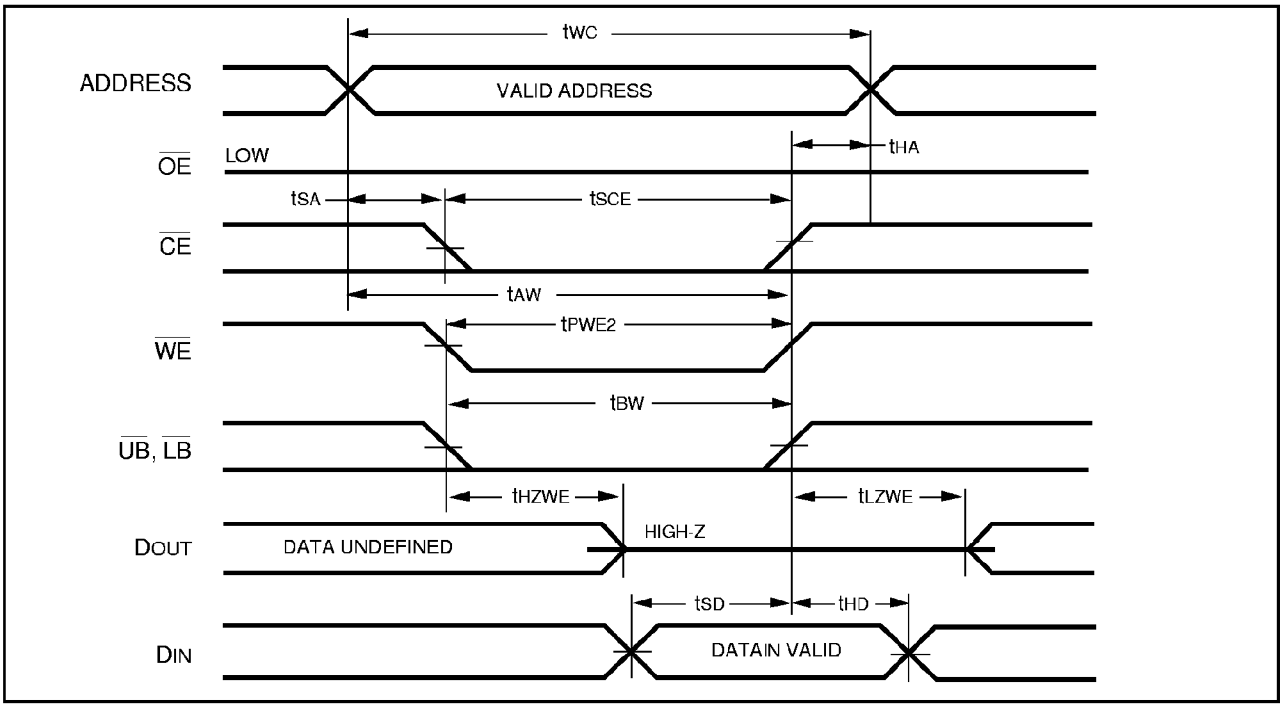


WRITE CYCLE NO. 3 ($\overline{OE}$ is HIGH During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{\text{OE}}$ is LOW During Write Cycle)



WRITE CYCLE NO. 5 ($\overline{\text{UB}}$, $\overline{\text{LB}}$ Controlled)