IXYS

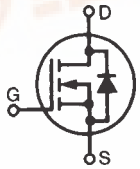
Advanced Technical Information

PolarHT™ Power MOSFET

IXTK 200N10P

V_{DSS} = 100 V
I_{D25} = 200 A
$R_{DS(on)}$ = 7.5 mΩ

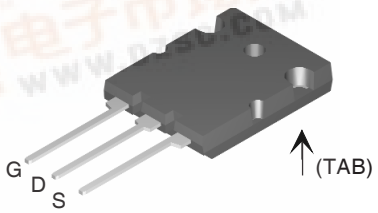
N-Channel Enhancement Mode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	100	V
V_{DGR}	T_J = 25°C to 175°C; R_{GS} = 1 MΩ	100	V
V_{GSM}		±20	V
I_{D25}	T_C = 25°C	200	A
$I_{D(RMS)}$	External lead current limit	75	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	400	A
I_{AR}	T_C = 25°C	60	A
E_{AR}	T_C = 25°C	100	mJ
E_{AS}	T_C = 25°C	4	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	800	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		10 g	

Symbol (T_J = 25°C, unless otherwise specified)	Test Conditions	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA	100			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 500µA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	µA
	T_J = 150°C			250	µA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5\ I_{D25}$			7.5	mΩ
	V_{GS} = 15 V, I_D = 400A		5.5		mΩ
	Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				

TO-264(SP) (IXTK)



G = Gate D = Drain
S = Source TAB = Drain

Features

- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect

Advantages

- Easy to mount
- Space savings
- High power density

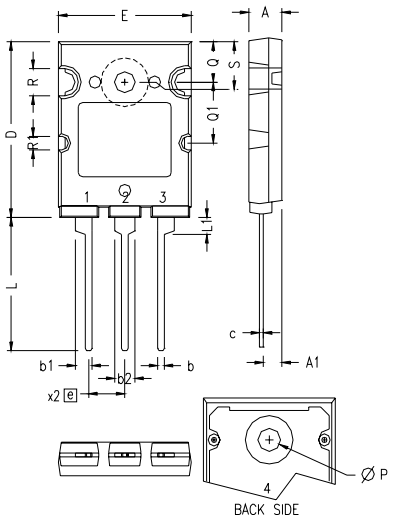
PolarHT™ DMOS transistors utilize proprietary designs and process. US patent is pending.

Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V; I_D = 0.5 I_{D25}, pulse test	60	97		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7600		pF
C_{oss}			2900		pF
C_{rss}			860		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 60 A R_G = 3.3 Ω (External)		30		ns
t_r			35		ns
$t_{d(off)}$			150		ns
t_f			90		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		240		nC
Q_{gs}			50		nC
Q_{gd}			135		nC
R_{thJC}				0.18	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	Characteristic Values Min.	typ.	Max.	
I_S	V_{GS} = 0 V			200	A
I_{SM}	Repetitive			400	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 25 A -di/dt = 100 A/µs		120		ns
Q_{RM}	V_R = 100 V		3.3		µC

TO-264(SP) Outline (IXTK)



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.70	5.30
A1	.102	.118	2.60	3.00
b	.035	.049	0.90	1.25
b1	.091	.106	2.30	2.70
b2	.110	.126	2.80	3.20
c	.020	.033	0.50	0.85
D	1.012	1.035	25.70	26.30
E	.776	.799	19.70	20.30
e	.215BSC		5.46 BSC	
L	.768	.807	19.50	20.50
L1	.091	.106	2.30	2.70
ØP	.122	.138	3.10	3.50
Q	.228	.244	5.80	6.20
Q1	.346	.362	8.80	9.20
ØR	.150	.165	3.80	4.20
ØR1	.071	.087	1.80	2.20
S	.228	.244	5.80	6.20

1 – GATE
2, 4 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)

NOTE: Leads and back heatsink are solder plated.

Fig. 1. Output Characteristics @ 25ºC

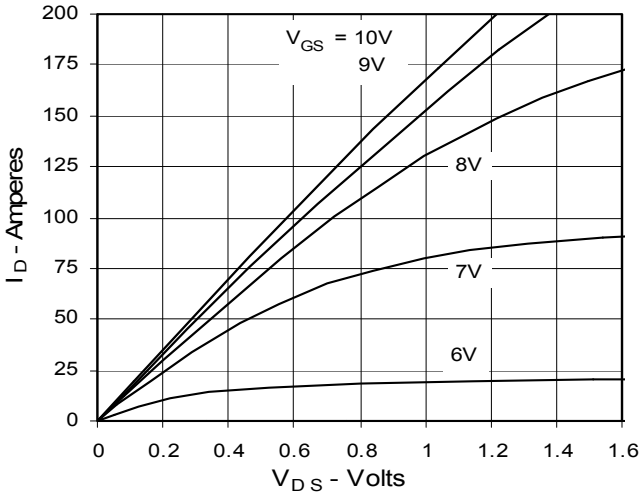


Fig. 2. Extended Output Characteristics @ 25ºC

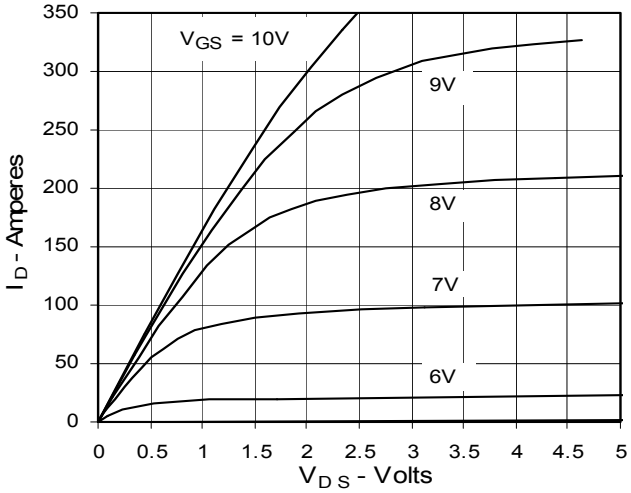


Fig. 3. Output Characteristics @ 150ºC

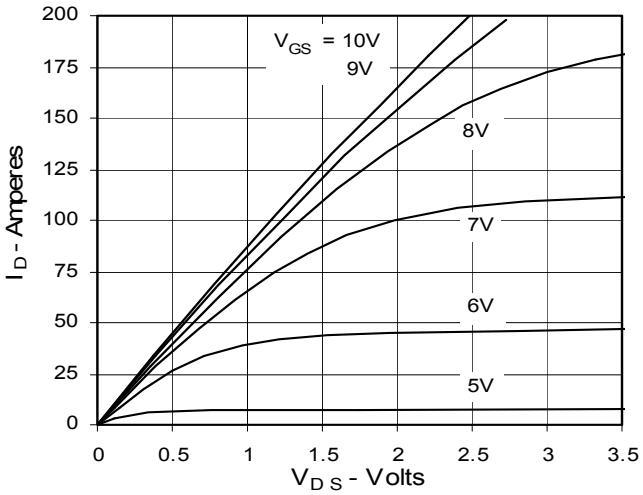


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

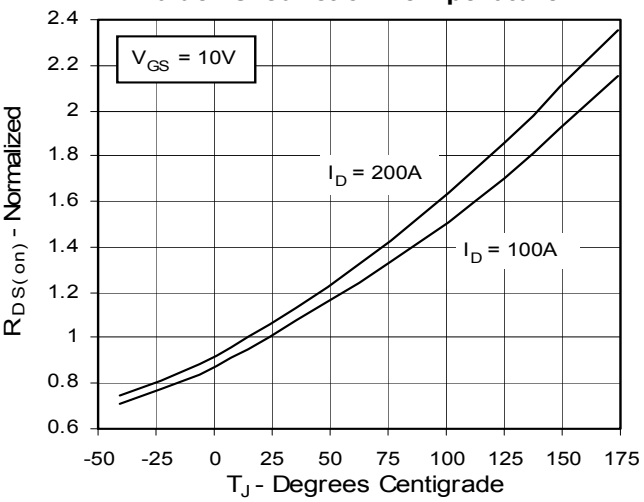


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Drain Current

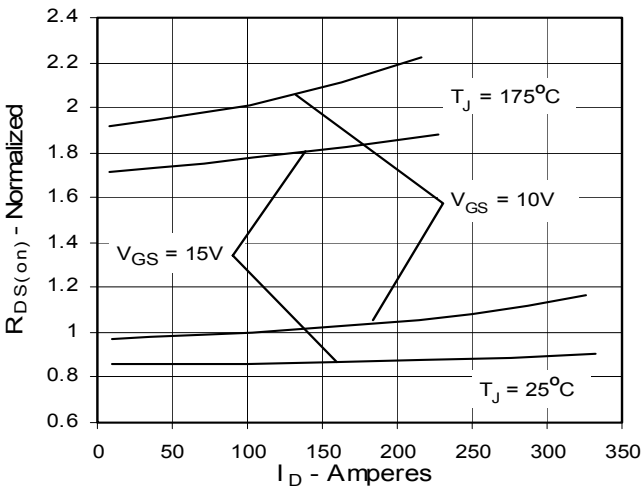


Fig. 6. Drain Current vs. Case Temperature

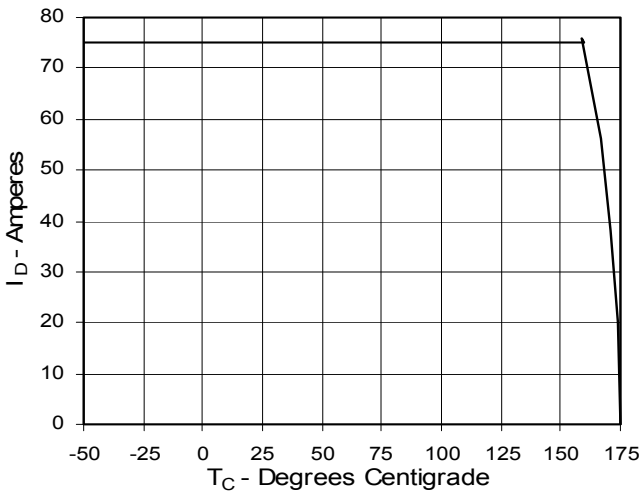


Fig. 7. Input Admittance

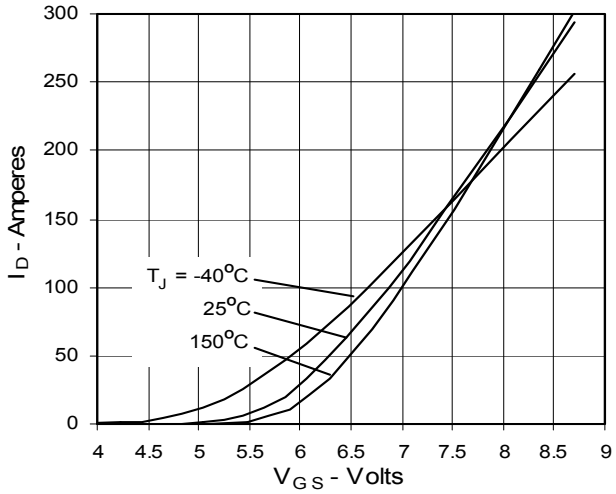


Fig. 8. Transconductance

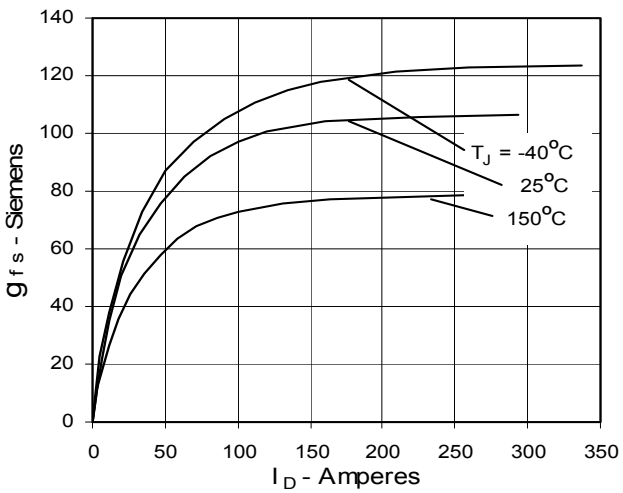


Fig. 9. Source Current vs. Source-To-Drain Voltage

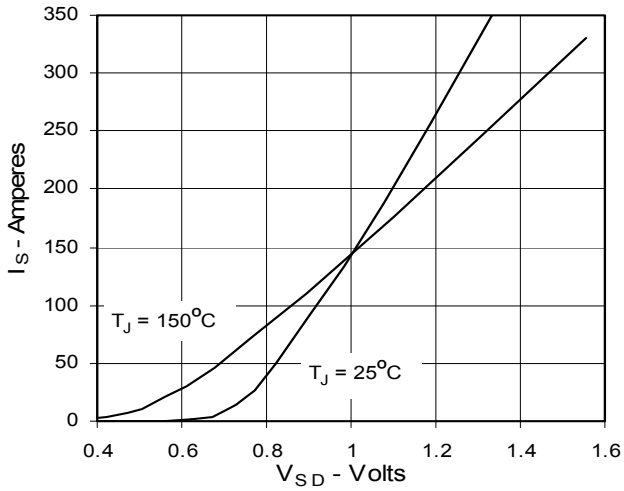


Fig. 10. Gate Charge

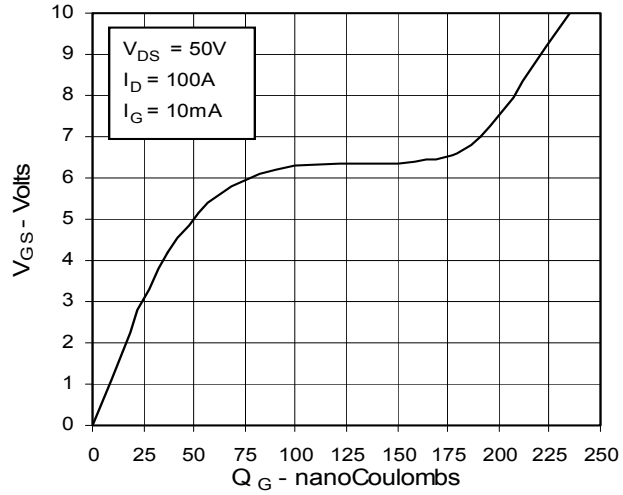


Fig. 11. Capacitance

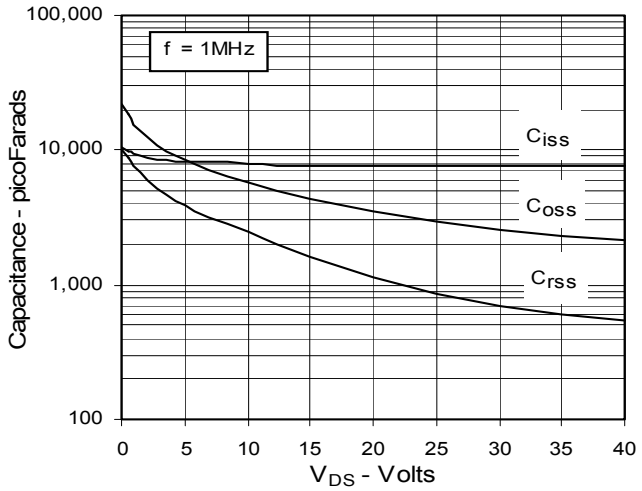


Fig. 12. Forward-Bias Safe Operating Area

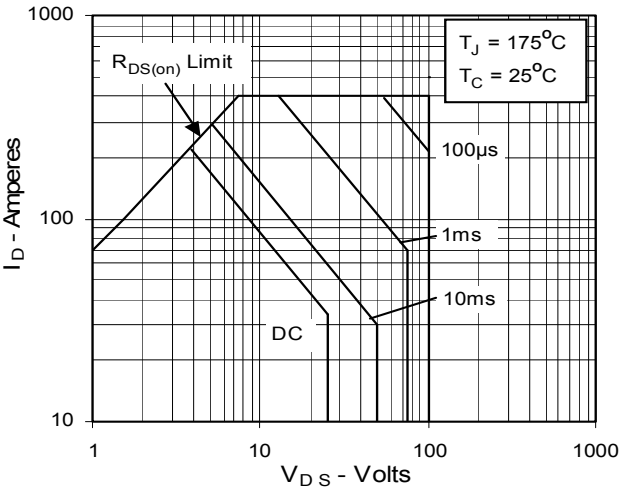


Fig. 13. Maximum Transient Thermal Resistance