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KB3511

High Efficiency, Low Noise, Fast Transient Dual 800mA, 2.2MHz Step-Down DC/DC Converter

System-Power

FEATURES

- Up to 97% Efficiency
- 25uA No Load Current Per Channel
- 800mA Output Current
- 2.5V to 6.5V Input Voltage Range
- 2.2MHz Constant Frequency Operation
- No Schottky Diode Required
- Low Dropout Operation: 100% Duty Cycle
- 0.6V Reference Allows Low Output Voltages
- Shutdown Mode Draws ≤ 1μA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- DFN33-10 Package

APPLICATIONS

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- Digital Still Cameras
- MP3 Players
- Portable Instruments

DESCRIPTION

The KB3511 is a high efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. The device is available in an adjustable version and fixed output voltages of 1.8V and 3.3V. Supply current during operation is only 25μA and drops to ≤1μA in shutdown. The 2.5V to 6.5V input voltage range makes the KB3511 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. Automatic Trickle Mode operation increases efficiency at light loads, further extending battery life.

Switching frequency is internally set at 2.2MHz, allowing the use of small surface mount inductors and capacitors.

The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.6V feedback reference voltage. The KB3511 is available in a low profile (0.8mm) DFN33-10 package.
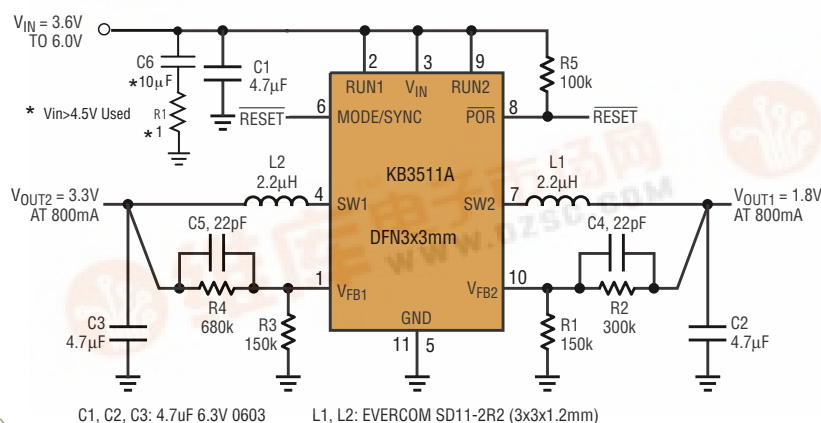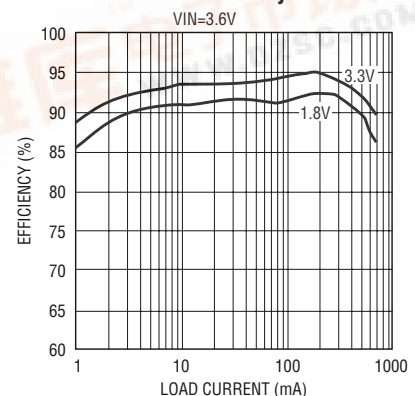
TYPICAL APPLICATION

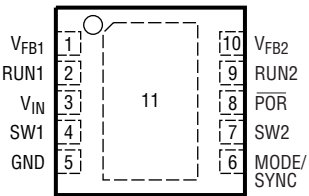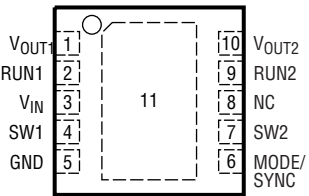**Figure 1. 3.3V/1.8V at 800mA Step-Down Regulators 1.3mm Height Core Supply**

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage .... −0.3V to 6.5V
RUN, V_{FB} Voltages .... −0.3V to V_{IN}
SW Voltage .... −0.3V to (V_{IN} + 0.3V)
P-Channel Switch Source Current (DC) 800mA
N-Channel Switch Sink Current (DC) 800mA

Peak SW Sink and Source Current 1.3A
Operating Temperature Range (Note 2) .. −40°C to 85°C
Junction Temperature (Note 3) .... 125°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................. 300°C

PACkAGE/ORDER INFORMATION

TOP VIEW

V_{FB1}	1	10 V_{FB2}
RUN1	2	9 RUN2
V_{IN}	3	8 $\overline{POR}$
SW1	4	7 SW2
GND	5	6 MODE/SYNC

11

DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

EXPOSED PAD IS PGND (PIN 11)
MUST BE CONNECTED TO GND

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER

KB3511A

V_{FB1} = V_{FB2} = 0.6V

DD PART MARKING

TOP VIEW

V_{OUT1}	1	10 V_{OUT2}
RUN1	2	9 RUN2
V_{IN}	3	8 NC
SW1	4	7 SW2
GND	5	6 MODE/SYNC

11

DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

EXPOSED PAD IS PGND (PIN 11)
MUST BE CONNECTED TO GND

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER

KB3511B

V_{OUT1} = 1.5V
V_{OUT2} = 2.2V

DD PART MARKING

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.
V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.5		6.5	V
I_{FB}	Feedback Pin Input Current		●			30	nA
V_{FB}	Feedback Voltage (Note 3)	0°C ≤ T_A ≤ 85°C		0.588	0.6	0.612	V
		−40°C ≤ T_A ≤ 85°C	●	0.585	0.6	0.612	V
$\Delta V_{LINE\ REG}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 3)			0.3	0.5	%/V
$\Delta V_{LOAD\ REG}$	Output Voltage Load Regulation	(Note 3)			0.5		%
I_S	Input DC Supply Current						
	Active Mode	V_{FB1} = V_{FB2} = 0.6V			50	100	μA
	Shutdown	RUN = 0V, V_{IN} = 5.5V, MODE/SYNC = 0V			0.1	1	μA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V	●	1.6	2.2	2.8	MHz
f_{SYNC}	Synchronization Frequency				2.2		MHz
I_{LIM}	Peak Switch Current Limit	V_{IN} = 3V, FBK = 0.5V, Duty Cycle <35%		0.85	1	1.25	A
$R_{DS(ON)}$	Top Switch On-Resistance	V_{IN} = 3.6V (Note 6)			0.35	0.45	Ω
	Bottom Switch On-Resistance	V_{IN} = 3.6V (Note 6)			0.30	0.45	Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5V, V_{RUN} = 0V, V_{FB} = 0V			0.01	1	μA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.
V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POR	Power-On Reset Threshold	V_{FB} Ramping Up, MODE/SYNC = 0V			8.5		%
		V_{FB} Ramping Down, MODE/SYNC = 0V			−8.5		%
	Power-On Reset On-Resistance				100	200	Ω
	Power-On Reset Delay				262,144		Cycles
V_{RUN}	RUN Threshold High		●	0.3	1	1.5	V
I_{RUN}	RUN Leakage Current		●		0.01	1	μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The KB3511 is guaranteed to meet specified performance from 0°C to 70°C. Specifications over the −40°C and 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The KB3511 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.
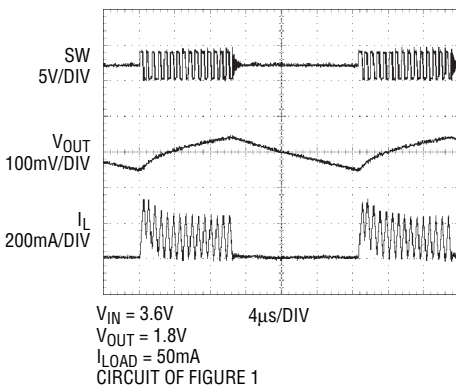
Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \cdot \theta_{JA})$.
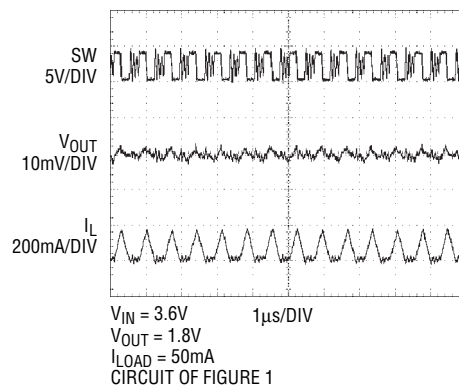
Note 6: The DFN switch on-resistance is guaranteed by correlation to wafer level measurements.
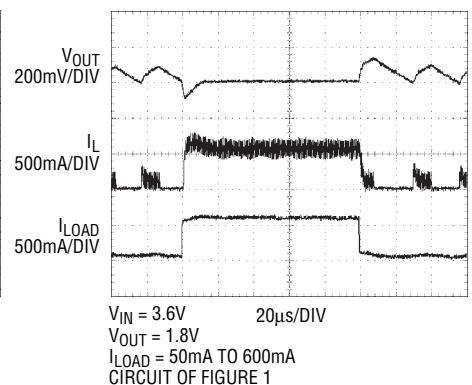
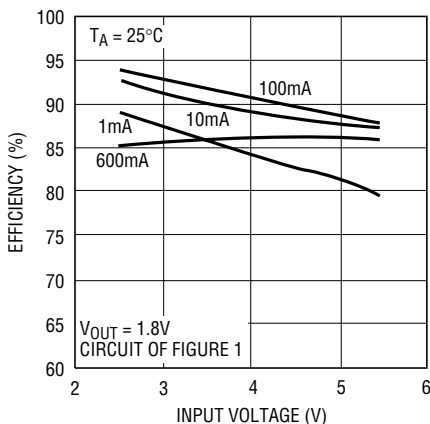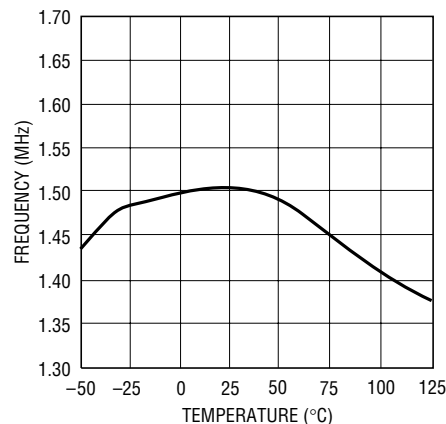# TYPICAL PERFORMANCE CHARACTERISTICS

Trickle Mode Operation

SW 5V/DIV
V_{OUT} 100mV/DIV
I_L 200mA/DIV

V_{IN} = 3.6V 4μs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 50mA
CIRCUIT OF FIGURE 1

PWM Mode

SW 5V/DIV
V_{OUT} 10mV/DIV
I_L 200mA/DIV

V_{IN} = 3.6V 1μs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 50mA
CIRCUIT OF FIGURE 1

Load Step

V_{OUT} 200mV/DIV
I_L 500mA/DIV
I_{LOAD} 500mA/DIV

V_{IN} = 3.6V 20μs/DIV
V_{OUT} = 1.8V
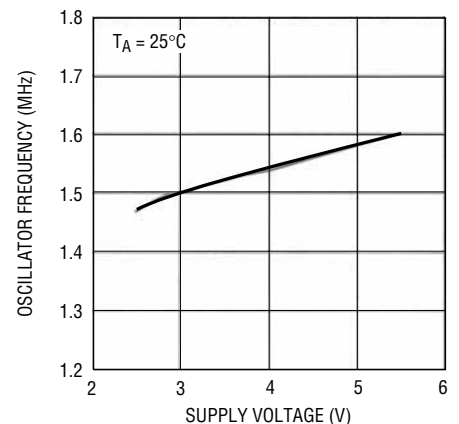I_{LOAD} = 50mA TO 600mA
CIRCUIT OF FIGURE 1

Efficiency vs Input Voltage

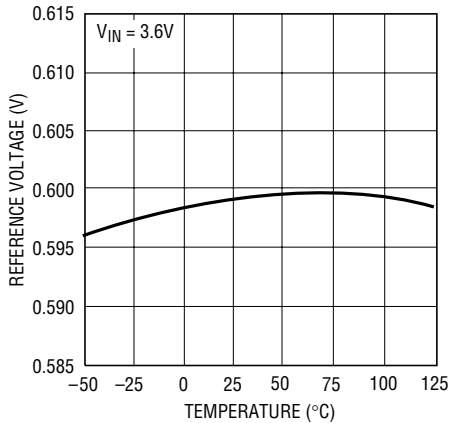### Oscillator Frequency vs Temperature
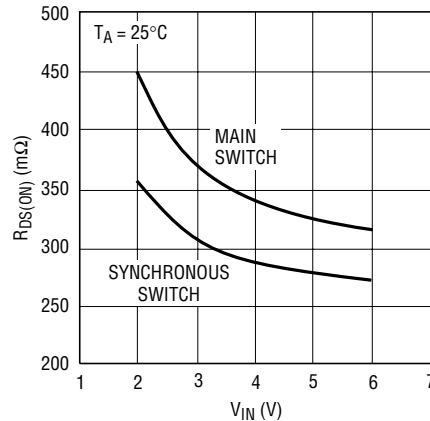

Oscillator Frequency vs Supply Voltage
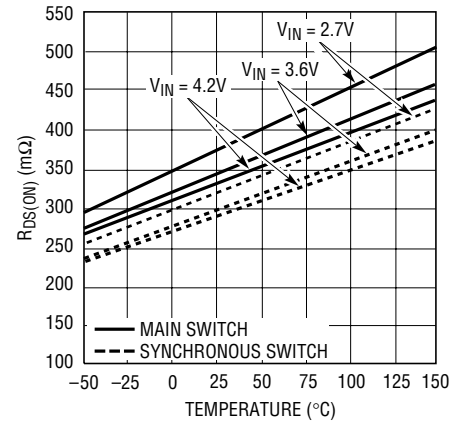
TYPICAL PERFORMANCE CHARACTERISTICS

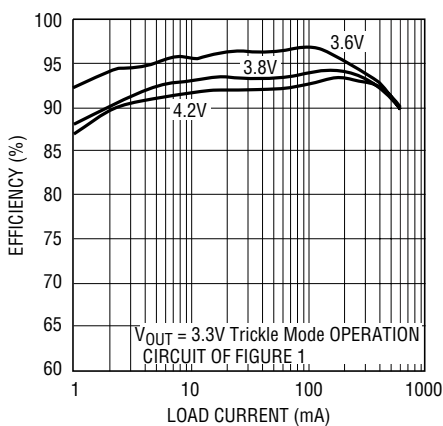**Reference Voltage vs Temperature**
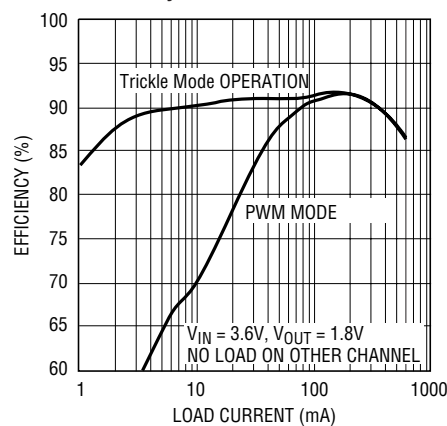

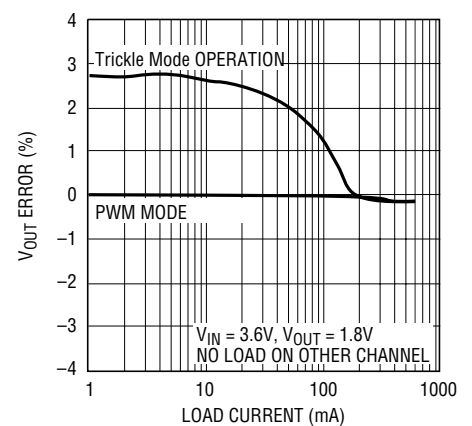**$R_{DS(ON)}$ vs Input Voltage**

$R_{DS(ON)}$ vs Temperature

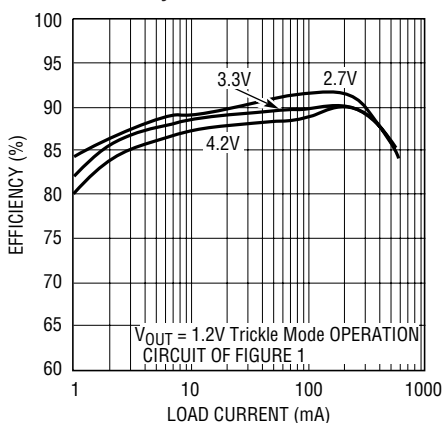

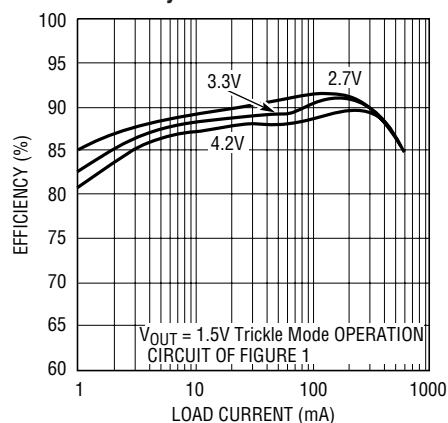**Efficiency vs Load Current**
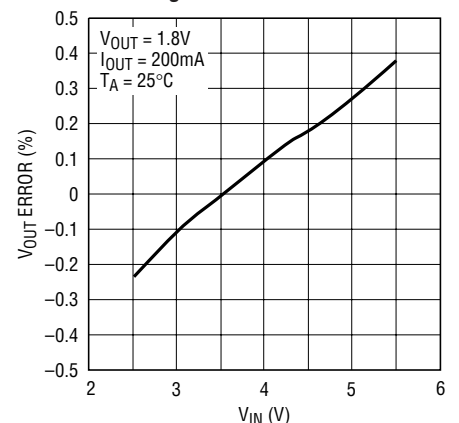

Efficiency vs Load Current

Load Regulation

Efficiency vs Load Current

Efficiency vs Load Current

Line Regulation

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PIN FUNCTIONS

V_{FB1} (Pin 1): Output Feedback. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.

RUN1 (Pin 2): Regulator 1 Enable. Forcing this pin to V_{IN} enables regulator 1, while forcing it to GND causes regulator 1 to shut down.

V_{IN} (Pin 3): Main Power Supply. Must be closely decoupled to GND.

SW1 (Pin 4): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

GND (Pin 5): Main Ground. Connect to the (–) terminal of C_{OUT}, and (–) terminal of C_{IN}.

MODE/SYNC (Pin 6): Combination Mode Selection and Oscillator Synchronization. This pin controls the operation of the device. When tied to V_{IN} or GND, Trickle Mode operation or PWM mode is selected, respectively. Do not float this pin. The oscillation frequency can be syncronized to an external oscillator applied to this pin and pulse skipping mode is automatically selected.

SW2 (Pin 7): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

$\overline{POR}$ (Pin 8): Power-On Reset . This common-drain logic output is pulled to GND when the output voltage is not within ±8.5% of regulation and goes high after 175ms when both channels are within regulation.

RUN2 (Pin 9): Output Feedback. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down.

V_{FB2} (Pin 10): Output Feedback. Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.

Exposed Pad (GND) (Pin 11): Power Ground. Connect to the (–) terminal of C_{OUT}, and (–) terminal of C_{IN}. Must be soldered to electrical ground on PCB.

SIMPLIFIED BLOC DIAGRAM
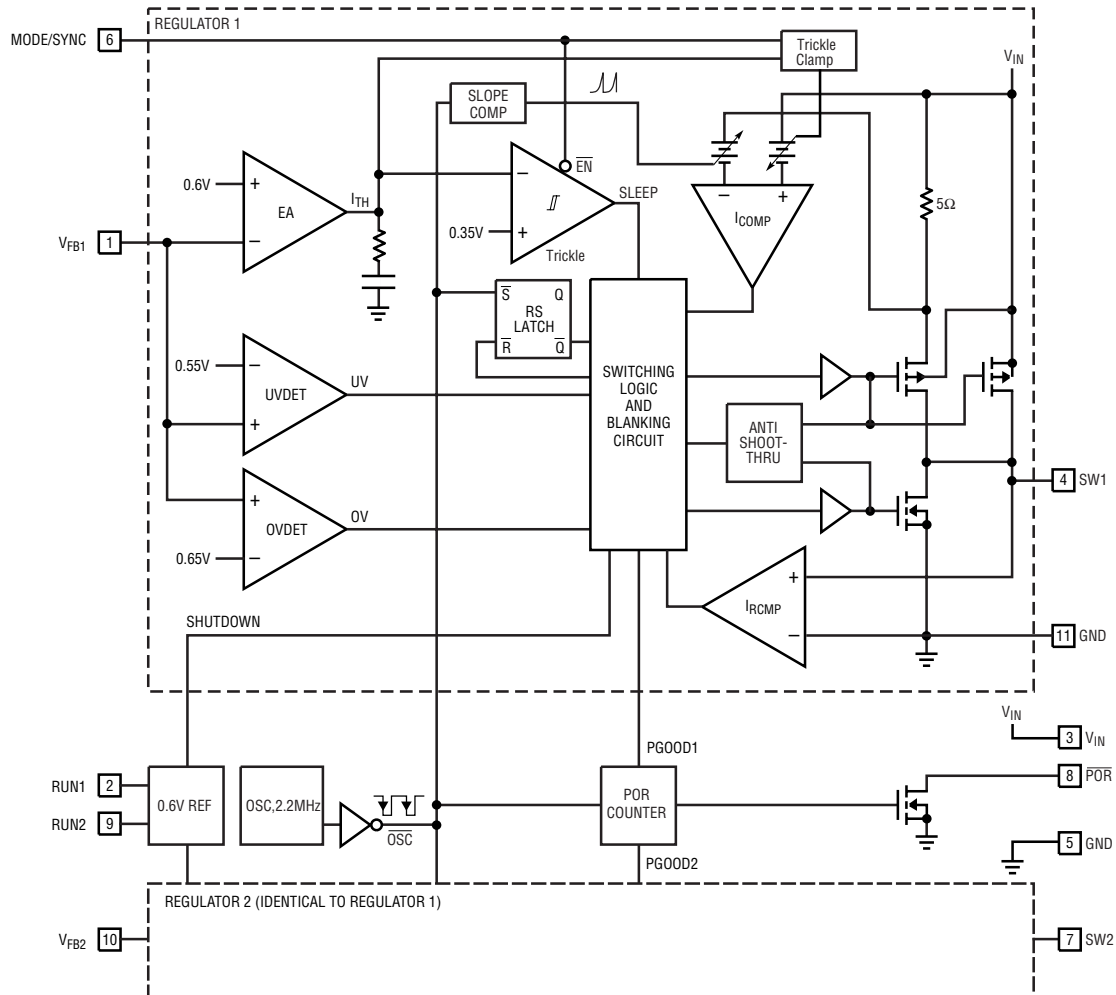
OPERATION

The KB3511 uses a constant frequency, current mode architecture. The operating frequency is set at 2.2MHz and can be synchronized to an external oscillator. Both channels share the same clock and run in-phase. To suit a variety of applications, the selectable Mode pin allows the user to trade-off noise for efficiency.

The output voltage is set by an external divider returned to the V_{FB} pins. An error amplfier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the $\overline{POR}$ output low if the output voltage is not within ±8.5%. The $\overline{POR}$ output will go high after 262,144 clock cycles (about 120ms) of achieving regulation.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle.

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier.This amplifier compares the V_{FB} pin to the 0.6V reference. When the load current increases, the V_{FB} voltage decreases slightly below the reference. This

OPERATION

decrease causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

Low Current Operation

Two modes are available to control the operation of the KB3511 at low currents. Both modes automatically switch from continuous operation to to the selected mode when the load current is low.

To optimize efficiency, the Trickle Mode operation can be selected. When the load is relatively light, the KB3511 automatically switches into Trickle Mode operation in which the PMOS switch operates intermittently based on load demand with a fixed peak inductor current. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. A hysteretic voltage comparator trips when I_{TH} is below 0.28V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until I_{TH}/RUN exceeds 0.6V, turning on the switch and the main control loop which starts another cycle.

For lower ripple noise at low currents, the pulse skipping mode can be used. In this mode, the KB3511 continues to switch at a constant frequency down to very low currents, where it will begin skipping pulses.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal p-channel MOSFET and the inductor.

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (See Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the KB3511 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information Section).

Low Supply Operation

The KB3511 incorporates an Under-Voltage Lockout circuit which shuts down the part when the input voltage drops below about 1.65V to prevent unstable operation.

APPLICATIONS INFORMATION

A general KB3511 application circuit is shown in Figure 2. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_0 \ L} \left(1 \ \frac{V_{OUT}}{V_{IN}} \right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple,

greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{LIM}$, where I_{LIM} is the peak switch current limit. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_0 \ \Delta I_L} \left(1 \ \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The inductor value will also have an effect on Trickle Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the Trickle clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load

APPLICATIONS INFORMATION

currents. This causes a dip in efficiency in the upper range of low current operation. In Trickle Mode operation, lower inductance values will cause the Trickle frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characterisitics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the KB3511 requires to operate. Table 1 shows some typical surface mount inductors that work well in KB3511 applications.

Input Capacitor (C$_{IN}$) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V$_{OUT}$/V$_{IN}$. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output current I$_{MAX}$ equals the peak current minus half the peak-to-peak ripple current, I$_{MAX}$ = I$_{LIM}$ − ΔI$_L$/2.

This formula has a maximum at V$_{IN}$ = 2V$_{OUT}$, where I$_{RMS}$ = I$_{OUT/2}$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1μF to 1μF ceramic capacitor is also recommended on V$_{IN}$ for high frequency decoupling, when not using an all ceramic capacitor solution.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (μH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm^3)
EVERCOM SD11	1.5	0.043	0.95	3.0 × 3.0 × 1.2
	2.2	0.075	0.80	
	3.3	0.110	0.70	
	4.7	0.162	0.60	
Sumida CMD4D06	2.2	0.116	0.950	3.5 × 4.3 × 0.8
	3.3	0.174	0.770	
	4.7	0.216	0.750	
Panasonic ELT5KT	3.3	0.17	1.00	4.5 × 5.4 × 1.2
	4.7	0.20	0.95	
Murata LQH32CN	1.0	0.060	1.00	2.5 × 3.2 × 2.0
	2.2	0.097	0.79	
	4.7	0.150	0.65	

Output Capacitor (C$_{OUT}$) Selection

The selection of C$_{OUT}$ is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV$_{OUT}$) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8f_0\ C_{OUT}} \right)$$

where f = operating frequency, C$_{OUT}$ = output capacitance and ΔI$_L$ = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI$_L$ increases with input voltage. With ΔI$_L$ = 0.3 • I$_{LIM}$ the output ripple will be less than 100mV at maximum V$_{IN}$ and f$_0$ = 2.2MHz with:

ESR$_{COUT}$ < 150mΩ

Once the ESR requirements for C$_{OUT}$ have been met, the RMS current rating generally far exceeds the I$_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantulum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer

APPLICATIONS INFORMATION

capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost, but also have the lowest capacitance density, a high voltage and temperature coefficient, and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic Special Polymer (SP) capacitors.

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the KB3511 in parallel with the main capacitors for high frequency decoupling.
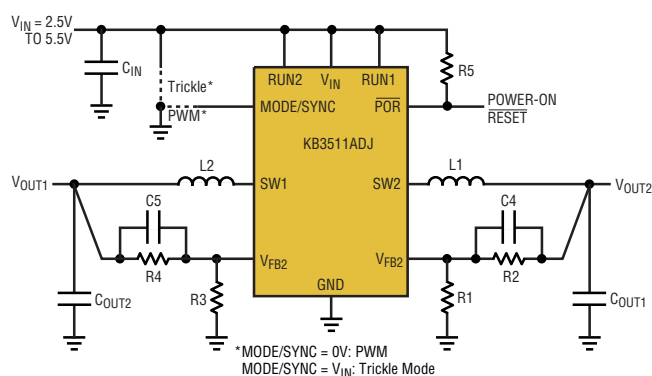

Figure 2. kB3511 General Schematic

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective.

Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used. A good selection of ceramic capacitors is available from Taiyo Yuden, TDK, and Murata.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3-4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 3 \frac{\Delta I_{OUT}}{f_0 \; V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The KB3511 develops a 0.6V reference voltage between the feedback pin, V_{FB}, and the ground as shown in Figure 2. The output voltage is set by a resistive divider according to the following formula:

APPLICATIONS INFORMATION

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making them too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor C_F may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Power-On Reset

The $\overline{POR}$ pin is an open-drain output which pulls low when either regulator is out of regulation. When both output voltages are within ±8.5% of regulation, a timer is started which releases $\overline{POR}$ after 2^{18} clock cycles (about 120ms). This delay can be significantly longer in Trickle Mode operation with low load currents, since the clock cycles only occur during a Trickle and there could be milliseconds of time between Trickles. This can be bypassed by tying the $\overline{POR}$ output to the MODE/SYNC input, to force pulse PWM mode during a reset. In addition, if the output voltage faults during Trickle Mode sleep, $\overline{POR}$ could have a slight delay for an undervoltage output condition and may not respond to an overvoltage output. This can be avoided by using pulse skipping mode instead. When either channel is shut down, the $\overline{POR}$ output is pulled low, since one or both of the channels are not in regulation.

Mode Selection & Frequency Synchronization

The MODE/SYNC pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to V_{IN} enables Trickle Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. When this pin is connected to ground, PWM operation is selected which provides the lowest output ripple, at the cost of low current efficiency.

The KB3511 can also be synchronized to an external 2.2MHz clock signal by the MODE/SYNC pin. During synchronization, the mode is set to pulse skipping and the top switch turn-on is synchronized to the rising edge of the external clock.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feed-forward capacitor, C_F, can be added to improve the high frequency response, as shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would

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produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, 4 main sources usually account for most of the losses in KB3511 circuits: 1)V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flowing through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

I^2R losses = $I_{OUT2}(R_{SW} + R_L)$

4) Other 'hidden' losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the KB3511 does not dissipate much heat due to its high efficiency. However, in applications where the KB3511 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To prevent the KB3511 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$T_{RISE} = P_D \bullet \theta_{JA}$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$T_J = T_{RISE} + T_{AMBIENT}$

As an example, consider the case when the KB3511 is in dropout on both channels at an input voltage of 2.7V with a load current of 800mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the main switch is 0.425Ω. Therefore, power dissipated by each channel is:

$P_D = I^2 \bullet R_{DS(ON)} = 272mW$

The MS package junction-to-ambient thermal resistance, θ_{JA}, is 45°C/W. Therefore, the junction temperature of the

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regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 2 \cdot 0.272 \cdot 45 + 70 = 95°C$$

which is below the absolute maximum junction temperature of 125°C.

Design Example

As a design example, consider using the KB3511 in an portable application with a Li-Ion battery. The battery provides a V_{IN} = 3.6V to 4.2V. The load requires a maximum of 600mA in active mode and 2mA in standby mode. The output voltage is V_{OUT} = 3.3V. Since the load still needs power in standby, Trickle Mode operation is selected for good low load efficiency.

First, calculate the inductor value for about 30% ripple current at maximum V_{IN}:

$$L = \frac{3.3V}{2.2MHz \quad 300mA} \left(1 - \frac{3.3V}{4.2V}\right) = 1.07\mu H$$

Choosing the closest inductor from a vendor of 1.0μH inductor, results in a maximum ripple current of:

$$\Delta I_L = \frac{3.3V}{2.2MHz \quad 1.0\mu} \left(1 - \frac{3.3V}{4.2V}\right) = 330mA$$

For cost reasons, a ceramic capacitor will be used. C_{OUT} selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT} \approx 3 \frac{600mA}{2.2MHz \quad (5\% \quad 3.3V)} = 4.9\mu F$$

The closest standard value is 10μF. Since the output impedance of a Li-Ion battery is very low, C_{IN} is typically 10μF.

The output voltage can now be programmed by choosing the values of R1 and R2. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2μA with the 0.6V feedback voltage makes R1~300k. A close standard 1% resistor is 280k, and R2 is then 887k.

The PGOOD pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed.

Figure 1 shows the complete schematic for this design example.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the KB3511. These items are also illustrated graphically in the layout diagram of Figure 3. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 3) and GND (exposed pad) as close as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.

2. Are the C_{OUT} and L1 closely connected? The (−) plate of C_{OUT} returns current to GND and the (−) plate of C_{IN}.

3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground sense line terminated near GND (exposed pad). The feedback signals V_{FB} should be routed away from noisy components and traces, such as the SW line (Pins 4 and 7), and its trace should be minimized.

4. Keep sensitive components away from the SW pins. The input capacitor C_{IN} and the resistors R1 to R4 should be routed away from the SW traces and the inductors.

5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point and should not share the high current path of C_{IN} or C_{OUT}.

6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.
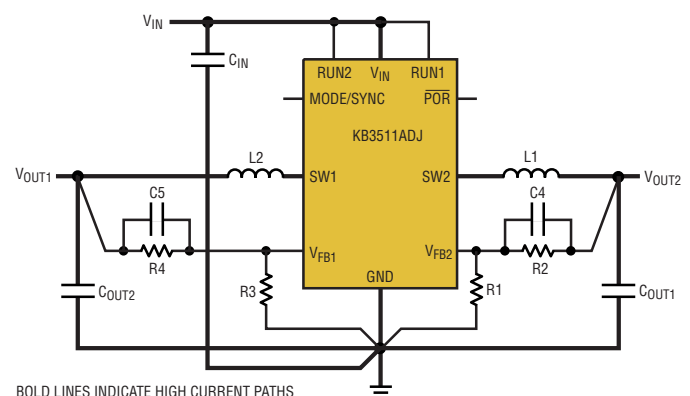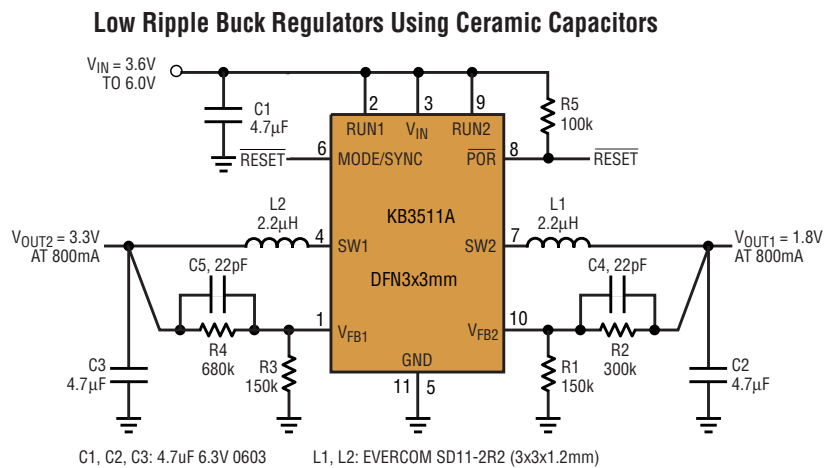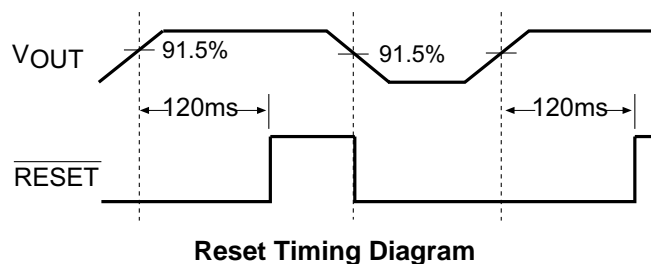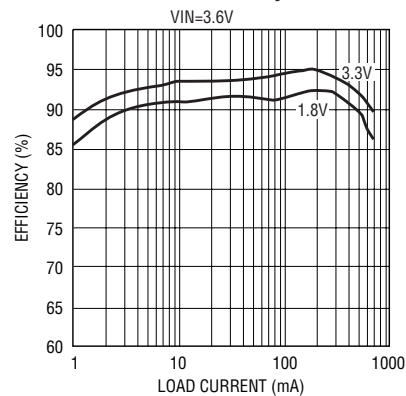

Figure 3. kB3511 Layout Diagram (See Board Layout Checklist)

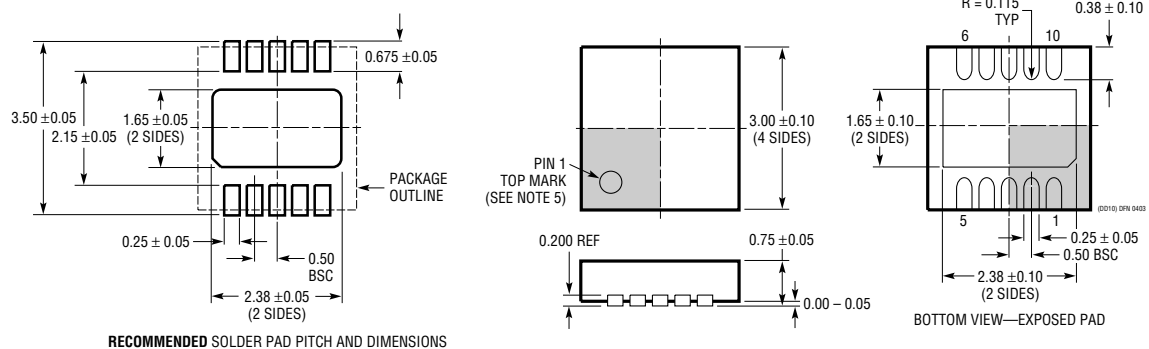## APPLICATIONS INFORMATION
TYPICAL APPLICATION

Low Ripple Buck Regulators Using Ceramic Capacitors

C1, C2, C3: 4.7uF 6.3V 0603   L1, L2: EVERCOM SD11-2R2 (3x3x1.2mm)

KB3511 Efficiency Curve

Reset Timing Diagram

PACAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

PIN 1
TOP MARK
(SEE NOTE 5)

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE KB WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE

4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE