

KEC

SEMICONDUCTOR
TECHNICAL DATA

KHB019N20P1/F1/F2

N CHANNEL MOS FIELD
EFFECT TRANSISTOR

General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for DC/DC converters and switching mode power supplies.

FEATURES

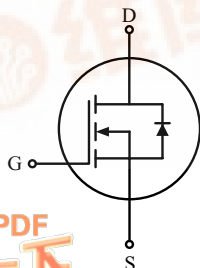
- $V_{DS}=200V$, $I_D=19A$
- Drain-Source ON Resistance : $R_{DS(ON)}=0.18\ \Omega$ @ $V_{GS}=10V$
- $Q_g(\text{typ.})=35nC$

MAXIMUM RATING (Tc=25℃)

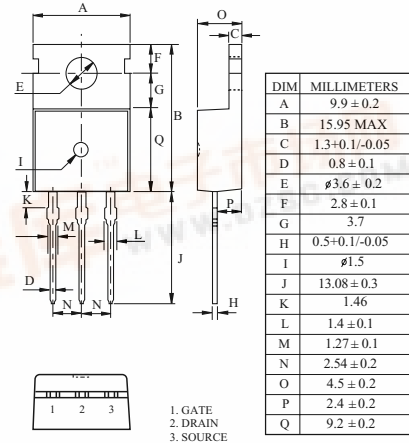
CHARACTERISTIC		SYMBOL	RATING		UNIT
			KHB019N20P1	KHB019N20F1 KHB019N20F2	
Drain-Source Voltage		V _{DSS}	200		V
Gate-Source Voltage		V _{GSS}	±30		V
Drain Current	@T _C =25℃	I _D	19	19*	A
	@T _C =100℃		12.1	12.1*	
	Pulsed (Note1)	I _{DP}	76	76*	
Single Pulsed Avalanche Energy (Note 2)		E _{AS}	250		mJ
Repetitive Avalanche Energy (Note 1)		E _{AR}	14		mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5		V/ns
Drain Power Dissipation	Tc=25℃	P _D	140	50	W
	Derate above 25℃		1.12	0.4	W/℃
Maximum Junction Temperature		T _j	150		℃
Storage Temperature Range		T _{stg}	-55~150		℃
Thermal Characteristics					
Thermal Resistance, Junction-to-Case		R _{thJC}	0.89	2.5	℃/W
Thermal Resistance, Case-to-Sink		R _{thCS}	0.5	-	℃/W
Thermal Resistance, Junction-to-Ambient		R _{thJA}	62.5	62.5	℃/W

* : Drain current limited by maximum junction temperature.

PIN CONNECTION

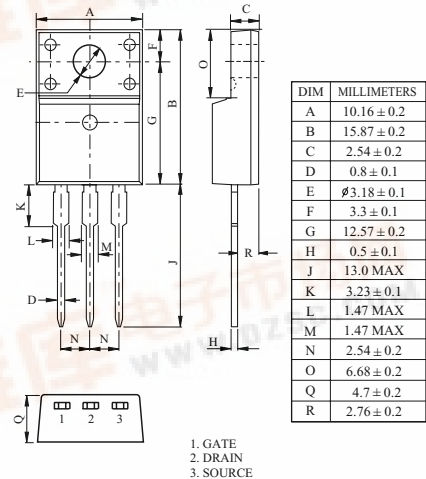


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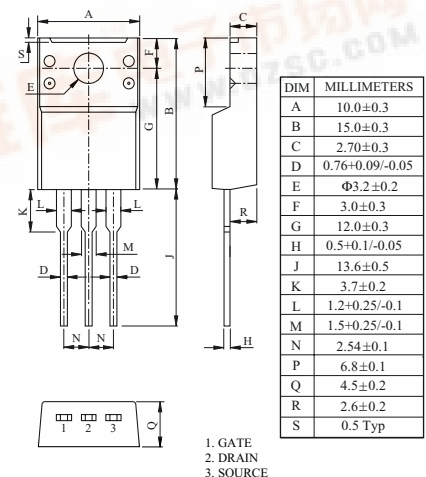
TO-220AB

KHB019N20F1



TO-220IS (1)

KHB019N20F2



TO-220IS

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ELECTRICAL CHARACTERISTICS (Tc=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	200	-	-	V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} / ΔT _j	I _D =250μA, Referenced to 25 °C	-	0.18	-	V/°C
Drain Cut-off Current	I _{DSS}	V _{DS} =200V, V _{GS} =0V,	-	-	±10	μA
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =250 μA	2	-	4	V
Gate Leakage Current	I _{GSS}	V _{GS} = ±30V, V _{DS} =0V	-	-	±100	nA
Drain-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =9.5A	-	0.14	0.18	Ω
Dynamic						
Total Gate Charge	Q _g	V _{DS} =160V, I _D =19A V _{GS} =10V (Note4,5)	-	35	44	nC
Gate-Source Charge	Q _{gs}		-	4.8	-	
Gate-Drain Charge	Q _{gd}		-	18	-	
Turn-on Delay time	t _{d(on)}	V _{DD} =100V R _L =5 Ω R _G =25 Ω (Note4,5)	-	12	30	ns
Turn-on Rise time	t _r		-	33	70	
Turn-off Delay time	t _{d(off)}		-	130	270	
Turn-off Fall time	t _f		-	75	160	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	900	1170	pF
Reverse Transfer Capacitance	C _{rss}		-	213	277	
Output Capacitance	C _{oss}		-	80	104	
Source-Drain Diode Ratings						
Continuous Source Current	I _S	V _{GS} <V _{th}	-	-	19	A
Pulsed Source Current	I _{SP}		-	-	76	
Diode Forward Voltage	V _{SD}	I _S =19A, V _{GS} =0V	-	-	1.5	V
Reverse Recovery Time	t _{rr}	I _S =19A, V _{GS} =0V, dIs/dt=100A/μs	-	215	-	ns
Reverse Recovery Charge	Q _{rr}		-	2	-	μC

Note 1) Repetivity rating : Pulse width limited by junction temperature.

Note 2) $L=1mH$, $I_S=19A$, $V_{DD}=50V$, $R_G=25\Omega$, Starting $T_j=25^\circ C$.

Note 3) $I_S \leq 19A$, $dI/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_j=25^\circ C$.

Note 4) Pulse Test : Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Note 5) Essentially independent of operating temperature.

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Fig1. $I_D - V_{DS}$

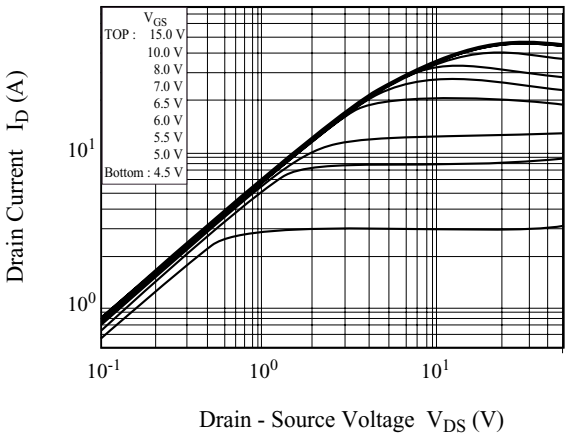


Fig2. $I_D - V_{GS}$

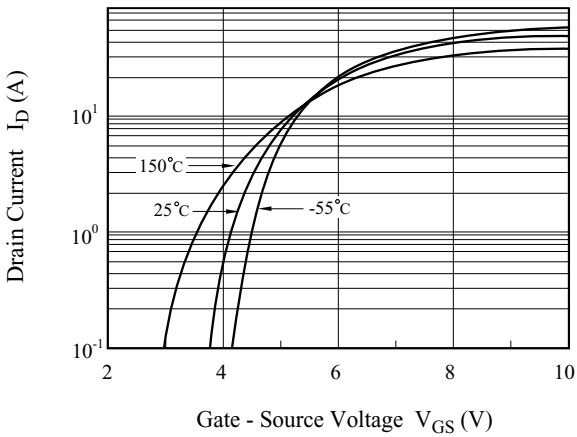


Fig3. $BV_{DSS} - T_j$

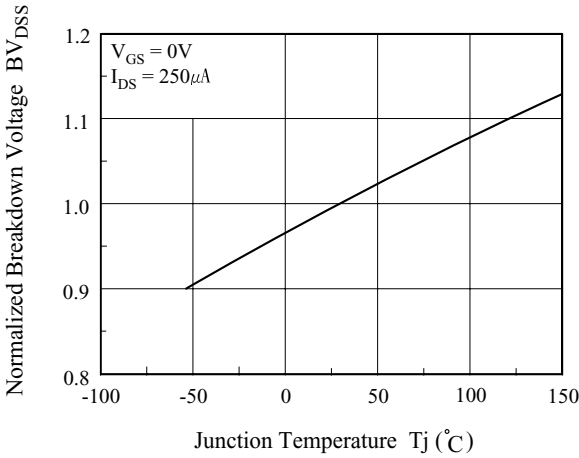


Fig4. $R_{DS(ON)} - I_D$

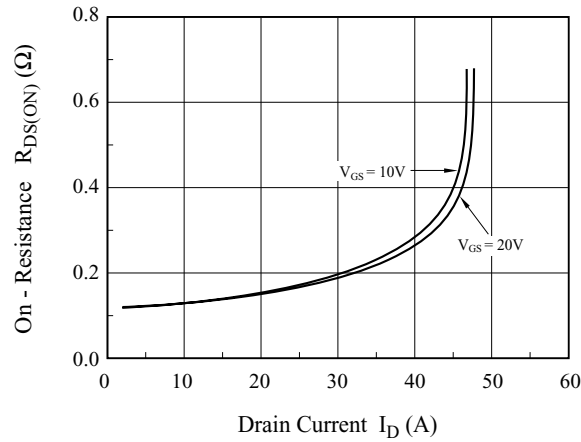


Fig5. $I_S - V_{SD}$

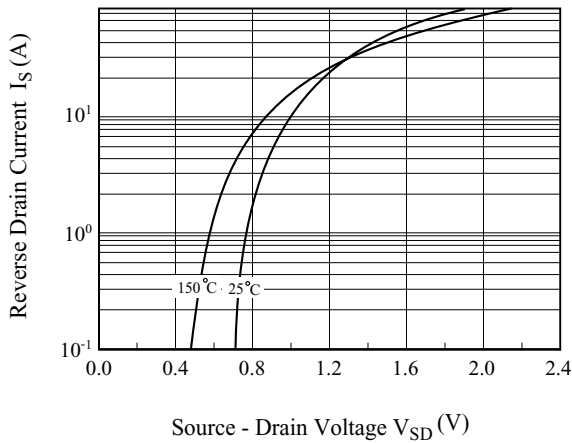
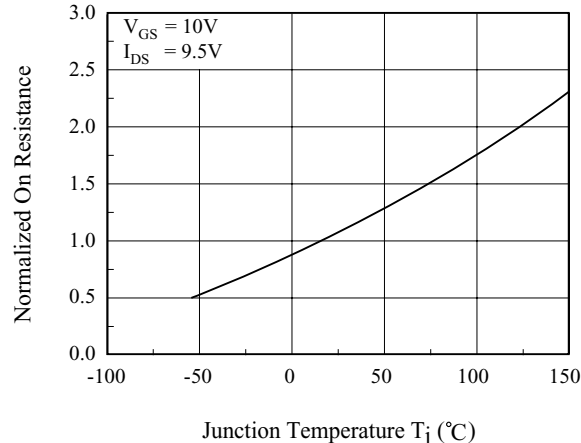


Fig6. $R_{DS(ON)} - T_j$



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Fig7. C - V_{DS}

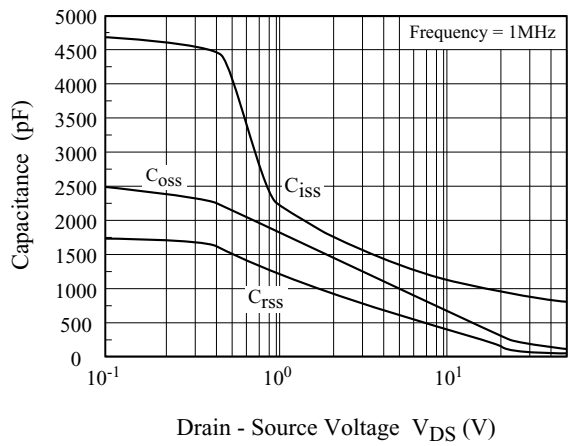


Fig8. Q_g - V_{GS}

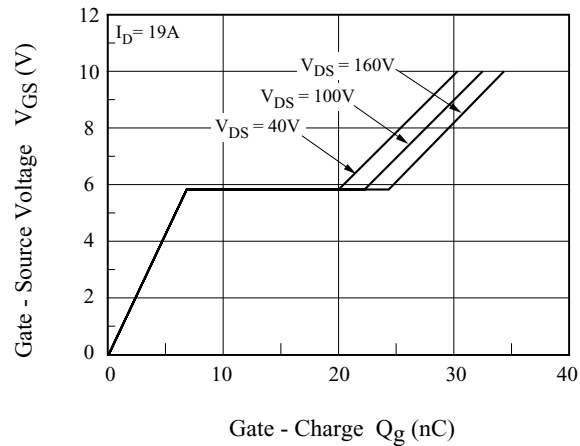


Fig9. Safe Operation Area

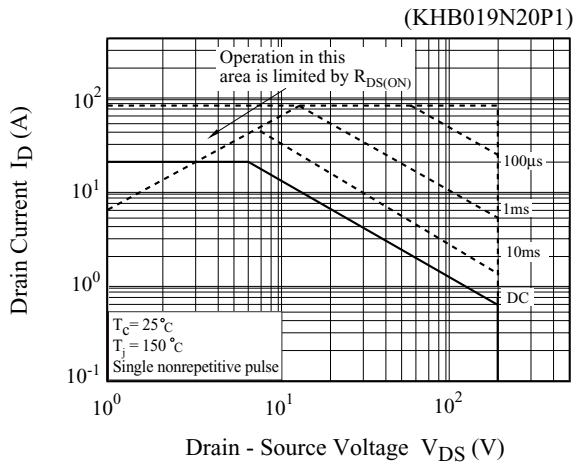


Fig10. Safe Operation Area

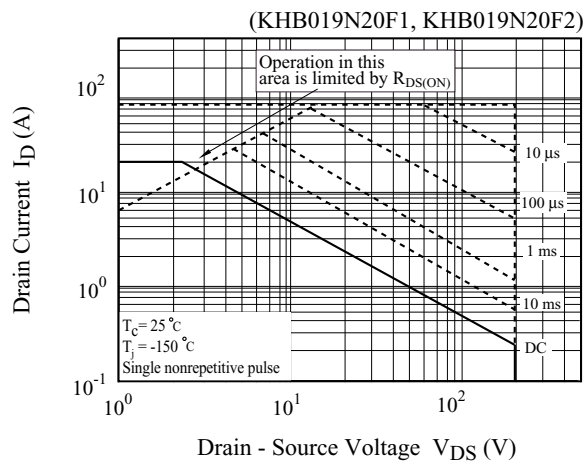
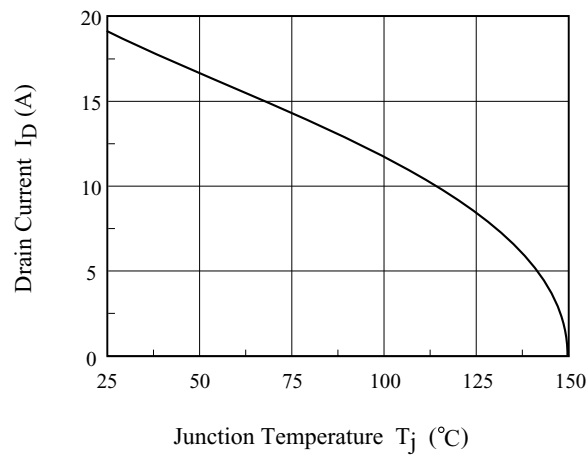


Fig11. I_D - T_j



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Fig12. Transient Thermal Response Curve

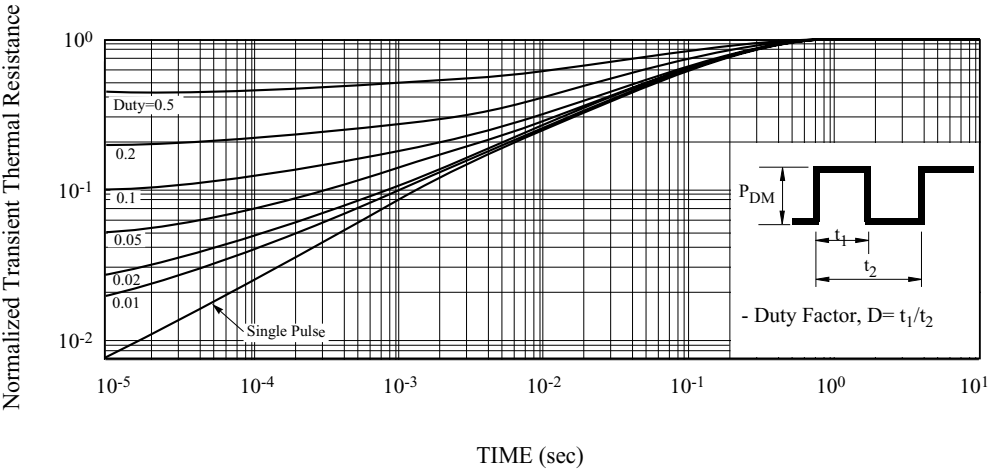
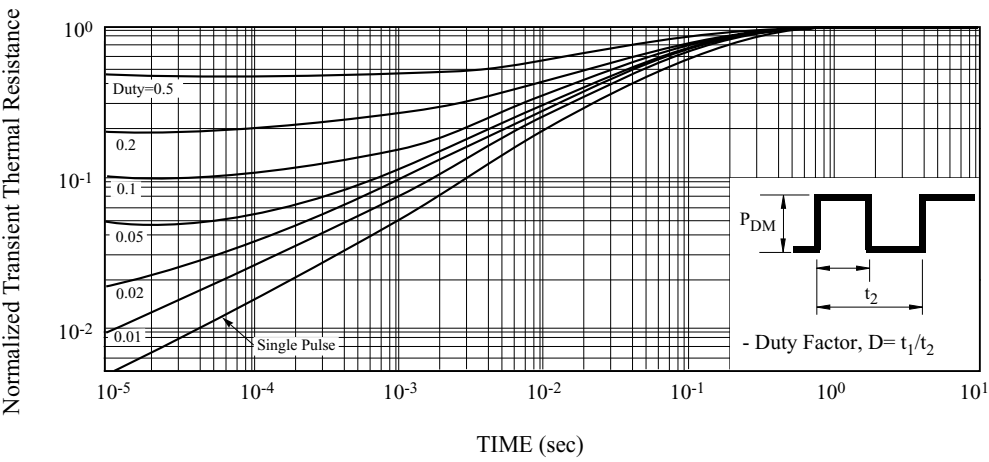


Fig13. Transient Thermal Response Curve



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Fig14. Gate Charge

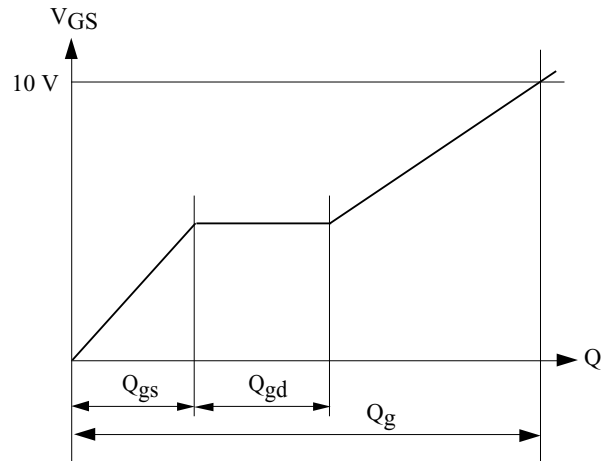
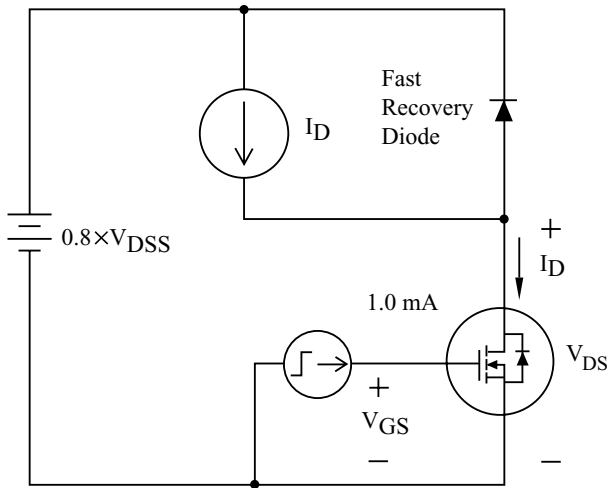
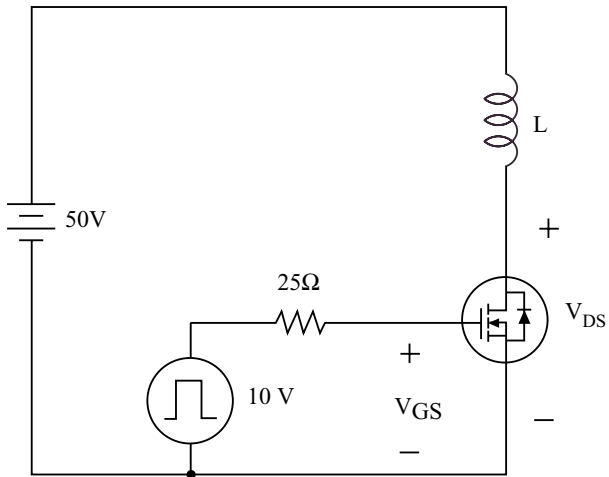


Fig15. Single Pulsed Avalanche Energy



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DS}}{BV_{DS} - V_{DD}}$$

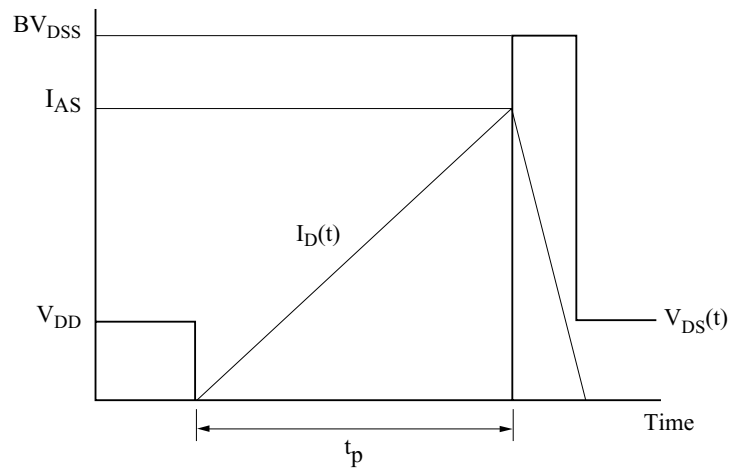
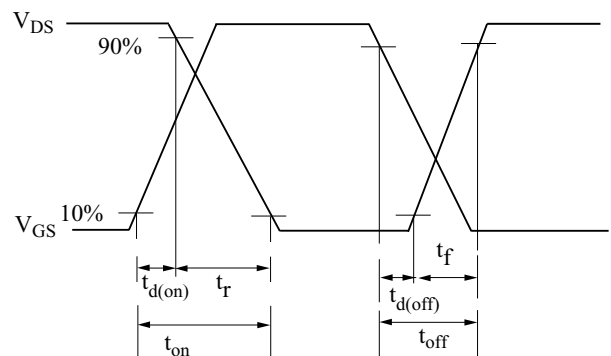
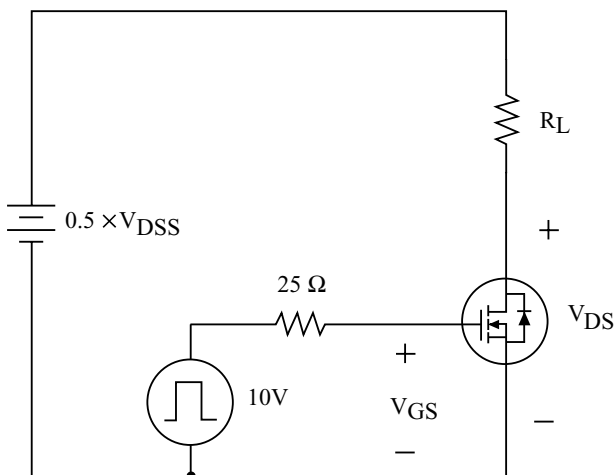


Fig16. Resistive Load Switching



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Fig17. Source - Drain Diode Reverse Recovery and dv /dt

